

Simple Mode

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

Architecture configurations available in this mode are similar to the common 10L8 and 12P6 devices with many permutations of generic output polarity or input choices.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

Pins 1 and 11 are always available as data inputs into the AND array. The center two macrocells (pins 15 & 16) cannot be used in the input configuration.

Pin 4 is used as dedicated power-down pin on GAL16LV8ZD. It cannot be used as a functional input.

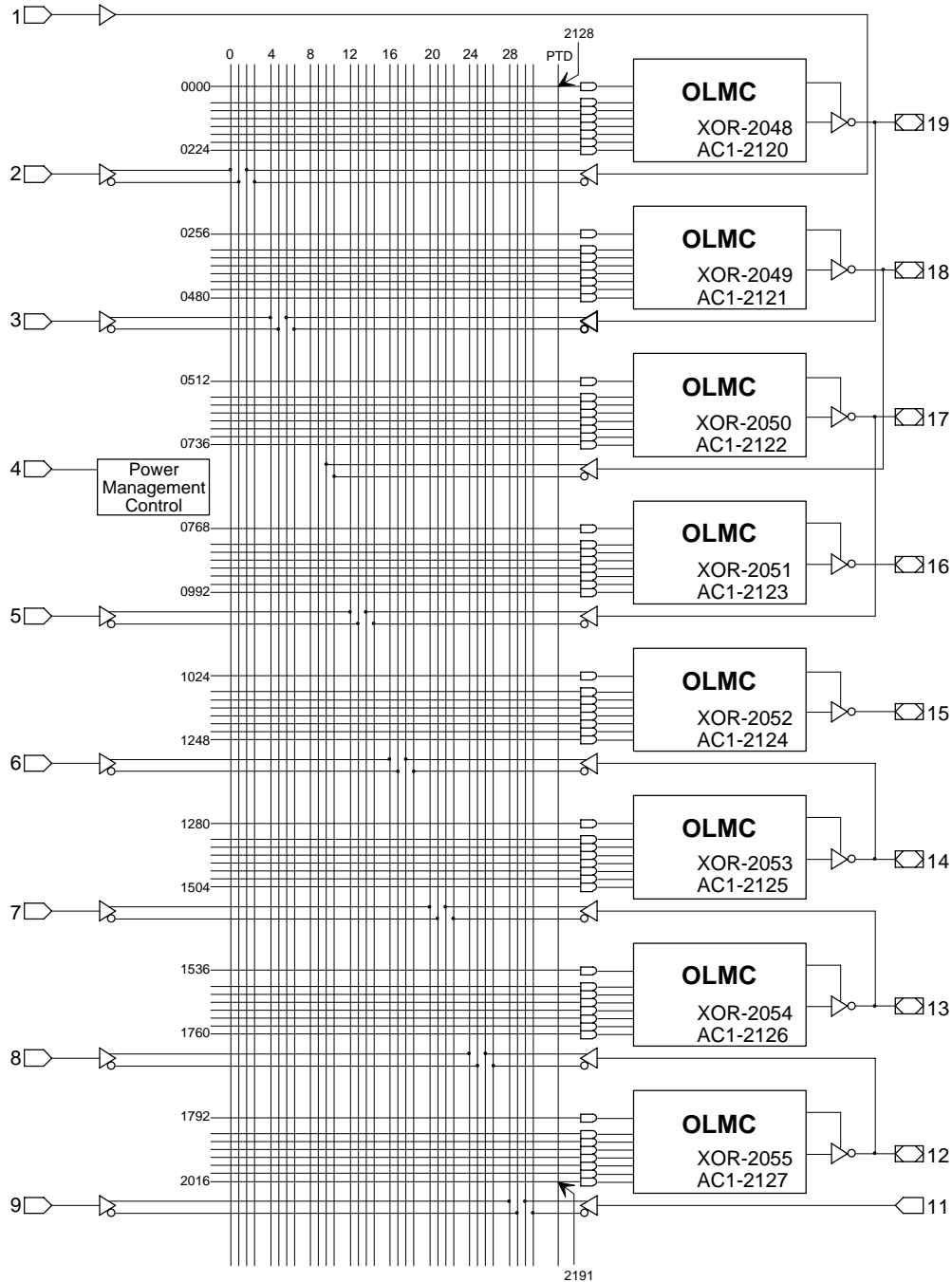
The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.

	<p>Combinatorial Output with Feedback Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - All OLMC except pins 15 & 16 can be configured to this function.
	<p>Combinatorial Output Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=0 defines this configuration. - Pins 15 & 16 are permanently configured to this function.
	<p>Dedicated Input Configuration for Simple Mode</p> <ul style="list-style-type: none"> - SYN=1. - AC0=0. - XOR=0 defines Active Low Output. - XOR=1 defines Active High Output. - AC1=1 defines this configuration. - All OLMC except pins 15 & 16 can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram

PLCC Package Pinout



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, 2118, 2119
Byte7 Byte6 Byte1 Byte0

MSB LSB

SYN-2192
AC0-2193

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Absolute Maximum Ratings⁽¹⁾

Supply voltage V_{CC}	-0.5 to +5.6V
Input voltage applied	-0.5 to +5.6V
Off-state output voltage applied	-0.5 to +5.6V
Storage Temperature	-65 to 150°C
Ambient Temperature with Power Applied	-55 to 125°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:

Ambient Temperature (T_A)	0 to +75°C
Supply voltage (V_{CC}) with Respect to Ground	+3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. ²	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS} - 0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	5.25	V
I_{IL}	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL} (MAX.)$	—	—	-10	μA
I_{IH}	Input or I/O High Leakage Current	$(V_{CC}-0.2)V \leq V_{IN} \leq V_{CC}$	—	—	10	μA
		$V_{CC} \leq V_{IN} \leq 5.25V$	—	—	1	mA
V_{OL}	Output Low Voltage	$I_{OL} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.5	V
		$I_{OL} = 0.5 \text{ mA } V_{in} = V_{IL} \text{ or } V_{IH}$	—	—	0.2	V
V_{OH}	Output High Voltage	$I_{OH} = MAX. V_{in} = V_{IL} \text{ or } V_{IH}$	2.4	—	—	V
		$I_{OH} = -0.5 \text{ mA } V_{in} = V_{IL} \text{ or } V_{IH}$	$V_{CC}-0.45$	—	—	V
		$I_{OH} = -100 \mu A V_{in} = V_{IL} \text{ or } V_{IH}$	$V_{CC}-0.2$	—	—	V
I_{OL}	Low Level Output Current		—	—	8	mA
I_{OH}	High Level Output Current		—	—	-8	mA
I_{OS}^1	Output Short Circuit Current	$V_{CC} = 3.3V V_{OUT} = GND T_A = 25^\circ C$	-30	—	-130	mA

COMMERCIAL

I_{SB}	Stand-by Power Supply Current	$V_{IL} = GND V_{IH} = V_{CC}$ Outputs Open	ZD -15/-25	—	50	100	μA
I_{CC}	Operating Power Supply Current	$V_{IL} = 0.5V V_{IH} = 3.0V$ $f_{toggle} = 15 \text{ MHz}$ Outputs Open	ZD -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.

2) Typical values are at $V_{CC} = 3.3V$ and $T_A = 25^\circ C$

AC Switching Characteristics

Over Recommended Operating Conditions

PARAM	TEST COND. ¹	DESCRIPTION	COM		COM		UNITS
			-15		-25		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinatorial Output	3	15	3	25	ns
t_{co}	A	Clock to Output Delay	2	10	2	15	ns
t_{cf}²	—	Clock to Feedback Delay	—	8	—	10	ns
t_{su}	—	Setup Time, Input or Fdbk before Clk↑	12	—	15	—	ns
t_h	—	Hold Time, Input or Fdbk after Clk↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	45.5	—	33.3	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	50	—	40	—	MHz
	A	Maximum Clock Frequency with No Feedback	62.5	—	41.6	—	MHz
t_{wh}	—	Clock Pulse Duration, High	8	—	12	—	ns
t_{wl}	—	Clock Pulse Duration, Low	8	—	12	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	17	—	25	ns
	B	$\overline{OE}\downarrow$ to Output Enabled	—	16	—	20	ns
t_{dis}	C	Input or I/O to Output Disabled	—	18	—	25	ns
	C	$\overline{OE}\uparrow$ to Output Disabled	—	17	—	20	ns

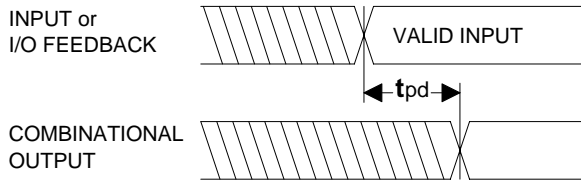
- 1) Refer to **Switching Test Conditions** section.
- 2) Calculated from f_{max} with internal feedback. Refer to **f_{max} Description** section.
- 3) Refer to **f_{max} Description** section.

Capacitance (T_A = 25°C, f = 1.0 MHz)

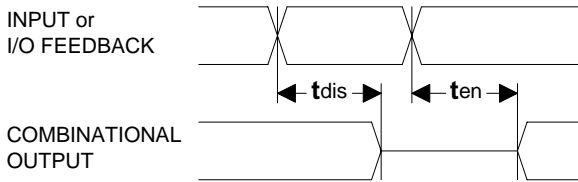
SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C _I	Input Capacitance	8	pF	V _{CC} = 3.3V, V _I = 0V
C _{I/O}	I/O Capacitance	8	pF	V _{CC} = 3.3V, V _{I/O} = 0V

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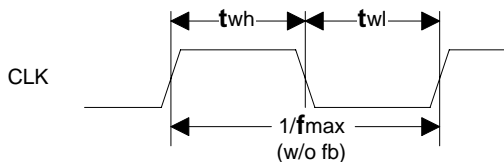
Switching Waveforms



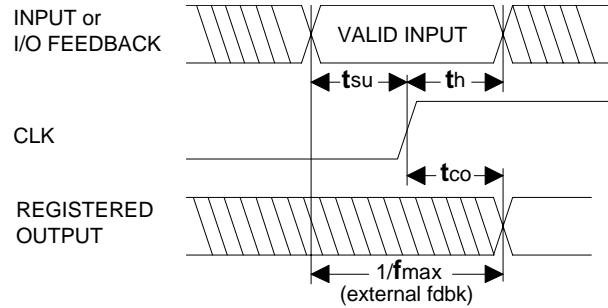
Combinatorial Output



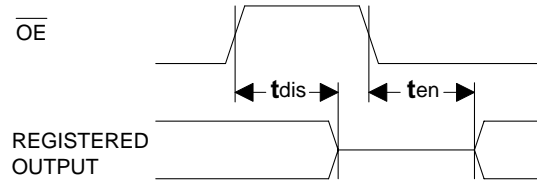
Input or I/O to Output Enable/Disable



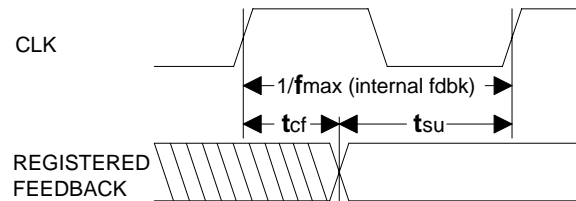
Clock Width



Registered Output



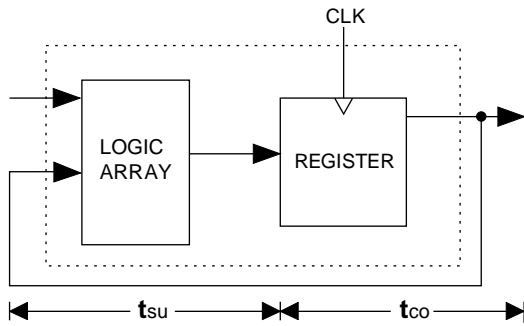
OE to Output Enable/Disable



f_{max} with Feedback

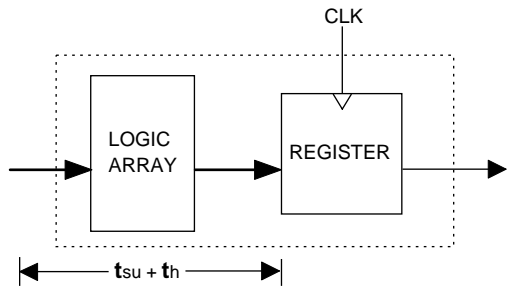
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f_{max} Descriptions



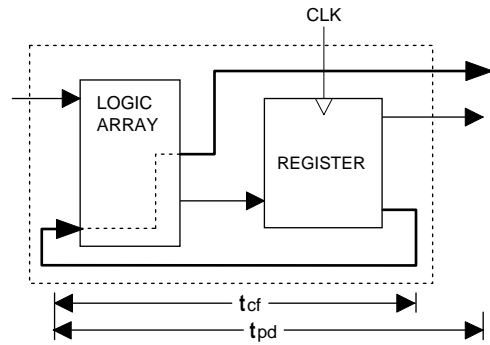
f_{max} with External Feedback 1/(t_{su}+t_{co})

Note: f_{max} with external feedback is calculated from measured t_{su} and t_{co}.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(t_{wh} + t_{wl}). This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback 1/(t_{su}+t_{cf})

Note: t_{cf} is a calculated value, derived by subtracting t_{su} from the period of f_{max} w/internal feedback (t_{cf} = 1/f_{max} - t_{su}). The value of t_{cf} is used primarily when calculating the delay from clocking a register to a combinational output (through registered feedback), as shown above. For example, the timing from clock to a combinational output is equal to t_{cf} + t_{pd}.

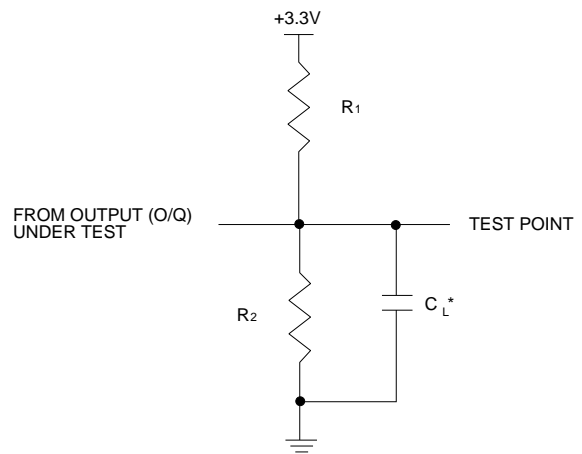
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	2ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level. 3-state to active transitions are measured at (V_{oh} - 0.5) V and (V_{ol} + 0.5) V.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L	
A	270Ω	220Ω	35pF	
B	Active High	270Ω	220Ω	35pF
	Active Low	270Ω	220Ω	35pF
C	Active High	270Ω	220Ω	5pF
	Active Low	270Ω	220Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

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Electronic Signature

An electronic signature word is provided in every GAL16LV8ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

Security Cell

A security cell is provided in the GAL16LV8ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available regardless of the security cell state.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

The GAL16LV8ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

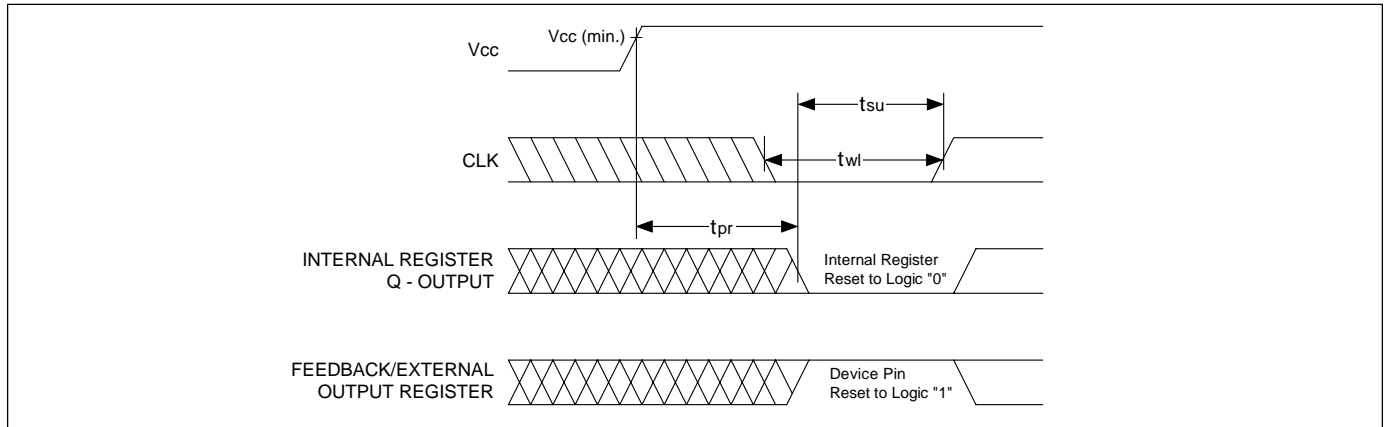
Input Buffers

GAL16LV8ZD devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

Dedicated Power-Down Pin

The GAL16LV8ZD uses pin 4 as the dedicated power-down signal to put the device in to the power-down state. DPP is an active high signal where a logic high driven on this signal puts the device into power-down state. Input pin 4 cannot be used as a logic function input on this device.

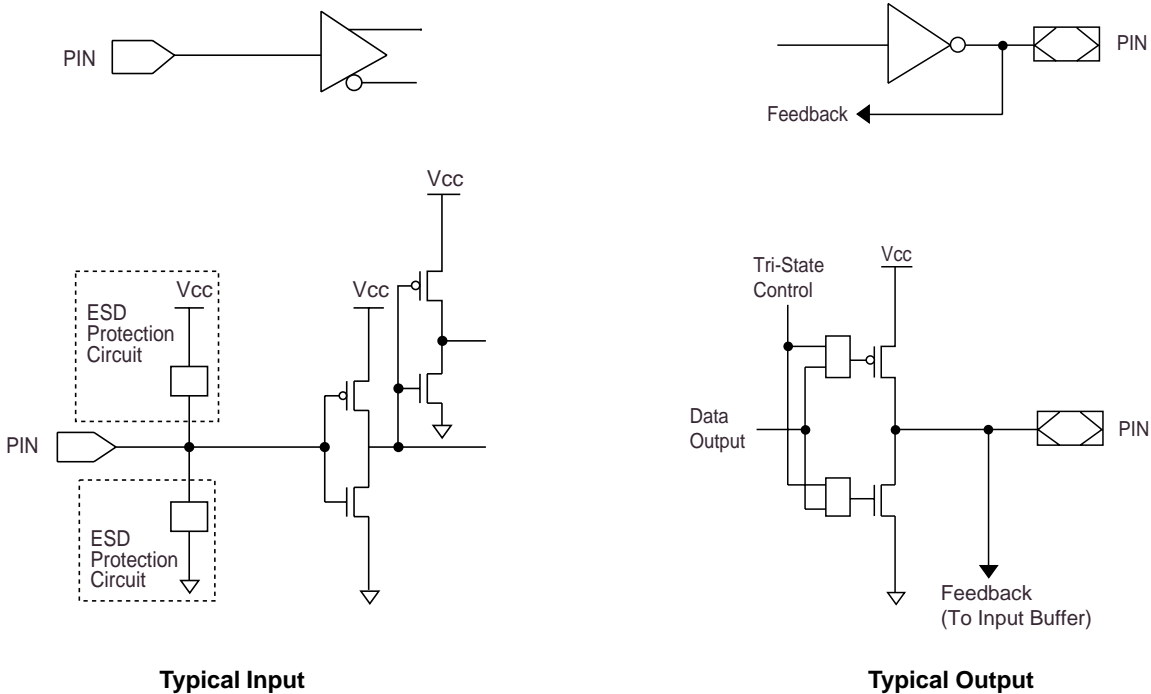
Power-Up Reset



Circuitry within the GAL16LV8ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 10μs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the

asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL16LV8ZD. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



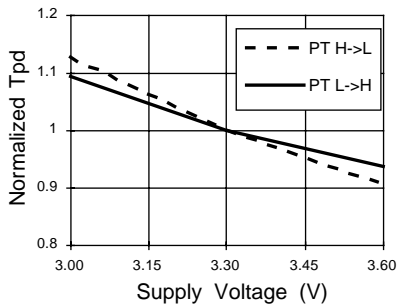
Typical Input

Typical Output

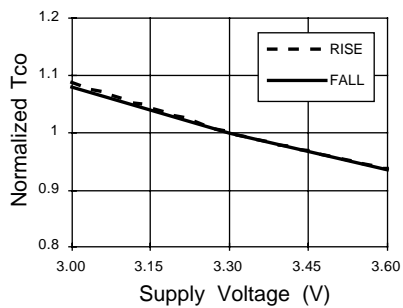
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Typical AC and DC Characteristics

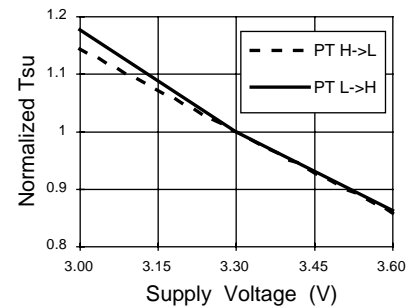
Normalized Tpd vs Vcc



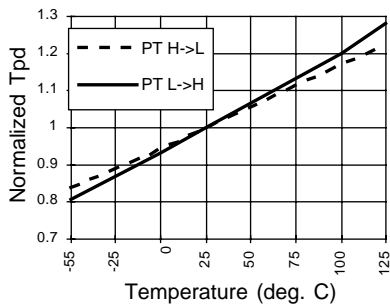
Normalized Tco vs Vcc



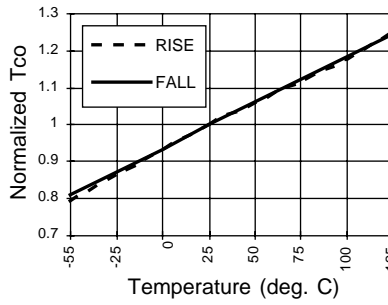
Normalized Tsu vs Vcc



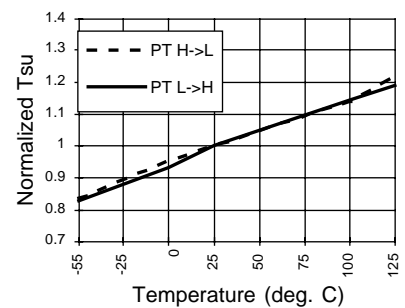
Normalized Tpd vs Temp



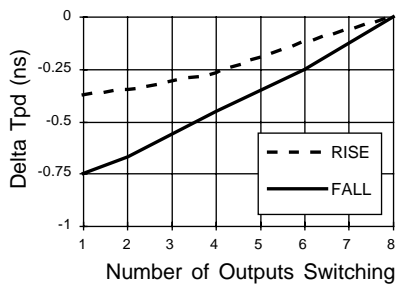
Normalized Tco vs Temp



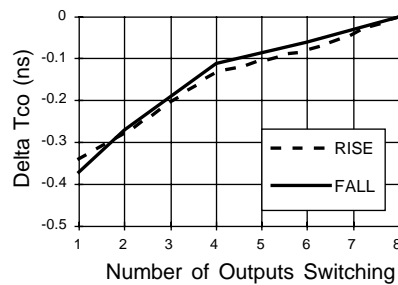
Normalized Tsu vs Temp



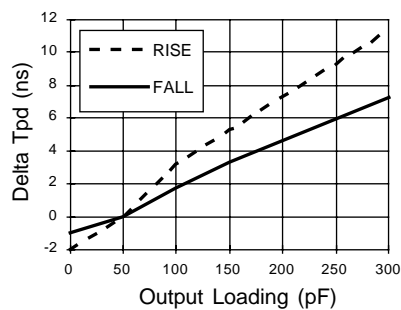
Delta Tpd vs # of Outputs Switching



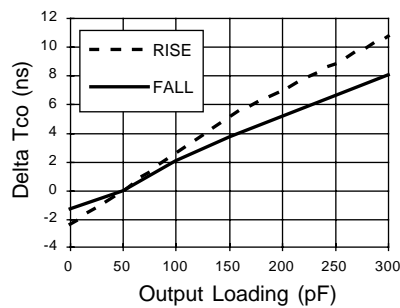
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading



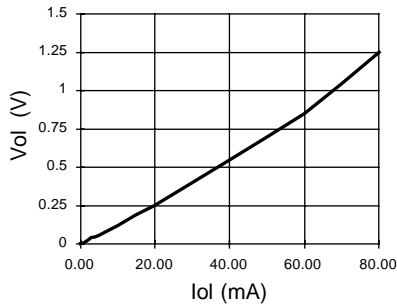
Delta Tco vs Output Loading



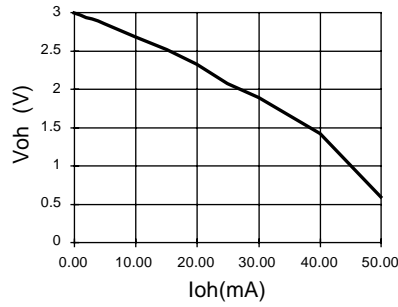
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Typical AC and DC Characteristics

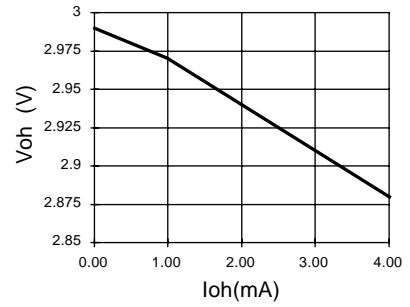
Vol vs Iol



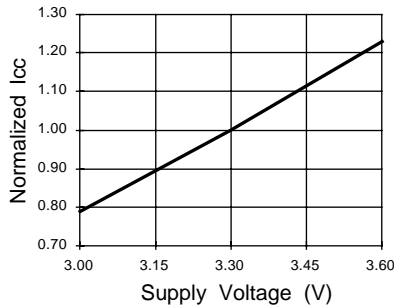
Voh vs Ioh



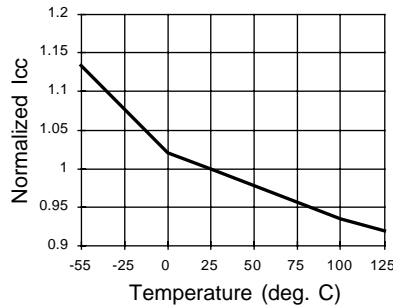
Voh vs Ioh



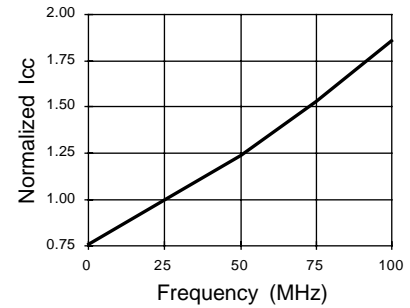
Normalized Icc vs Vcc



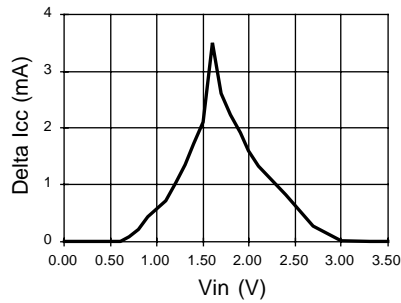
Normalized Icc vs Temp



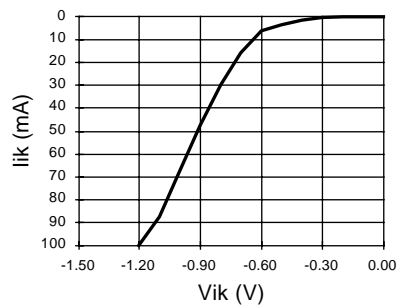
Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Iik)



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