

Absolute Maximum Ratings⁽¹⁾

Supply voltage V_{CC} -0.5 to +4.6V
 Input voltage applied -0.5 to +5.6V
 I/O voltage applied -0.5 to +4.6V
 Off-state output voltage applied -0.5 to +4.6V
 Storage Temperature -65 to 150°C
 Ambient Temperature with
 Power Applied -55 to 125°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
 Ambient Temperature (T_A) 0 to 75°C
 Supply voltage (V_{CC})
 with Respect to Ground +3.0 to +3.6V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP. ³ | MAX. | UNITS |
|------------|-----------------------------------|---|-----------------|-------------------|----------------|---------|
| V_{IL} | Input Low Voltage | | $V_{SS} - 0.3$ | — | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.0 | — | 5.25 | V |
| | I/O High Voltage | | 2.0 | — | $V_{CC} + 0.5$ | V |
| I_{IL}^1 | Input or I/O Low Leakage Current | $0V \leq V_{IN} \leq V_{IL} (MAX.)$ | — | — | -100 | μA |
| I_{IH} | Input or I/O High Leakage Current | $(V_{CC} - 0.2)V \leq V_{IN} \leq V_{CC}$ | — | — | 10 | μA |
| | Input High Leakage Current | $V_{CC} \leq V_{IN} \leq 5.25V$ | — | — | 10 | μA |
| | I/O High Leakage Current | $V_{CC} \leq V_{IN} \leq 4.6V$ | — | — | 20 | mA |
| V_{OL} | Output Low Voltage | $I_{OL} = MAX. \quad V_{in} = V_{IL} \text{ or } V_{IH}$ | — | — | 0.4 | V |
| | | $I_{OL} = 500\mu A \quad V_{in} = V_{IL} \text{ or } V_{IH}$ | — | — | 0.2 | V |
| V_{OH} | Output High Voltage | $I_{OH} = MAX. \quad V_{in} = V_{IL} \text{ or } V_{IH}$ | 2.4 | — | — | V |
| | | $I_{OH} = -100\mu A \quad V_{in} = V_{IL} \text{ or } V_{IH}$ | $V_{CC} - 0.2V$ | — | — | V |
| I_{OL} | Low Level Output Current | | — | — | 8 | mA |
| I_{OH} | High Level Output Current | | — | — | -8 | mA |
| I_{OS}^2 | Output Short Circuit Current | $V_{CC} = 3.3V \quad V_{OUT} = 0.5V \quad T_A = 25^\circ C$ | -15 | — | -80 | mA |

COMMERCIAL

| | | | | | | |
|----------|-----------------|---|---|----|----|----|
| I_{CC} | Operating Power | $V_{IL} = 0V \quad V_{IH} = 3.0V$ Unused Inputs at V_{IL} | — | 45 | 70 | mA |
| | Supply Current | $f_{toggle} = 1MHz$ Outputs Open | | | | |

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
 2) One output at a time for a maximum duration of one second. $V_{out} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Characterized but not 100% tested.
 3) Typical values are at $V_{CC} = 3.3V$ and $T_A = 25^\circ C$

AC Switching Characteristics

Over Recommended Operating Conditions

| PARAMETER | TEST COND ¹ . | DESCRIPTION | COM | | COM | | COM | | UNITS |
|-------------------------------------|--------------------------|--|------|------|-------|------|------|------|-------|
| | | | -3 | | -5 | | -7 | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| t_{pd} ² | A | Input or I/O to Combinational Output | 1 | 3.5 | 1 | 5 | 1 | 7.5 | ns |
| t_{co} ² | A | Clock to Output Delay | 1 | 2.5 | 1 | 3 | 1 | 5 | ns |
| t_{cf} ³ | — | Clock to Feedback Delay | — | 2 | — | 2 | — | 3 | ns |
| t_{su} | — | Setup Time, Input or Feedback before Clock [↑] | 3 | — | 4 | — | 5 | — | ns |
| t_h | — | Hold Time, Input or Feedback after Clock [↑] | 0 | — | 0 | — | 0 | — | ns |
| f_{max} ⁴ | A | Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co}) | 180 | — | 142.8 | — | 100 | — | MHz |
| | A | Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf}) | 200 | — | 166 | — | 125 | — | MHz |
| | A | Maximum Clock Frequency with No Feedback | 250 | — | 166 | — | 125 | — | MHz |
| t_{wh} ⁴ | — | Clock Pulse Duration, High | 2 | — | 3 | — | 4 | — | ns |
| t_{wl} ⁴ | — | Clock Pulse Duration, Low | 2 | — | 3 | — | 4 | — | ns |
| t_{en} | B | Input or I/O to Output Enabled | — | 4.5 | — | 6 | — | 7.5 | ns |
| | B | \overline{OE} to Output Enabled | — | 3.5 | — | 5 | — | 6.5 | ns |
| t_{dis} | C | Input or I/O to Output Disabled | — | 4.5 | — | 6 | — | 7.5 | ns |
| | C | \overline{OE} to Output Disabled | — | 3.5 | — | 5 | — | 6.5 | ns |

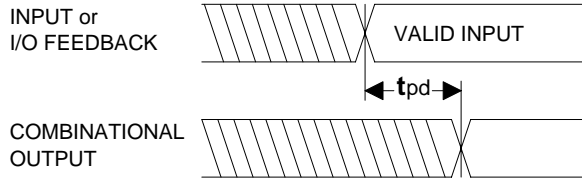
- 1) Refer to **Switching Test Conditions** section.
- 2) Minimum values for **t_{pd}** and **t_{co}** are not 100% tested but established by characterization.
- 3) Calculated from **f_{max}** with internal feedback. Refer to **f_{max} Descriptions** section.
- 4) Refer to **f_{max} Descriptions** section. Characterized but not 100% tested.

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

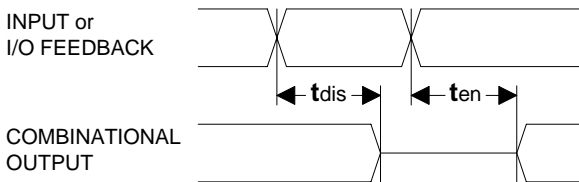
| SYMBOL | PARAMETER | TYPICAL | UNITS | TEST CONDITIONS |
|----------|-------------------|---------|-------|------------------------------|
| C_I | Input Capacitance | 5 | pF | $V_{CC} = 3.3V, V_I = 0V$ |
| C_{IO} | I/O Capacitance | 5 | pF | $V_{CC} = 3.3V, V_{IO} = 0V$ |

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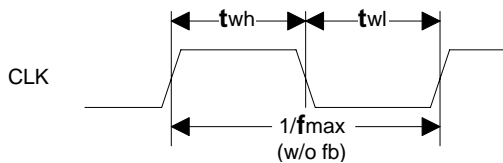
Switching Waveforms



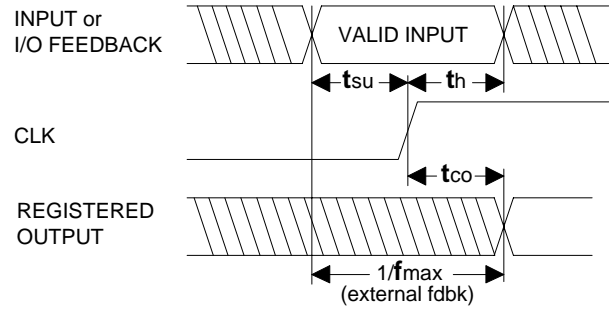
Combinatorial Output



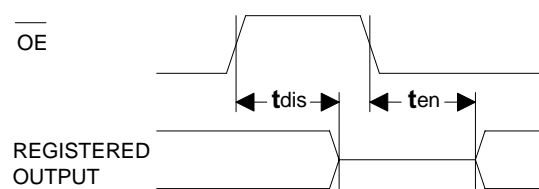
Input or I/O to Output Enable/Disable



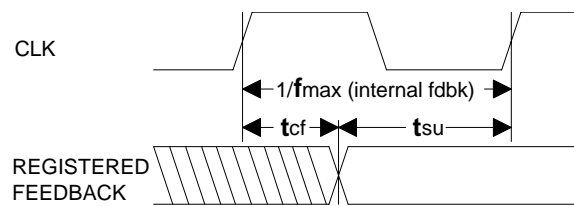
Clock Width



Registered Output



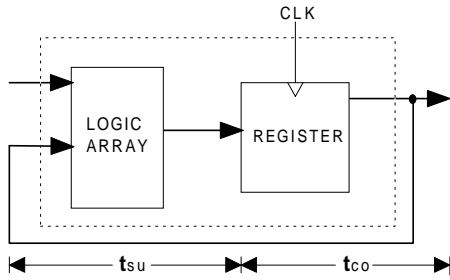
OE to Output Enable/Disable



fmax with Feedback

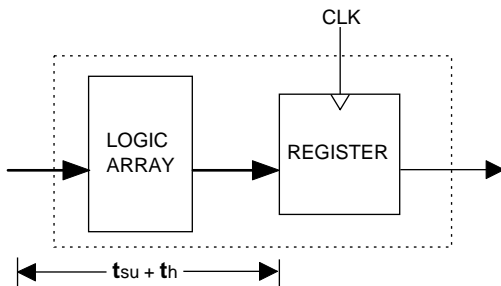
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f_{max} Descriptions



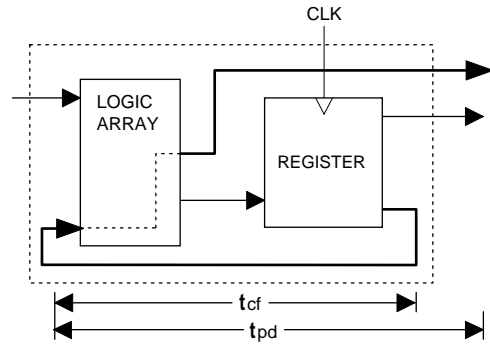
f_{max} with External Feedback 1/(tsu+tco)

Note: f_{max} with external feedback is calculated from measured tsu and tco.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback 1/(tsu+tcf)

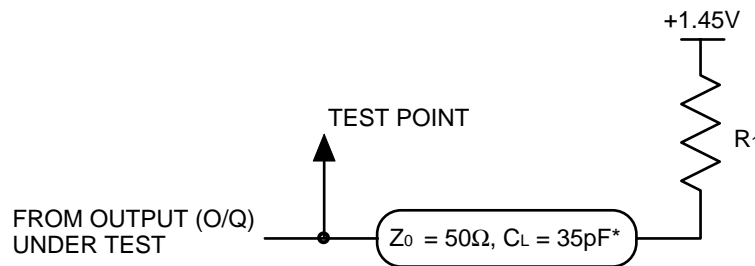
Note: tcf is a calculated value, derived by subtracting tsu from the period of f_{max} w/internal feedback (tcf = 1/f_{max} - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

Switching Test Conditions

| | |
|--------------------------------|-----------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 1.5ns 10% – 90% |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See Figure |

Output Load Conditions (see figure)

| Test Condition | | R ₁ | C _L |
|----------------|-------------------------------|----------------|----------------|
| A | | 50Ω | 35pF |
| B | High Z to Active High at 1.9V | 50Ω | 35pF |
| | High Z to Active Low at 1.0V | 50Ω | 35pF |
| C | Active High to High Z at 1.9V | 50Ω | 35pF |
| | Active Low to High Z at 1.0V | 50Ω | 35pF |



*C_L includes test fixture and probe capacitance.

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Electronic Signature

An electronic signature is provided in every GAL20LV8D device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

Security Cell

A security cell is provided in the GAL20LV8D devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

Latch-Up Protection

GAL20LV8D devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias minimizes the potential of latch-up caused by negative input undershoots.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

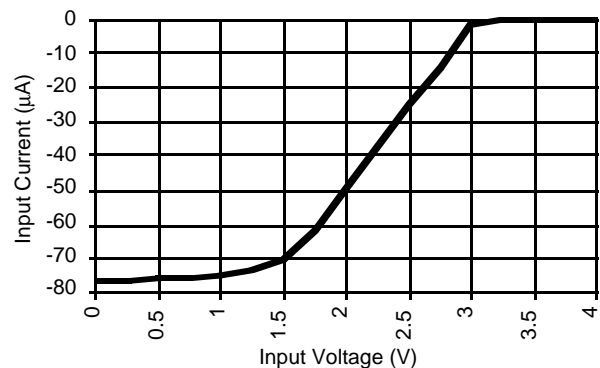
GAL20LV8D devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

Input Buffers

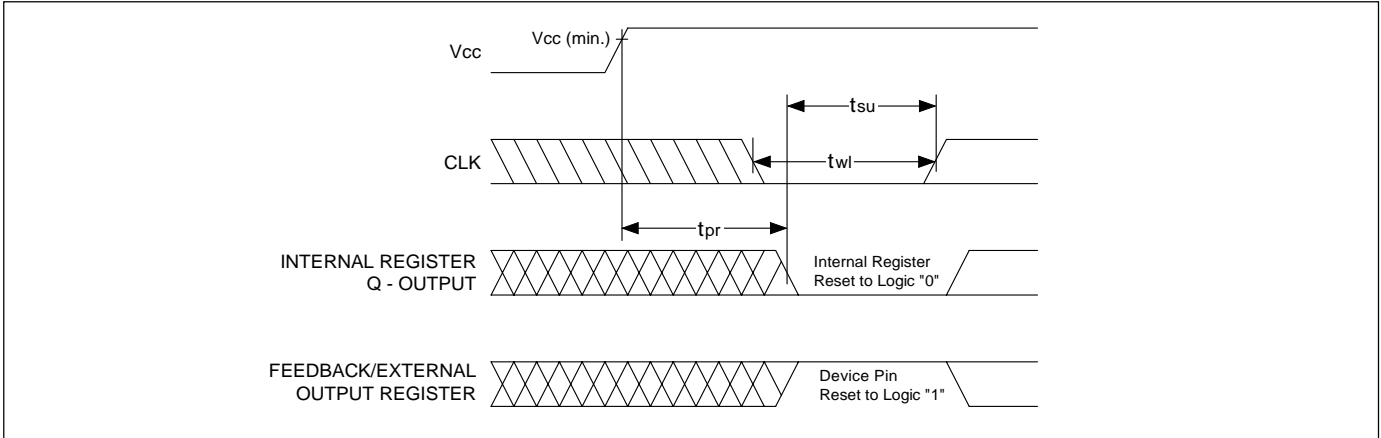
GAL20LV8D devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

The GAL20LV8D input and I/O pins have built-in active pull-ups. As a result, unused inputs and I/Os will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or Ground. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Pull-up Characteristic



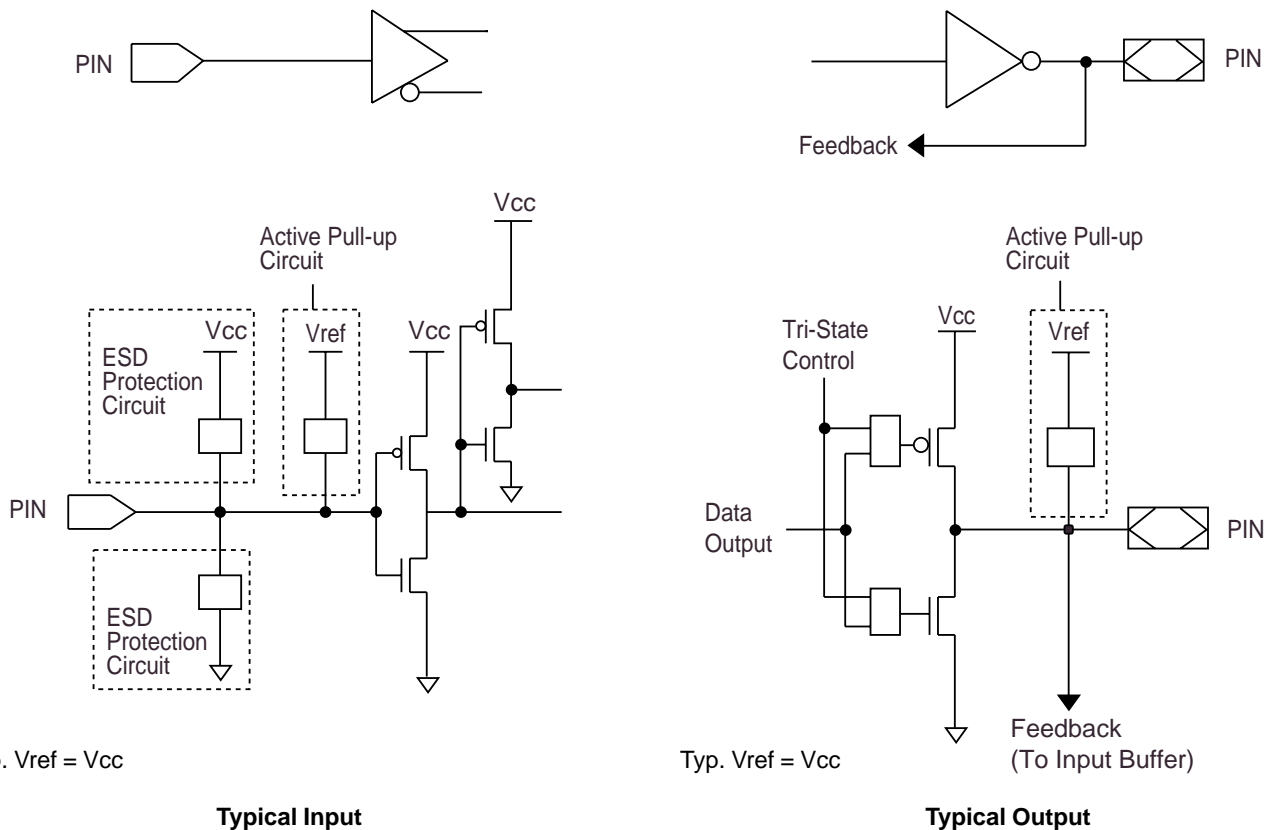
Power-Up Reset



Circuitry within the GAL20LV8D provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1μs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. Because of the asynchronous nature of system power-up, some conditions must be met to

provide a valid power-up reset of the device. First, the Vcc rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

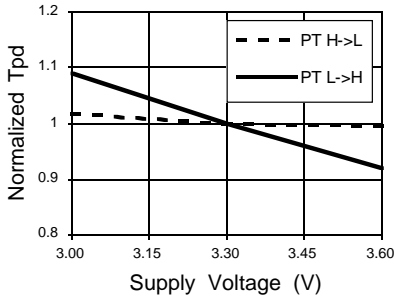
Input/Output Equivalent Schematics



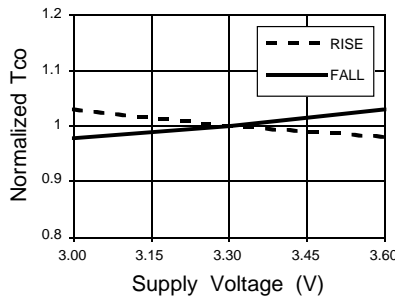
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Typical AC and DC Characteristic Diagrams

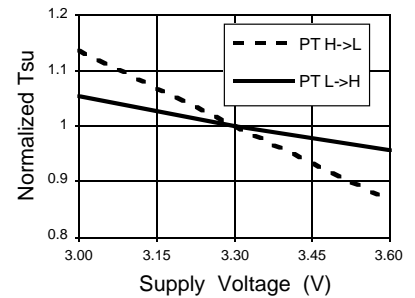
Normalized Tpd vs Vcc



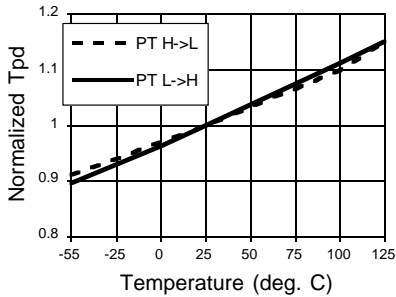
Normalized Tco vs Vcc



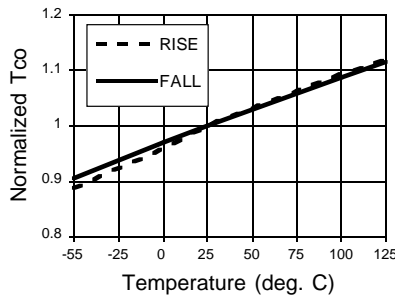
Normalized Tsu vs Vcc



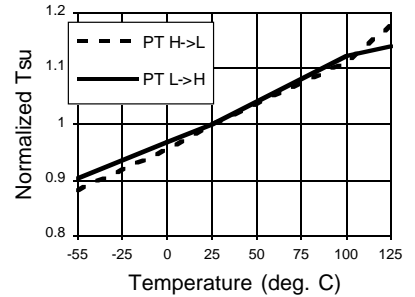
Normalized Tpd vs Temp



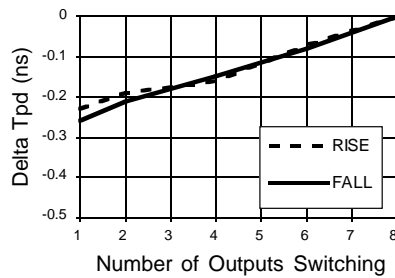
Normalized Tco vs Temp



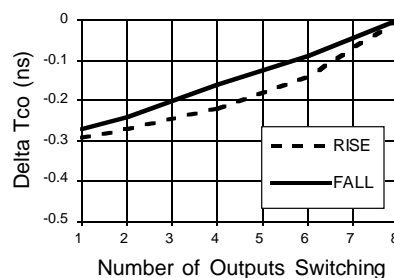
Normalized Tsu vs Temp



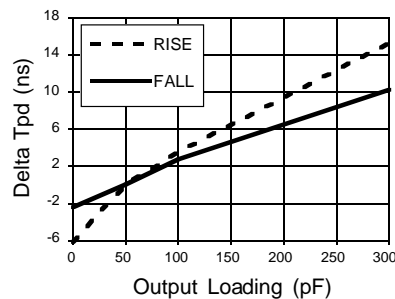
Delta Tpd vs # of Outputs Switching



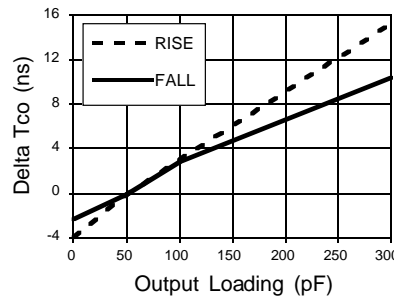
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

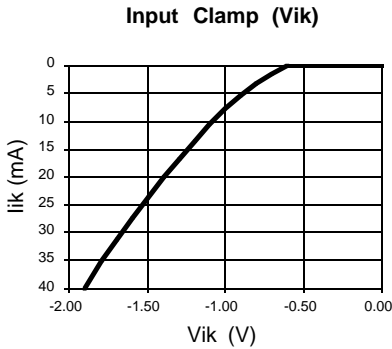
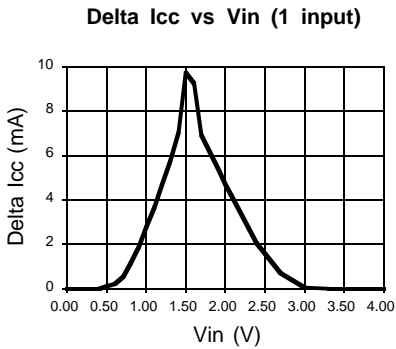
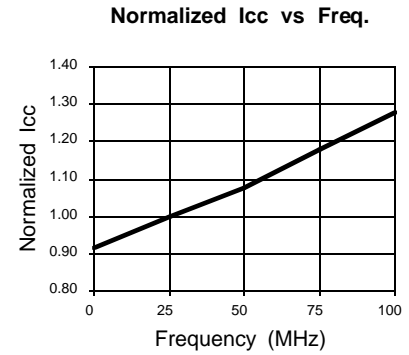
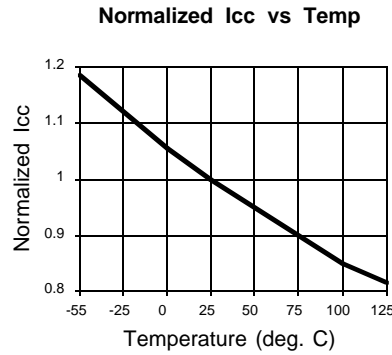
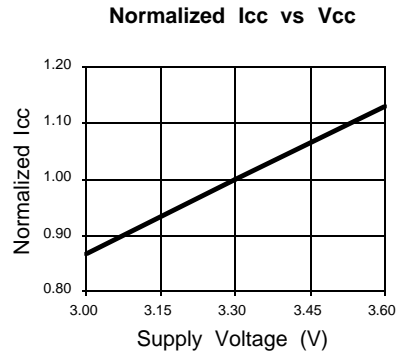
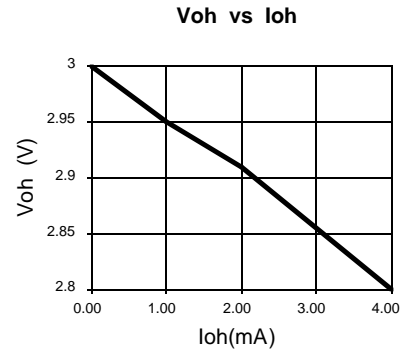
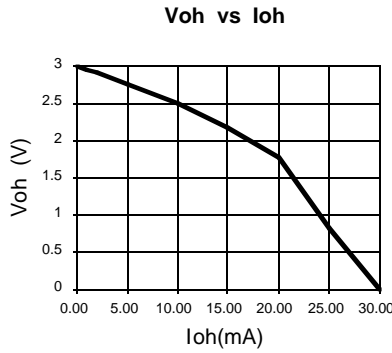
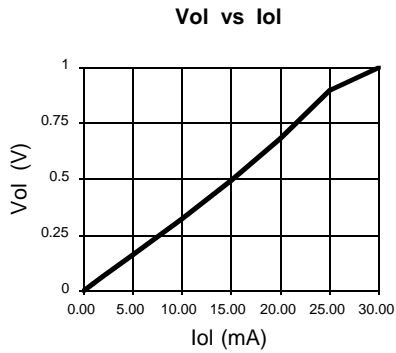


Delta Tco vs Output Loading



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Typical AC and DC Characteristic Diagrams



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