

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM		COM		UNITS
			-12		-15		
			MIN.	MAX.	MIN.	MAX.	
t_{pd}	A	Input or I/O to Combinational Output	3	12	3	15	ns
t_{co}	A	Clock to Output Delay	2	8	2	10	ns
t_{cf}²	—	Clock to Feedback Delay	—	6	—	7	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	10	—	15	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}³	A	Maximum Clock Frequency with External Feedback, 1/(t _{su} + t _{co})	55	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(t _{su} + t _{cf})	62.5	—	45.5	—	MHz
	A	Maximum Clock Frequency with No Feedback	83.3	—	62.5	—	MHz
t_{wh}	—	Clock Pulse Duration, High	6	—	8	—	ns
t_{wl}	—	Clock Pulse Duration, Low	6	—	8	—	ns
t_{en}	B	Input or I/O to Output Enabled	—	12	—	15	ns
	B	\overline{OE} to Output Enabled	—	12	—	15	ns
t_{dis}	C	Input or I/O to Output Disabled	—	15	—	15	ns
	C	\overline{OE} to Output Disabled	—	12	—	15	ns

1) Refer to **Switching Test Conditions** section.

2) Calculated from **f_{max}** with internal feedback. Refer to **f_{max} Specification** section.

3) Refer to **f_{max} Specification** section.

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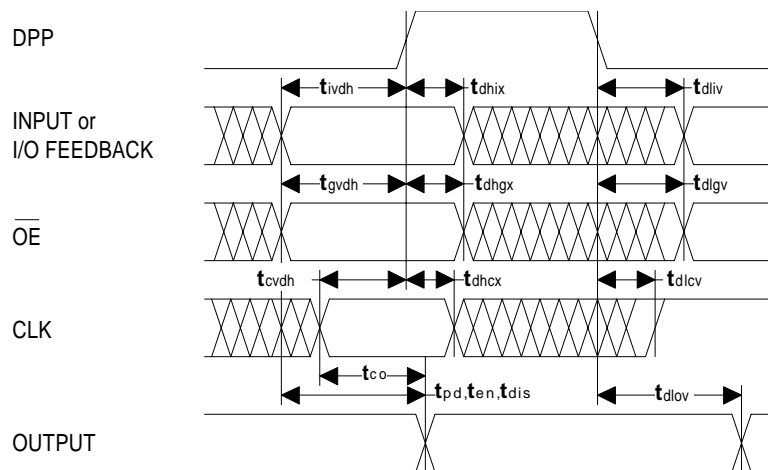
Dedicated Power-Down Pin Specifications

Over Recommended Operating Conditions

PARAMETER	TEST COND ¹ .	DESCRIPTION	COM -12		COM -15		UNITS
			MIN.	MAX.	MIN.	MAX.	
			t_{whd}	—	DPP Pulse Duration High	12	
t_{wld}	—	DPP Pulse Duration Low	25	—	30	—	ns
ACTIVE TO STANDBY							
t_{ivdh}	—	Valid Input before DPP High	5	—	8	—	ns
t_{gvdh}	—	Valid OE before DPP High	0	—	0	—	ns
t_{cvdh}	—	Valid Clock Before DPP High	0	—	0	—	ns
t_{dhix}	—	Input Don't Care after DPP High	—	2	—	5	ns
t_{dhgx}	—	\overline{OE} Don't Care after DPP High	—	6	—	9	ns
t_{dhcx}	—	Clock Don't Care after DPP High	—	8	—	11	ns
STANDBY TO ACTIVE							
t_{dliv}	—	DPP Low to Valid Input	12	—	15	—	ns
t_{dlgv}	—	DPP Low to Valid \overline{OE}	16	—	20	—	ns
t_{dlcv}	—	DPP Low to Valid Clock	18	—	20	—	ns
t_{dlov}	A	DPP Low to Valid Output	5	24	5	30	ns

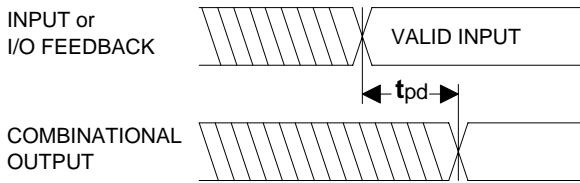
1) Refer to **Switching Test Conditions** section.

Dedicated Power-Down Pin Timing Waveforms

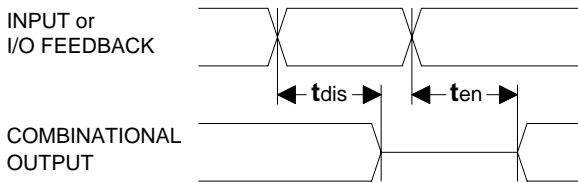


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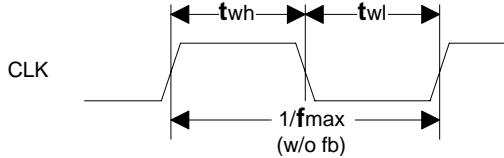
Switching Waveforms



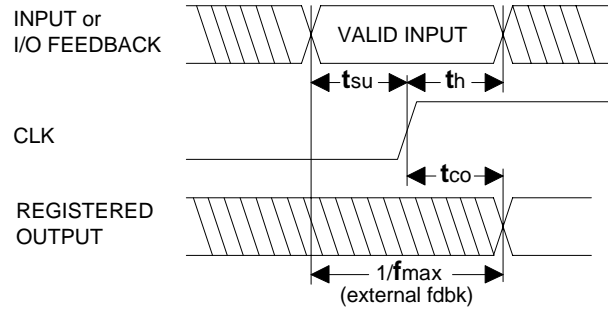
Combinatorial Output



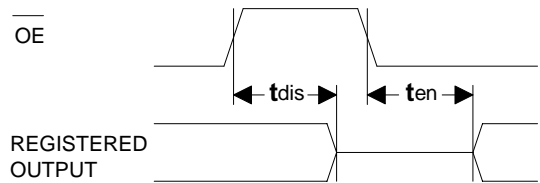
Input or I/O to Output Enable/Disable



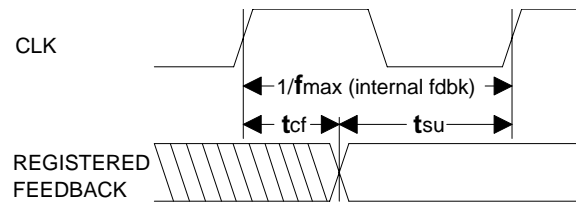
Clock Width



Registered Output



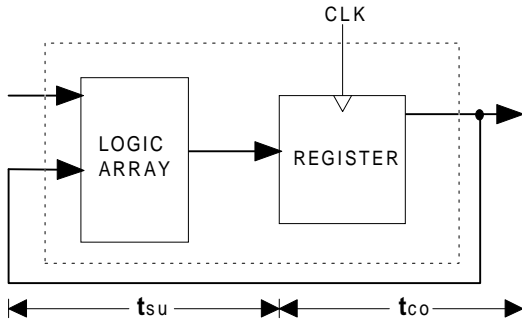
OE to Output Enable/Disable



fmax with Feedback

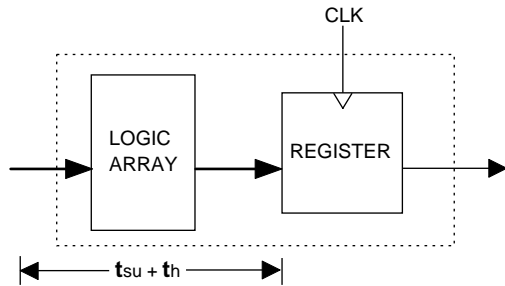
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f_{max} Specifications



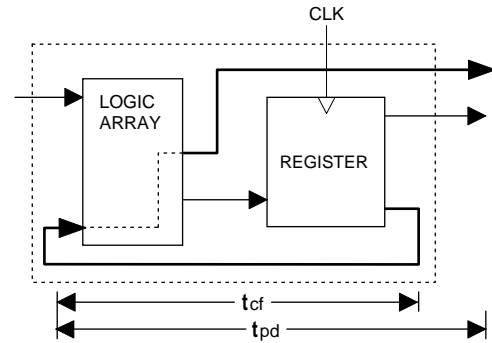
f_{max} with External Feedback 1/(tsu+tco)

Note: f_{max} with external feedback is calculated from measured tsu and tco.



f_{max} with No Feedback

Note: f_{max} with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



f_{max} with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of f_{max} w/internal feedback (tcf = 1/f_{max} - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

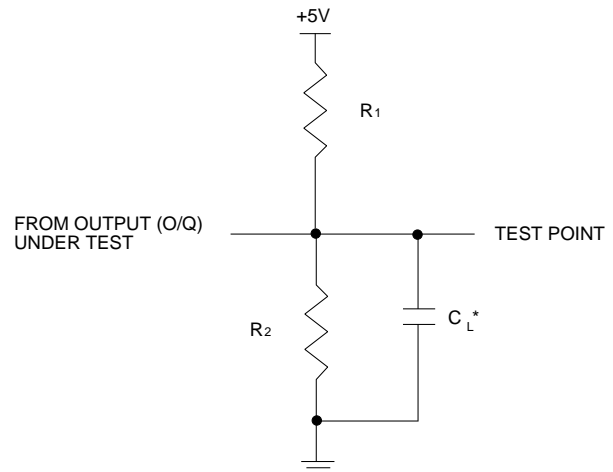
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition	R ₁	R ₂	C _L
A	300Ω	390Ω	50pF
B	Active High	∞	390Ω
	Active Low	300Ω	390Ω
C	Active High	∞	5pF
	Active Low	300Ω	390Ω



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

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Electronic Signature

An electronic signature word is provided in every GAL20V8Z/ZD device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter checksum.

Security Cell

A security cell is provided in the GAL20V8Z/ZD devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by re-programming the device, so the original configuration can never be examined once this cell is programmed. The electronic signature data is always available to the user, regardless of the state of this security cell.

Device Programming

GAL devices are programmed using a Lattice Semiconductor-approved Logic Programmer, available from a number of manufacturers (see the GAL Development Tools Section of the Data Book). Complete programming of the device takes only a few seconds. Erasing of the device is transparent to the user, and is done automatically as part of the programming cycle.

Input Transition Detection (ITD)

The GAL20V8Z relies on its internal input detection circuitry to put the device in power down mode. If there is no input transition for the specified period of time, the device will go into the power down state. Any valid input transition will put the device back into active state. The first rising clock transition from power-down state only acts as a wake up signal into the device and will not clock the data input through to the output (refer to standby power timing waveform for more detail). Any input pulse widths greater than 5ns at input voltage level of 1.5V will be detected as input transition. The device will not detect any input pulse widths less than 1ns measured at input voltage level of 1.5V as input transition.

Dedicated Power-Down Pin

The GAL20V8ZD uses pin 4 (pin 5 on PLCC) as the dedicated power-down signal to put the device in power-down state. DPP is an active high signal where logic high driven on this signal puts the device into power-down state. Input pin 4 (5) cannot be used as a functional input on this device.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

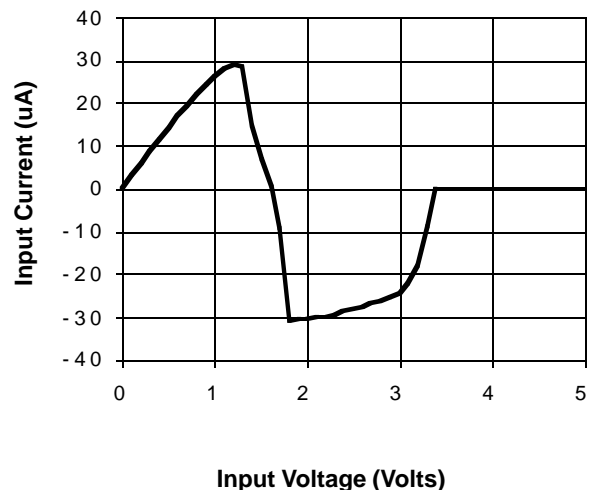
The GAL20V8Z/ZD devices includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing text vectors perform output register preload automatically.

Input Buffers

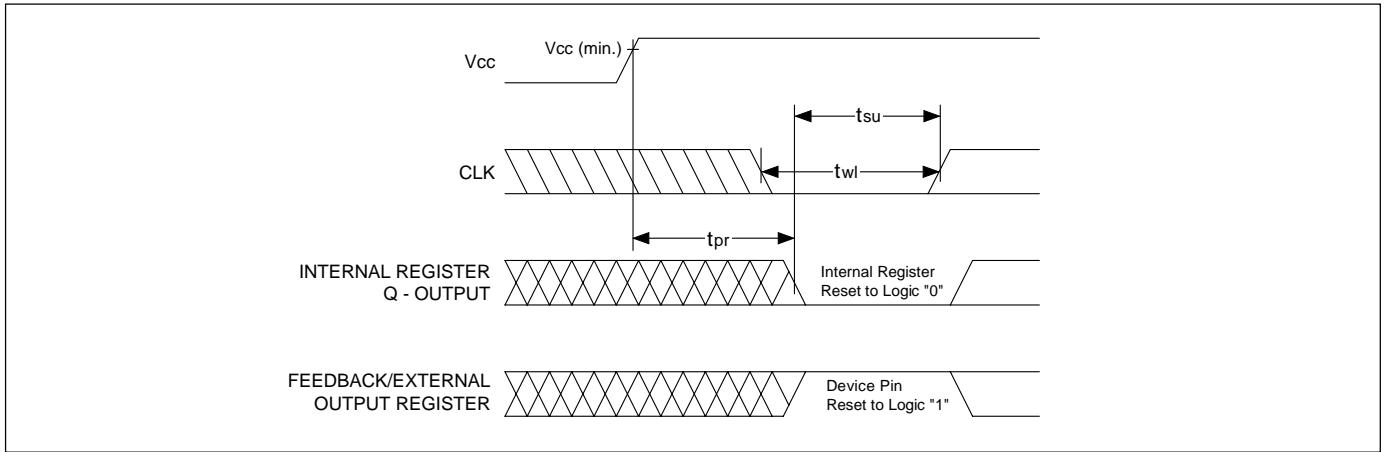
GAL20V8Z/ZD devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL20V8Z/ZD input buffers have latches within the buffers. As a result, when the device goes into standby mode the inputs will be latched to its values prior to standby. In order to overcome the input latches, they will have to be driven by an external source. Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC} , or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

Typical Input Characteristic



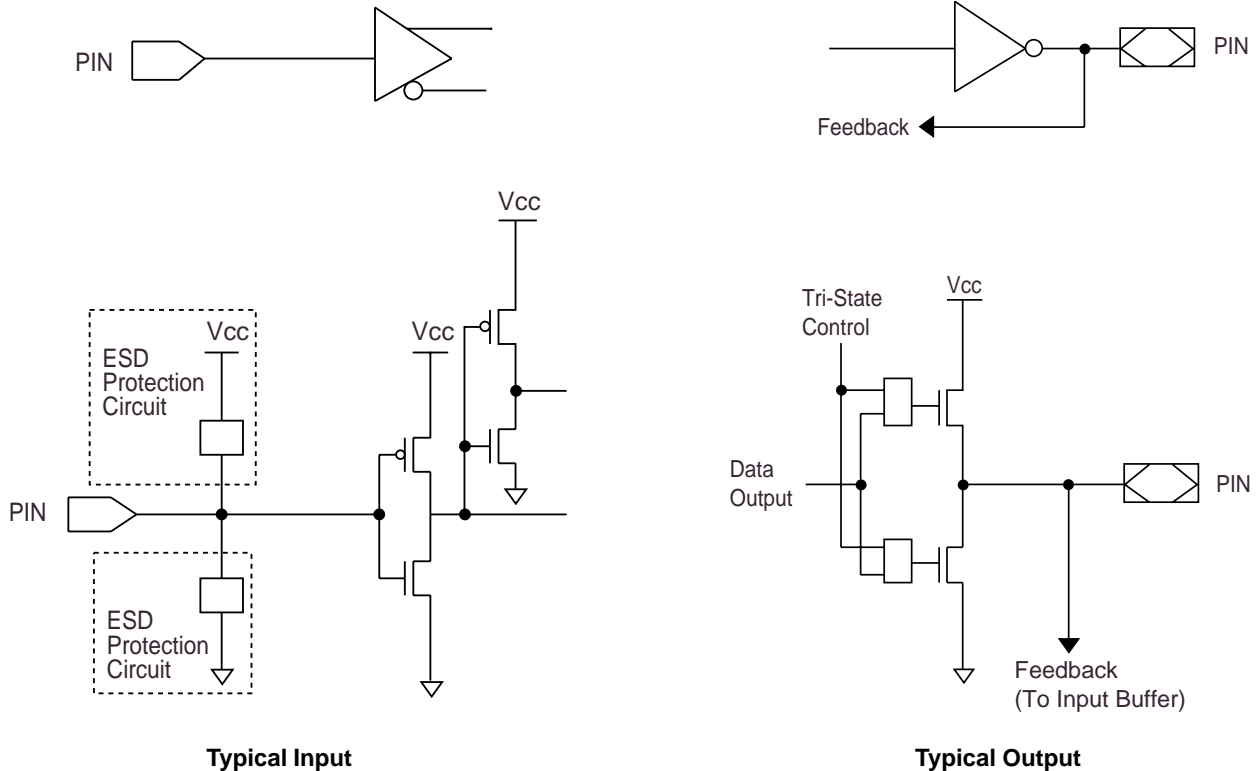
Power-Up Reset



Circuitry within the GAL20V8Z/ZD provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{pr}, 1μs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown below. Because of the

asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20V8Z/ZD. First, the V_{cc} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of t_{pr} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics

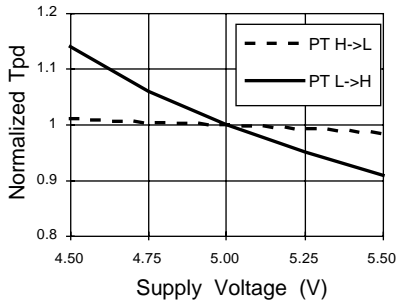


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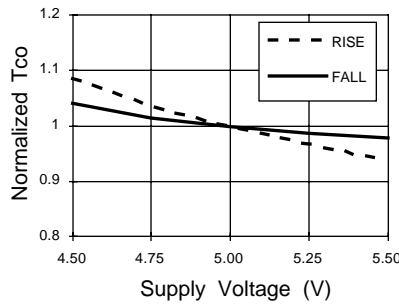
Typical AC and DC Characteristics

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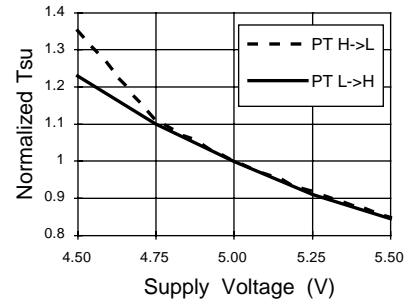
Normalized Tpd vs Vcc



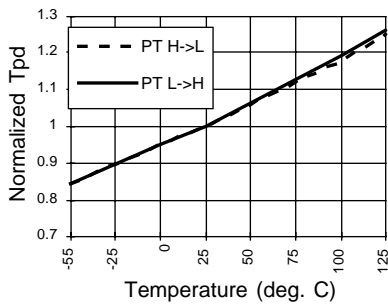
Normalized Tco vs Vcc



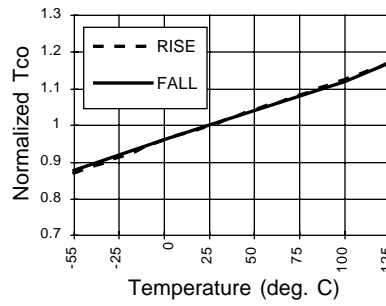
Normalized Tsu vs Vcc



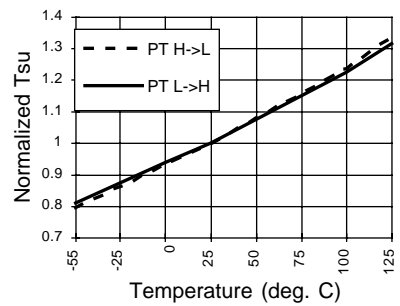
Normalized Tpd vs Temp



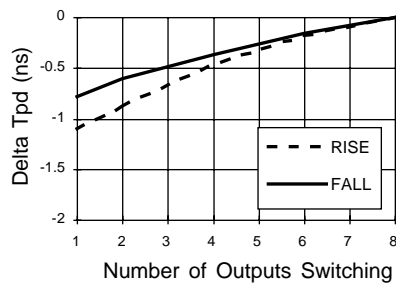
Normalized Tco vs Temp



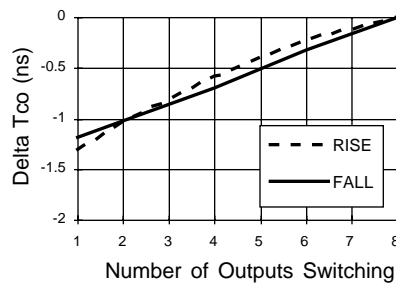
Normalized Tsu vs Temp



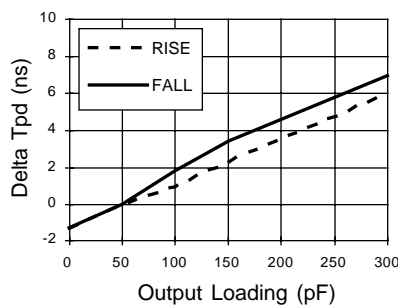
Delta Tpd vs # of Outputs Switching



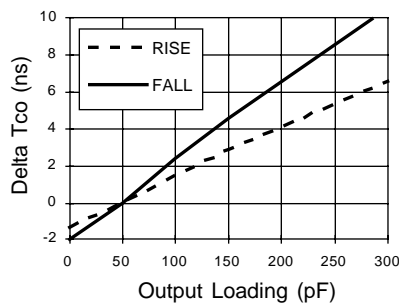
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

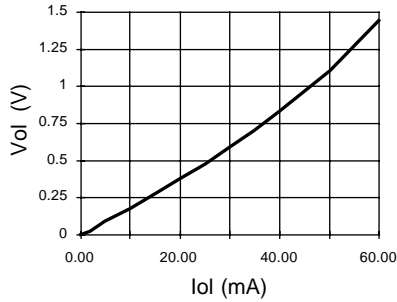


Delta Tco vs Output Loading

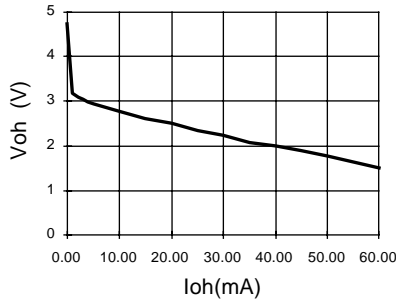


Typical AC and DC Characteristics

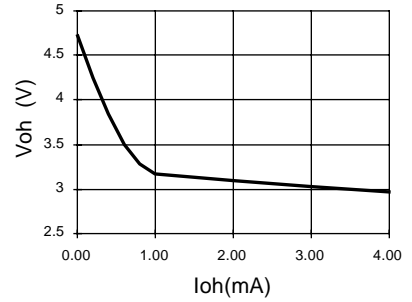
Vol vs Iol



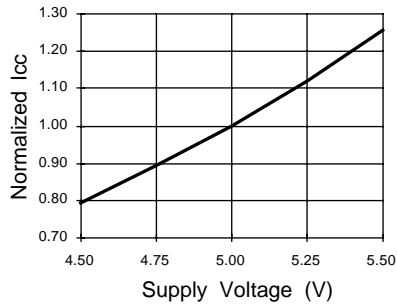
Voh vs Ioh



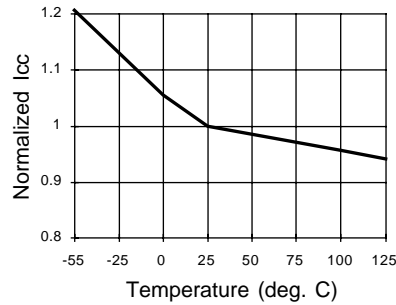
Voh vs Ioh



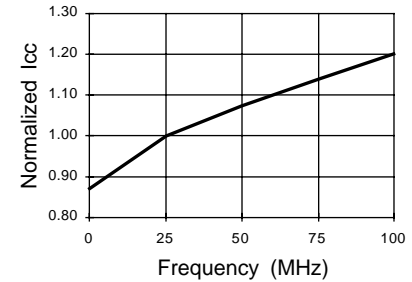
Normalized Icc vs Vcc



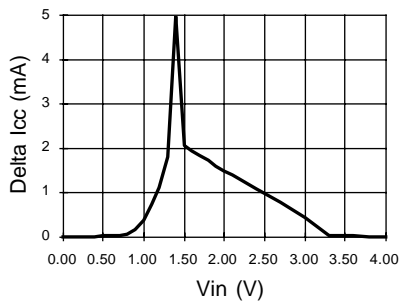
Normalized Icc vs Temp



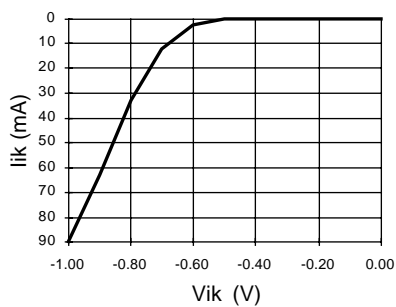
Normalized Icc vs Freq. (DPP & ITD > 10MHz)



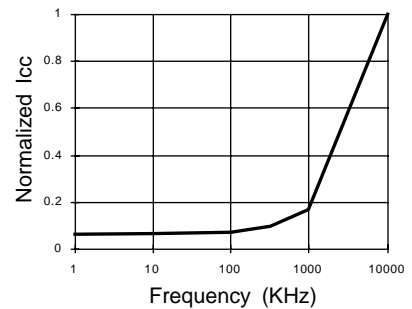
Delta Icc vs Vin (1 input)



Input Clamp (Vik)



Normalized Icc vs Freq. (ITD)



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