



Lattice
Semiconductor
Corporation

ispCLOCK-Manager Development Kit

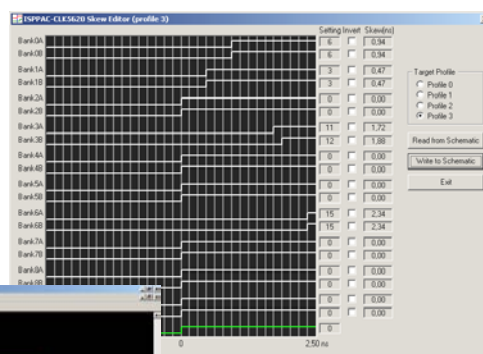
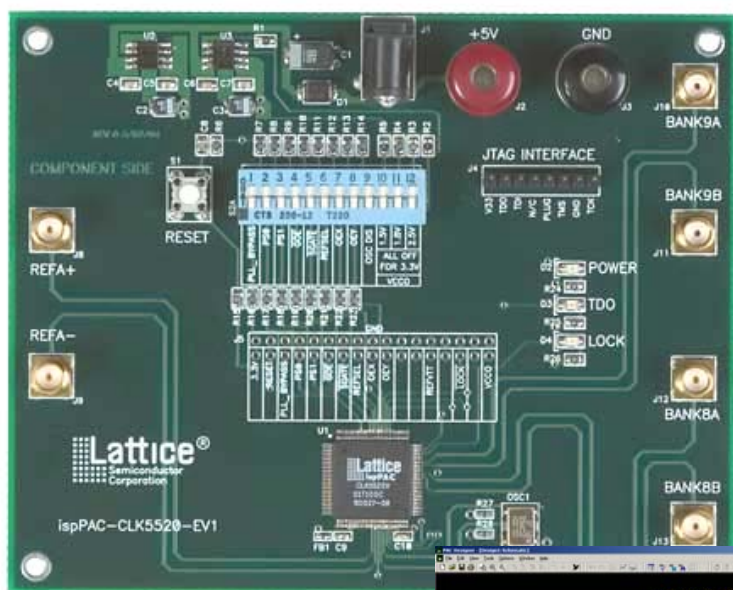
Evaluation-Board for Lattice ispCLOCK Family with ispPAC-CLK5520 Device and Download-Cable

ispCLOCK Manager Key Features

- JTAG Programming Interface and Boundary Scan Test Support
- 3.3V (ispClock5500V) or 2.5V (ispClock5500B) Operation
- Four On-chip Profiles for Easy Configuration Switching
- 48-pin/10-output (5510) and 100-pin/20-output (5520) Options

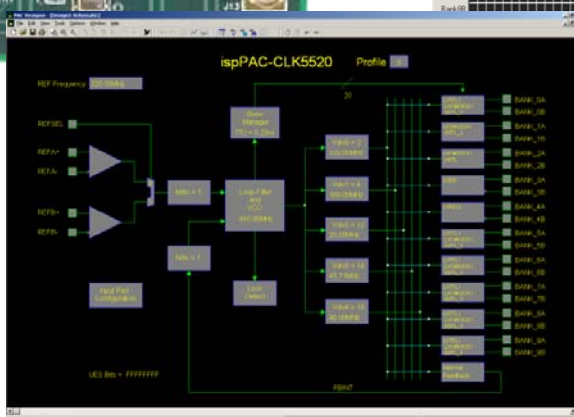
Programmable High Performance PLL Core

- Generate up to five output frequencies
- Low cycle to cycle jitter (70ps peak-peak max.)
- Programmable loop filter response
- Programmable lock detection Programmable Input and Output Section
- 10-320MHz input and output frequency range
- Interface directly to LVTTTL, LVCMOS, HSTL, SSTL, LVPECL, LVDS with up to 20 clock outputs
- Low pin-to-pin skew (<50ps)
- Programmable input and output impedance from 40Ω to 70Ω in 5Ω steps
- Programmable skew using 16 precision skew steps
- Programmable slew rate



Design Environment PAC-Designer

- Easy-to-use GUI
- intuitive pull-down menus
- Skew Editor
- Frequency Calculator



nur € 275,-

Angebot freibleibend

Hiermit bestelle ich zu den allgemeinen Geschäftsbedingungen der MSC Vertriebs GmbH:

ispClock Development Kit (PAC-SYSTEMCLK5520) für € 275,- netto

Firma _____

Name _____

Tel/Fax _____

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Ort, Datum _____

Unterschrift _____

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