

Lattice Diamond

Leading-edge design and implementation tools optimized for Lattice FPGA architectures.

Lattice Diamond™ design software offers leading-edge design and implementation tools optimized for cost-sensitive, low-power Lattice FPGA architectures. Diamond is the next generation replacement for ispLEVER® featuring design exploration, ease of use, improved design flow, and numerous other enhancements. This combination of new and enhanced features allows users to complete designs faster, easier, and with better results than ever before.

Diamond software is available as a download from the Lattice website for both Windows and Linux. Once downloaded and installed, it can be used with either a free license or a subscription license.

Diamond Software Free License

A free license can be requested from the Lattice website. This license provides immediate access to many popular Lattice devices such as MachXO™, LatticeXP2™ and LatticeECP2™ at no cost. It also includes Synopsys® Synplify Pro™ for Lattice synthesis and Aldec® Active-HDL™ Lattice Web Edition II simulation software.*

Diamond Software Subscription License

A subscription license can be purchased which adds support for all Lattice FPGAs including the latest LatticeECP3™ devices. It includes Synopsys Synplify Pro for Lattice synthesis and Aldec Active-HDL Lattice Edition II mixed language simulator* for increased capacity and performance. The subscription license also enables both the new Diamond software and existing ispLEVER software from a single license.

✓ **SUPERIOR DESIGN EXPLORATION**

✓ **EASE OF USE**

✓ **IMPROVED DESIGN FLOW**



Key Features and Benefits

- **Design Exploration Features**
 - Explore design alternatives with Implementations & Strategies
 - Run Manager for utilizing multi-core processors
 - Integrated HDL code checking
- **Ease-of-Use Features**
 - Advanced next generation user interface
 - Centralized reports and messaging
 - Extensive cross-probing support
 - Manage multiple preference, debug, timing analyzer, and power calculator files within file list view
 - ECO Editor for specific physical netlist-level changes
 - Programmer for rapid re-programming
- **Improved Design Flow**
 - New Timing Analyzer view allows re-timing without re-implementing design
 - Simulation Wizard for exporting designs
 - Extensive Tcl scripting dictionaries
- **Additional Software Included with Diamond**
 - LatticeMico32™ system integration for embedded microprocessor applications
 - ispVM™ System software provides complete programming support
 - EPIC full-featured physical netlist-level editor

*Aldec Lattice Web Edition II simulation software is only available for Windows nodelocked licenses. Aldec Lattice Edition II simulator is only available for Windows. Floating licenses require the additional ALDEC-USBKEY product.

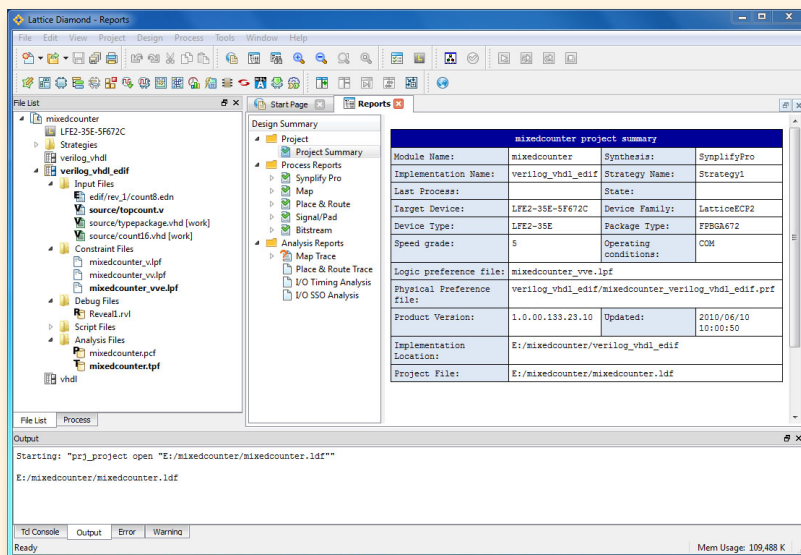
Diamond Key New Features

Design Exploration

PROJECTS / IMPLEMENTATIONS / STRATEGIES

Diamond allows more robust projects and offers new capabilities for improved design exploration. Key features include:

- Mixing of Verilog, VHDL, EDIF, and schematic sources
- Implementations allow multiple versions of a design within a single project for easy design exploration
- Strategies allow implementation “recipes” to be applied to any implementation within a project or shared between projects
- Manage and choose files for constraints, timing analysis, power calculation, and hardware debug
- Use Run Manager view for parallel processing of multiple implementations to explore design alternatives for the best results



Diamond Environment for Design Exploration

HDL CODE CHECKING

Save time by analyzing your design prior to synthesis with Diamond's integrated HDL code checking capability. Click “Generate Hierarchy” and HDL Diagram,

Hierarchy, Module, and Dictionary views become available to help in analyzing your design. Additionally, a number of BKM (Best Known Methods) rule checks can be run against your design.

Ease of Use

GUI FOR A NEW GENERATION OF TOOLS

The Diamond user interface combines leading edge features and customization while offering improved ease of use. All tools open in “Views” integrated into a common user interface. Once the operation for a single tool is learned, this knowledge can be applied to other tools.

KEY GUI ELEMENTS

- Common menu and button locations for all views
- Three user interface sections for tools, projects, and output
- Start Page – open projects, import ispLEVER projects, online help, software updates
- Report View – Centralized location for all reports from implementation tools

SPEED COMMON FUNCTIONS WITH ECO EDITOR & PROGRAMMER

- ECO Editor provides quick access to commonly used physical netlist editing functions without using the EPIC full editor
- Programmer allows fast reprogramming of FPGAs once the hardware configuration has been set up with ispVM System software

Improved Design Flow

FAST, EASY TIMING ANALYSIS

Timing Analysis view offers an easy-to-use graphical environment for navigating timing information.

- Click on a constraint and see the timing paths, detailed paths, and path schematic views instantly
- Easy visual cues provide instant design feedback.
- Rapidly updated analysis when timing constraints are changed

power calculation, and hardware debug.

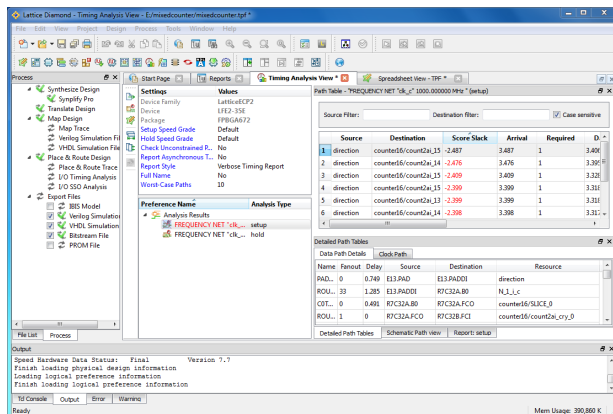
- In addition to the Tcl console in the Diamond environment, a separate Tcl console application allows running scripts independently.

EASY EXPORT TO SIMULATORS

The new Simulation Wizard guides you through all the necessary steps to get your design to Aldec or ModelSim simulators in the format you choose.

SCRIPTING WITH Tcl

- Tcl command dictionaries for projects, netlists, HDL code checking,

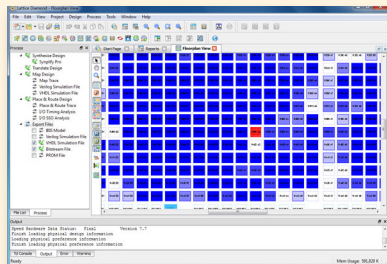


Diamond Timing Analysis View

Improved Features

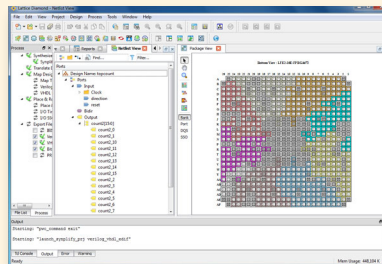
| Feature | Description |
|--|--|
| Power Calculator | <ul style="list-style-type: none"> • Uses highly accurate data models and a data-driven power model • Provides power estimation and calculation results, graphical power displays, and reports |
| Spreadsheet View | <ul style="list-style-type: none"> • Enter and view design constraints (pin assignments, clock resource usage, global preferences, timing preferences, and more) • Works with File List view to manage multiple constraints files |
| Package View | <ul style="list-style-type: none"> • Easy graphical assignment of signals to pins • Graphical representation of SSO noise analysis |
| Floorplanning Tasks | <ul style="list-style-type: none"> • Floorplan View – View design placement and edit placement constraints • Physical View – Detailed view of physical routing of paths to understand timing issues • Netlist View – Browse design ports, instances, and nets. Drag and drop into other views to set constraints. • NCD View – Detailed usage information of physical components • Device View – View device resources and edit placement constraints |
| Reveal Hardware Debugger | <ul style="list-style-type: none"> • Easy insertion of embedded logic analyzer debug hardware for real-time analysis • New streamlined Reveal Analyzer module with multiple cursors and rubber banding for measuring events in the waveform display |
| IPexpress | <ul style="list-style-type: none"> • The interface to the catalog of modules and intellectual property (IP) optimized for Lattice devices • Import a reference file for each module or IP to easily incorporate the changes resulting from regenerating a module or IP |
| Simulink Blockset | <ul style="list-style-type: none"> • Provides DSP blocks that can be used to build DSP solutions within the MATLAB/Simulink environment • These solutions can be exported in HDL optimized for Lattice FPGA architectures |
| ispVM System Software | <ul style="list-style-type: none"> • Comprehensive device programming manager • Efficiently programs Lattice devices using JEDEC and bitstream files generated by Lattice software |
| Synopsys Synplify Pro for Lattice Synthesis | <ul style="list-style-type: none"> • Automatically produce an RTL schematic of your design • Cross-probe with RTL source code • Mixed VHDL and Verilog synthesis support • Compile points • Automatic re-timing (balancing registers across combinatorial logic) • Automatic gated-clock and generated-clock conversion for efficient implementation of RTL written for an ASIC into an FPGA |
| Aldec Active-HDL Simulation | <ul style="list-style-type: none"> • Mixed language simulation of VHDL and Verilog (Aldec Active-HDL Lattice Edition II only) • Language Assistant • Code Execution Tracing • Advanced Breakpoint Management • Memory Viewing |

FLOORPLAN VIEW



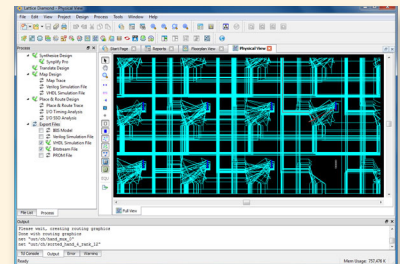
Floorplan View provides the ability to view design placement and edit placement constraints.

PACKAGE VIEW



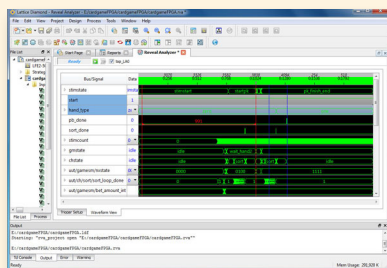
Easy graphical assignment of signals to pins and a graphical representation of SSO noise analysis.

PHYSICAL VIEW



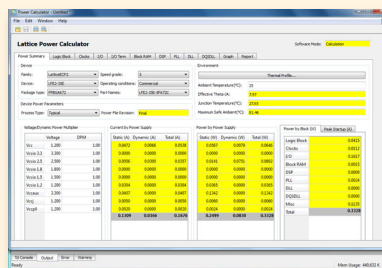
A detailed, read-only view of the physical routing of paths for a more detailed understanding of timing issues.

REVEAL HARDWARE DEBUGGER



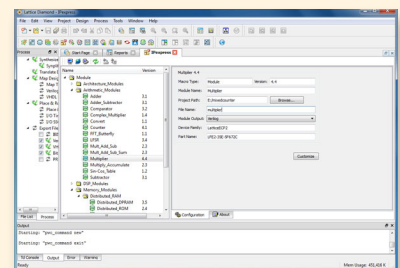
The Reveal Hardware Debugger uses a signal-centric model that allows easy insertion of embedded logic analyzer debug hardware for real-time analysis.

POWER CALCULATOR



The data driven approach of Power Calculator provides very accurate results for both power estimation and calculation.

IPexpress



An interface to the Lattice catalog of modules and IP optimized for Lattice devices.

Diamond Software Configuration Summary

| | Lattice Diamond Free License | Lattice Diamond Subscription License |
|---|-----------------------------------|---|
| Lattice Device Support | | |
| LatticeECP3, LatticeECP2M/S, LatticeSC™, LatticeSCM™, LatticeECP2/S | | ✓ |
| MachXO™, LatticeECP™, LatticeEC™, LatticeXP™, LatticeXP2, LatticeECP2 | ✓ | ✓ |
| Key Software Features | | |
| Complete Diamond Software Environment | ✓ | ✓ |
| Third-Party Software | | |
| Synopsys Synplify Pro | ✓ | ✓ |
| Aldec Active-HDL Lattice Edition II | | ✓ |
| Aldec Active-HDL Lattice Web Edition II | ✓ | |
| Operating Systems | | |
| Windows – XP, Vista (32-bit), 7 (32-bit app, both 32 & 64-bit OS) | ✓ | ✓ |
| Linux – RHEL 4, 5.3; Novell SUSE 10SP1, 11 | ✓ | ✓ |
| Licensing and Ordering | | |
| License Terms | 1 Year Nodelocked Only, Renewable | 1 Year Subscription, Nodelocked or Floating |
| Part Number | N/A | DIAMOND-E-12M |

Related Products

| Product | Description | Ordering Part Number |
|---|---|----------------------|
| Diamond DVD Media Backup | Diamond software on DVD media. This is media only and does not include a Diamond license. | DIAMOND-I-12M |
| USB Key for Aldec Simulation Floating License | Required to use Aldec simulation with a floating license. Existing USB keys from ispLEVER can also be used with Diamond software. | ALDEC-USBKEY |
| Download Cable (1.2V to 5V USB Programming Cable) | USB programming cable | HW-USBN-2A |
| Download Cable (1.8V to 5V Parallel Port Programming Cable) | Parallel port programming cable | HW-DLN-3C |

Applications Support

1-800-LATTICE (528-8423)
 (503) 268-8001
 techsupport@latticesemi.com
 www.latticesemi.com

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June 2010
 Order #: I0207