

# LatticeECP3 IO Protocol Evaluation Board User's Guide

## Introduction

The LatticeECP3 IO Protocol Evaluation Board provides a convenient platform to evaluate, test and debug user designs and IP cores targeted for the LatticeECP3-95 FPGA. The board features a LatticeECP3-95 FPGA in the 1152 fpBGA package. The LatticeECP3 I/Os are connected to a rich variety of both generic and application-specific interfaces described later in this document.

**Important:** This document (including the schematics in the appendix) describes LatticeECP3 IO Protocol Evaluation Boards marked as Rev A. This marking can be seen on the silkscreen of the printed circuit board, under the Lattice Semiconductor logo.

The LatticeECP3 is a third-generation device utilizing reconfigurable SRAM logic technology optimized to deliver high performance features such as an enhanced DSP architecture, high speed SERDES and high speed source synchronous interfaces in an economical FPGA fabric. The Lattice ECP3 devices also provide popular building blocks such as LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), and advanced configuration support, including encryption, multi-boot capabilities and TransFR field upgrade features. The LatticeECP3 SERDES dedicated PCS functions, high jitter tolerance and low transmit jitter allow the SERDES plus PCS blocks to be configured to support an array of popular data protocols including PCI Express, SMPTE, Ethernet (XAUI, GbE, and SGMII), SATA I/II, OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make the SERDES suitable for transmission and reception over various forms of media.

For a full description of the LatticeECP3 FPGA, see the Lattice web site for datasheets, applications notes, technology summaries and more:

<http://www.latticesemi.com>

Some common uses for the LatticeECP3 IO Protocol Evaluation board include:

- Applications requiring large DDR3 memory width and depth
- High-speed parallel ADC/DAC Interface
- SERDES data transfer with external devices
- 1000base-T PHY/RJ45 networking
- A single-board computer system
- A platform for evaluating the Input/Output (I/O) characteristics of the FPGA
- A platform for evaluation and development with Lattice IP cores

## Features

Key features of the LatticeECP3 IO Protocol Evaluation Board include:

- SPI Serial Flash device included for low-cost, non-volatile configuration storage
- Two 64 bit DDR3 DIMM module sockets
- Tri-speed (10/100/1000 Mbit) Ethernet PHY with RJ-45 (includes 12 core magnetics)
- USB 2.0 transceiver
- Built in USB 2.0 download to LatticeECP3 and ispPAC bitstreams.
- High-speed HMZD connector with 80 differential pair connections and selectable VTT voltage
- 8-pin DIP switch
- Discrete LEDs and 7-segment LED

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- LCD module connector
- Prototyping areas with 96 IO pins
- 1 selectable user I/O bank voltage with access to 2 VREF test points
- Logic analyzer probe connection
- 2 pairs of high speed differential IO using SMA connectors
- 5 crystal oscillators
- 2 selectable high speed differential external clock sources with PLL feed back inputs
- 4 channels (1 quad) of differential SERDES (TX and RX) using SMA connectors
- 1 high current high speed IO connection using an SMA connector
- 3.3V, 2.5V, 1.5V, 1.2V and DDR3 voltages are generated from a single 12V power source
- 3 fixed or adjustable DDR3 reference voltages
- Power Manager ispPAC-POWR1220AT8 chip for monitoring input power and regulator outputs to be within nominal tolerance with programmable trims
- IspVM System™ programming support
- Multi-board JTAG programming capability and sysCONFIG connector

### General Description

The heart of the board is the LatticeECP3 FPGA. The board also provides several different interconnections and support devices that permit it to be used for a variety of purposes. The DDR3 sockets, and Tri-speed Ethernet PHY are useful for applications using Lattice IP cores.

A number of connectors are useful for general purpose LatticeECP3 I/O capability. These include the SMA connectors, USB, PHY, LCD connector, and the various generic prototype access points.

Other features on the board help in evaluating the capabilities and performance of the LatticeECP3. The 4 channels of SERDES PCS allow straight forward, flexible, high data rate connections to external devices. The various SMA connectors permit the evaluation of high-speed differential signals, and protocols. The HMZD connector provides a wide parallel data path for up to 80 high speed differential signal connections with easy bench top board to board plug in expansion with low signal skew. The SPI memory showcases the failsafe capabilities of the LatticeECP3.

The board also acts as a showcase for the ispPAC-POWR1220 power manager. The ispPAC-POWR1220 is a programmable device useful for safely managing the power supply system on the board. It can be programmed to sequence, monitor, and adjust the voltages on the LatticeECP3 Advanced board.

Additional resources for the LatticeECP3 Advanced Evaluation Board, such as updates to this document, sample programs and links to demos can be found on the Lattice web site. Go to [www.latticesemi.com/boards](http://www.latticesemi.com/boards), and navigate to the appropriate page for this board.

### Initial Setup and Handling

The following is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

**CAUTION:** *The devices on the board can be damaged by improper handling.*

The devices on the evaluation board contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the "Human

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Body Model" specification for an example of ESD characterization requirements). Even so, the devices are static sensitive to conditions that exceed their designed in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications require can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation board when it is removed from the static shielding bag. If you will not be using the board for a while, it's best to put it back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the board when it is not in use.

When reaching for the board, it is recommended that you first touch the outside threaded portion of one of the gold SMA connectors. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

**CAUTION:** *to minimize the possibility of ESD damage, the first and last electrical connection to the board, should be always be from test equipment chassis ground to GND on the board (left side post of TB1 labeled GND on the board).*

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the GND on the board. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged, should be the chassis GND connection to the evaluation board GND. If you have a signal source that is floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board while it's not in a static shielding bag, please keep one finger on the threaded portion of one of the gold SMA connectors. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back in it.

## Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 8 inches by 8 inches. The environmental specifications are as follows:

- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C
- Humidity: <95% without condensation
- 12v +/-10% DC (20 watts max)

## Functional Description



Figure 1: LatticeECP3 IO Protocol Evaluation Board

### LatticeECP3 Device

This board features a LatticeECP3 FPGA with a 1.2VDC core in a 1152-ball fpBGA package. The default device is the LatticeECP3-95. **Any other LatticeECP3 density in this package can be accommodated.** A complete description of this device can be found on the Lattice web site at: <http://www.latticesemi.com>

### Power Setup

The board is supplied by a single 12V +/-10% DC power supply while on-board regulators will provide the necessary supply voltages: 3.3V, 2.5V, 1.5V, 1.2V, and 0.75V. The DC power may be

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applied through the power jack at J56 using an AC adapter with 12V +/-10% DC output range. The requirements for the J56 power jack are listed in Table 1.

**Table 1. Power Jack J56 Specifications**

Polarity	Positive Center
Inside Diameter	0.1" (2.5mm)
Outside Diameter	0.218" (5.5mm)
Current Capacity	Up to 1.7A

Other than using the AC adapter, the DC power may also be applied using a workbench power supply through the terminal block at TB1 (12\_0VIN, GND). The workbench power supply voltage has to be between 10.8v and 13.2v for normal operation of switching power supply modules U14 and U15. If the 12v power source is outside the normal voltage range, the row of LEDs next to the ispPAC (U17) will all blink if the topmost lever of SW1 is up. The 12v input voltage out of range LED blink warning can be disabled by pushing the topmost lever of SW1 down. It is recommended that if you are using a power source that initiates the LED blink warning, that you first investigate the source of the out of tolerance voltage condition and correct it rather than disable the warning. For example, some small wall mount power supplies produce 14v or more while under lightly loaded conditions, if they produce too high of an input voltage, the 12v switching regulators could be damaged.

Power may also be supplied directly for each individual supply rail using test point connections. To enable this mode of operation, the appropriate fuses must be removed and the topmost lever of SW1 should be pushed down. All power sources must be regulated to the specifications in Table 2.

**Table 2. Individual Control of Supplies**

Supply	Test Points	Fuse	Requirement
3.3V	PP5	F2 (5A)	+/- 5%
2.5V	PP8	F6 (5A)	+/- 5%
1.5V	PP7	F5 (5A)	+/- 5%
1.2V	PP9	F4 (5A)	+/- 5%
VCC_CORE	PP6	F3 (5A)	+/- 5%

The reference voltages for the DDR3 module sockets and LatticeECP3 can be set to a regulated 0.75v source by adding jumpers to J15, J16 and J19. With no jumpers on J15, J16 or J19, the DDR3 reference voltages can be individually set to adjustable voltages using the potentiometers R7, R8 and R12 to provide 0.75v +/- 0.25v adjustment range.

### Power Voltage Sequencing and Monitoring

A Lattice's ispPAC® Power Manager II device, ispPAC-POWR1220AT8, is used for sequencing and monitoring various voltages on the board. The recommended power supply sequence for the ECP3 device is VCCAUX, VCCIO, VCC, and then VCCA. Given the voltage connections made on the evaluation board, the recommended power supply sequence becomes: 3.3v, 2.5v/1.5v, VCC\_CORE, and then 1.2v. When power is first applied, the PAC outputs are tri-stated, so the transistors Q19, Q20, Q21, Q22 and Q23 are on, which disables the voltage regulators. The ispPAC device is programmed to wait specified time delays to sequences the supplies in the

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specified order by selectively waiting to turn off those transistors which then enables the voltage regulators in the programmed sequence.

There are ten “Power Good” LEDs used to indicate the status of the monitoring voltages. If a monitored voltage is not in the normal voltage range, the corresponding power good LED will be OFF, otherwise the LED will stay ON. Table 3 shows the ten monitored voltages and the corresponding LEDs.

**Table 3. Individual Monitoring of 12 Power Voltages**

Voltage	LED	Monitoring Voltage Range
1_2V	D27	1.2V +/- 5%
VCC_CORE	D26	1.2V +5%, 1.0V – 5%
3_3V	D25	3.3V +/- 5%
2_5V	D24	2.5V +/- 5%
1_5V	D23	1.5V +/- 5%
DDR3_VDD	D22	1.5V +/- 5%
DDR3_VTT	D21	0.75V +/- 5%
DDR3_VREF	D20	0.75V +/- 5%
5_0V	D19	5.0V +/- 5%
VCCIO_1	D18	3.3v +5%, 1.2V – 5%
12_0V, 12_0VIN	ALL	12.0V +/- 10%

For the 12\_0V and 12\_0VIN supply voltage, all LEDs will indicate normally when the input power is 12.0v +/-10%. When the 12v input voltage is outside the normal range, all LEDs above will blink to warn that the 12v switching regulator modules (U14 and U15) are outside their normal operation range. As discussed above, the LED blink warning can be disabled by pushing down the topmost lever of SW1.

### Power Voltage Adjustment and Control

The Lattice's ispPAC® Power Manager II device, ispPAC-POWR1220AT8, can also adjust the power supply voltages: 3\_3V, 2\_5V, 1\_5V, 1\_2V, VCC\_CORE, and DDR3\_VDD by +/- several percent from the nominal value using 6 of the built in DAC trim outputs TRIM[1..8]. Additionally the 3\_3V supply can be enabled or disabled with the HVOUT1 output from the PAC device while the J49 jumper is removed.

### LatticeECP3 I/O Bank Voltage Setting

The jumper listed in Table 4 allows the user to select the bank 1 VCCIO voltage applied to the LatticeECP3 device. All other bank VCCIO voltages are hard wired to their respective voltages. Certain restrictions for VCCIO1 apply depending on which features of the board are being used.

**Table 4. Vccio Selection Jumper**

SysIO Bank	Jumper	Jumper on pins
1	J41	1-3 -> 3.3V 2-4 -> 2.5V 3-5 -> 1.5V 4-6 -> 1.2V None -> External

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Depending on the optional devices installed, some sysIO banks may have restrictions. For J41 only select one bank voltage position at the jumper. For example, attaching more than one jumper to J41's 6 square pins could short supplies. You can also remove the jumper on J41 and apply an external voltage to pins 3 and 4 of J41. When applying an external voltage to J41, do not exceed the LatticeECP3 datasheet specified absolute maximum rating for Output Supply Voltage VCCIO range of -0.5v to +3.75v, or damage to the device may occur.

**Table 5. sysIO Bank Considerations**

Bank	Setting
1	Selectable. LCD may require 3.3v

The following tables detail the various I/O standards supported by the LatticeECP3 sysIO structures. More information can be found in the *LatticeECP3 SysIO Usage Guide Technical Note (TN1136)*:

Note (TN1136):

<http://www.latticesemi.com/documents/TN1136.pdf>

**Table 6. Mixed Voltage I/O Support**

V <sub>CCIO</sub>	Input sysIO Standards					Output sysIO Standards				
	1.2V	1.5V	1.8V	2.5V	3.3V	1.2V	1.5V	1.8V	2.5V	3.3V
1.2V	Yes			Yes	Yes	Yes				
1.5V	Yes	Yes		Yes	Yes		Yes			
1.8V	Yes		Yes	Yes	Yes			Yes		
2.5V	Yes			Yes	Yes				Yes	
3.3V	Yes			Yes	Yes					Yes

For example, if VCCIO is 3.3V then signals from devices powered by 1.2V, 2.5V, or 3.3V can be input and the thresholds will be correct, assuming the user has selected the desired input level using ispLEVER<sup>®</sup> software. Output levels are tied directly to VCCIO.

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**Table 7. sysIO Standards Supported per Bank (needs latest table)**

1. These differential standards are implemented by using complementary LVCMOS drivers and external resistors.

Description	Top Side, Banks 0-1	Right Side, Banks 2-3	Bottom Side, Banks 4-5	Left Side, Banks 6-7
Types of I/O Buffers	Single-ended	Single-ended and Differential	Single-ended	Single-ended and Differential
Output standards supported	LVTTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12  SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II  HSTL15 Class I HSTL18_I, II  SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II  HSTL15D Class I HSTL18D Class I, II  PCI33 LVDS25E <sup>1</sup> LVPECL <sup>1</sup> BLVDS <sup>1</sup> RSDS <sup>1</sup>	LVTTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12  SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II  HSTL15 Class I HSTL18 Class I, II  SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II  HSTL15D Class I, II HSTL18D Class I, II  PCI33 LVDS LVDS25E <sup>1</sup> LVPECL <sup>1</sup> BLVDS <sup>1</sup> RSDS <sup>1</sup>	LVTTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12  SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II  HSTL15 Class I HSTL18 Class I, II  SSTL18D Class I, II SSTL25D Class I, II, SSTL33D Class I, II  HSTL15D Class I HSTL18D Class I, II  PCI33 LVDS25E <sup>1</sup> LVPECL <sup>1</sup> BLVDS <sup>1</sup> RSDS <sup>1</sup>	LVTTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12  SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II  HSTL15 Class I, III HSTL18 Class I, II, III  SSTL18D Class I, SSTL25D Class I, II, SSTL33D_I, II  HSTL15D Class I HSTL18D Class I, II  PCI33 LVDS LVDS25E <sup>1</sup> LVPECL <sup>1</sup> BLVDS <sup>1</sup> RSDS <sup>1</sup>
Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Clock Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
PCI Support	PCI33 no clamp	PCI33 no clamp	PCI33 with clamp	PCI33 no clamp
LVDS Output Buffers		LVDS (3.5mA) Buffers <sup>2</sup>		LVDS (3.5mA) Buffers <sup>2</sup>

2. Available on 50% of the I/O's in the Bank.

## Prototype Areas

For general purpose I/O testing or monitoring, numerous test points are provided for direct access. Some test points are grouped together and arranged in a grid pattern according to their associated I/O bank and are labeled with the pin locations on the silkscreen of the board. Most test point IOs are brought out to IDC connectors J32, J54, J55, and J57 with both source and end type termination resistors available for high speed signal transmission over ribbon cables.

## Differential Signal Connections

There are 14 pairs of SMA connectors, and one HMZD connector that provide general purpose high speed differential signal paths to the LatticeECP3. These SMA connectors are provided for SERDES, clocks and general purpose user-definable signals.

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Table 8 details to which I/O pin each SMA connector is wired to.

**Table 8. SMA Connectors**

Location	LatticeECP3 I/O	Polarity	SysIO Bank	Description
J39	A17	P	1	PT74A
J45	B17	N	1	PT74B
J47*	T30	P	2	PR40A
J48*	U30	N	2	PR40B
J6	U5	P	7	PL43E_A/LUM0_GPLL_T_FB_A
J12	U4	N	7	PL43E_B/LUM0_GPLL_T_FB_B
J21	AH15 (from U8)	P	Quad B	PCSB_REFCLKP
J26	AH16 (from U8)	N	Quad B	PCSB_REFCLKN
J33	Y30 (from U8) U6 (from U8)	P	3 7	PR61E_C/RLM1_GPLL_T_IN_A PL43E_C/LUM0_GPLL_T_IN_A
J36	AA29 (from U8) U7 (from U8)	N	3 7	PR61E_D/RLM1_GPLL_T_IN_B PL43E_D/LUM0_GPLL_T_IN_B
J42	AA34	P	3	PR61E_A/RLM1_GPLL_T_FB_A
J50	AA33	N	3	PR61E_B/RLM1_GPLL_T_FB_B
J7	AL17	P	Quad B	PCSB_HDINP0
J13	AK17	N	Quad B	PCSB_HDINN0
J22	AL16	P	Quad B	PCSB_HDINP1
J27	AK16	N	Quad B	PCSB_HDINN1
J34	AP17	P	Quad B	PCSB_HDOUTP0
J37	AN17	N	Quad B	PCSB_HDOUTN0
J43	AP16	P	Quad B	PCSB_HDOUTP1
J51	AN16	N	Quad B	PCSB_HDOUTN1
J8	AL15	P	Quad B	PCSB_HDINP2
J14	AK15	N	Quad B	PCSB_HDINN2
J23	AL14	P	Quad B	PCSB_HDINP3
J28	AK14	N	Quad B	PCSB_HDINN3
J35	AP15	P	Quad B	PCSB_HDOUTP2
J38	AN15	N	Quad B	PCSB_HDOUTN2
J44	AP14	P	Quad B	PCSB_HDOUTP3
J52	AN14	N	Quad B	PCSB_HDOUTN3

\* Note: Requires removal of R65 and installation of C30 and C31.

### HMZD Connector

J58 is a high speed HMZD header with 80 differential signal connections for interfacing to the LatticeECP3 device. IOs connected as LVDS inputs can be terminated to a 1.25v VTT voltage provided by U10 when header J31 pins 1 and 2 are shorted. When pins 2 and 3 of J31 are shorted, the VTT voltage is 0v. The connections for J58 are listed in Table 9 below.

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*Table 9. J58 HMZD Connections*

<b>J58 Pin</b>	<b>LatticeECP3 I/O</b>	<b>Polarity</b>	<b>SysIO Bank</b>	<b>Description</b>
A1	V27	P	3	PR49A*^
B1	V26	N	3	PR49B*
A2	Y26	P	3	PR61A*
B2	Y25	N	3	PR61B*
A3	W27	P	3	PR55A*
B3	W26	N	3	PR55B*
A4	AL30	P	3	PR91A*
B4	AM30	N	3	PR91B*
A5	T29	P	2	PR34A*/VREF1_2
B5	T28	N	2	PR34B*/VREF2_2
A6	N26	P	2	PR19A*
B6	P26	N	2	PR19B*
A7	W30	P	3	PR53A
B7	W29	N	3	PR53B
A8	AB34	P	3	PR62A
B8	AB33	N	3	PR62B
A9	Y34	P	3	PR56A
B9	Y33	N	3	PR56B
A10	R34	P	2	PR32A
B10	R33	N	2	PR32B
C1	AJ31	P	3	PR88A*
D1	AK31	N	3	PR88B*
C2	V29	P	3	PR52A*/VREF1_3
D2	W28	N	3	PR52B*/VREF2_3
C3	U26	P	2	PR43A*/PCLKT2_0
D3	U27	N	2	PR43B*/PCLKC2_0
C4	U28	P	3	PR46A*/PCLKT3_0
D4	V28	N	3	PR46B*/PCLKC3_0
C5	R28	P	2	PR28A*
D5	R27	N	2	PR28B*
C6	AB30	P	3	PR70E_C/RLM2_GPLLT_IN_A
D6	AB29	N	3	PR70E_D/RLM2_GPLLT_IN_B
C7	AN34	P	3	PR80A
D7	AN33	N	3	PR80B
C8	V31	P	3	PR44A
D8	V30	N	3	PR44B
C9	N27	P	2	PR22A*^
D9	N28	N	2	PR22B*
C10	W34	P	3	PR47A
D10	W33	N	3	PR47B
E1	AH33	P	3	PR82A*

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F1	AJ33	N	3	PR82B*
E2	AA25	P	3	PR64A*
F2	AA26	N	3	PR64B*
E3	AM29	P	3	PR97A*
F3	AN29	N	3	PR97B*
E4	AL34	P	3	PR85A*^
F4	AL33	N	3	PR85B*
E5	P28	P	2	PR25A*
F5	P27	N	2	PR25B*
E6	AN32	P	3	PR89A
F6	AM32	N	3	PR89B
E7	AP33	P	3	PR83A
F7	AP32	N	3	PR83B
E8	W32	P	3	PR50A
F8	W31	N	3	PR50B
E9	R31	P	2	PR29A
F9	R30	N	2	PR29B
E10	N30	P	2	PR17A
F10	N29	N	2	PR17B
G1	AJ34	P	3	PR79E_C/RLM3_GPLL_T_IN_A
H1	AK34	N	3	PR79E_D/RLM3_GPLL_T_IN_B
G2	Y28	P	3	PR58A*^
H2	Y27	N	3	PR58B*
G3	V34	P	2	PR43E_C/RUM0_GPLL_T_IN_A
H3	V33	N	2	PR43E_D/RUM0_GPLL_T_IN_B
G4	AP29	P	3	PR94A*^
H4	AP30	N	3	PR94B*
G5	R26	P	2	PR31A*^
H5	R25	N	2	PR31B*
G6	AL32	P	3	PR86A
H6	AK32	N	3	PR86B
G7	Y32	P	3	PR59A
H7	Y31	N	3	PR59B
G8	T26	P	2	PR37A*/RUM0_GDLLT_IN_A
H8	T27	N	2	PR37B*/RUM0_GDLLT_IN_B
G9	T32	P	2	PR35A
H9	T31	N	2	PR35B
G10	N32	P	2	PR20A
H10	N31	N	2	PR20B

**Crystal Oscillators and External Clock Sources**

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Designs loaded into the LatticeECP3 can select from 4 separate clock sources: 2 crystal oscillators, and 2 pairs of differential external clocks applied through SMA connectors. The selection of internal or external clock sources is done with U8, a high speed LVPECL multiplexer (MC100LV100VEL56) using the control signals CLK\_SEL and PCSB\_CLK\_SEL. The multiplexer clock source selections are organized as INT/EXT CLOCK source for the LatticeECP3 general purpose clock and INT/EXT PCSB CLOCK source for the LatticeECP3 SERDES reference clock. The CLK\_SEL signal sourced from the LatticeECP3 pin AA31 controls U8 to select whether the internal or external clock source will drive the general purpose clock input to the LatticeECP3 device. The PCSB\_CLK\_SEL signal sourced from the LatticeECP3 pin AN31 controls U8 to select whether the internal or external PCSB clock source will drive the SERDES reference clock input to the LatticeECP3 device. Tables 10 and 11 detail the clock source selections.

**Table 10. SERDES Clock Source Selection**

U8 Mux0 Input			LatticeECP3 Input Clock			
Source	Description	LatticeECP3	I/O Pin	Bank	Usage	IO_TYPE
J21, J26	EXT PCSB CLK	AN31 = 0	AH15, AH16	SERDES	Reference	CML 50 ohm
Y2	156.25 MHz	AN31 = 1				

**Table 11. General Purpose and DDR3 Clock Source Selection**

U8 Mux1 Input			LatticeECP3 Input Clock			
Source	Description	LatticeECP3	I/O Pin	Bank	Usage	IO_TYPE
J33, J36	EXT CLK	AA31 = 0	Y30, AA29	3	General	LVDS
Y3	100 MHz	AA31 = 1	U6, U7	7	DDR3	SSTL15D

The internal clock sources Y2 and Y3 are crystal oscillators with +/-50ppm accuracy that are individually enabled only while the U8 multiplexer is selecting them. The external clock sources are user supplied through SMA connectors at J21, J26, J33, and J36, after which they are AC coupled and 50 ohm terminated at the inputs of the U8 multiplexer. The external clock sources can be applied either single ended or differentially and should have an amplitude in the range of 0.15v to 1.0v p-p (max, into 50 ohm loads, 1MHz to 1GHz) for U8 to function normally.

Note that if U8 is set to select an external source when no external clock signal is attached, it is possible for residual crosstalk and thermal noise to be amplified by the U8 multiplexer, resulting in a relatively random clock signal, or no clock signal, to be output from the U8 multiplexer. Also for best performance, when the U8 multiplexer is selecting an internal clock source, the corresponding external de-selected clock source should be either shut off or disconnected for lowest output clock jitter from the U8 multiplexer.

The U8 multiplexer outputs drive the LatticeECP3 input IO at pins Y30, AA29, U6, U7, AH15 and AH16. The Y30 and AA29 pins are the general purpose differential clock source applied to bank 3. They should be set for LVDS input levels, and they do not require turning on the internal termination at the LatticeECP3. The U6 and U7 signals are used for the DDR3 clock in bank 7. They should be set for SSTL15D input type, and they do not require internal termination at the LatticeECP3. The general purpose clock and DDR3 clock signals are essentially the same clock signal from U8 applied to both banks 3 and 7, but with different IO\_TYPE setting requirements. The AH15 and AH16 signals drive the SERDES reference clock inputs and are terminated as CML 50 ohm loads.

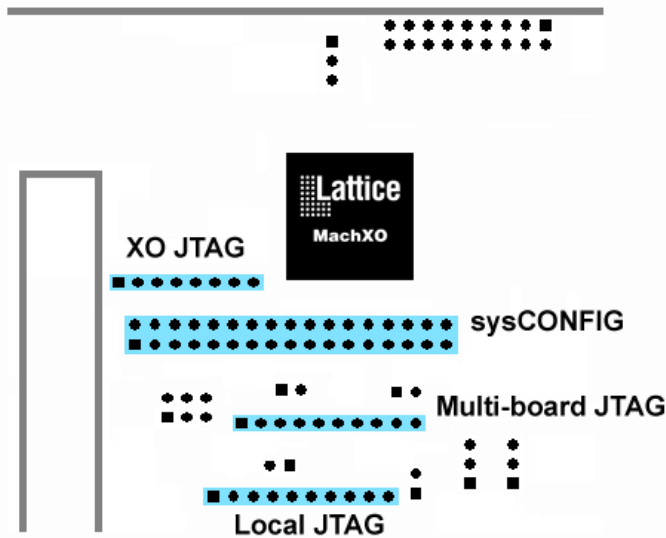
**SPI Serial Flash**

SPI Serial Flash are available in three package styles. The device used on this board is an 8 pin, 64 Mbit, sufficient to store two bitstreams simultaneously in order to support SPI mode.

**Configuration/Programming Headers**

Four programming headers are provided on the evaluation board, providing JTAG access to the LatticeECP3, MachXO, and ispPAC-POWR1220AT8 as well as sysCONFIG port access to the LatticeECP3. See Fig3 and Table 12 for the locations and usage of the programming headers.

**Fig 3. Configuration/Programming Headers**



**Table 12. Programming Header Access to Devices**

Header	Function	Device Programmed
J10	Local JTAG	ECP3, PAC
J11	Multi-board JTAG	External
J4	XO JTAG	MachXO
J5	sysCONFIG	ECP3

The “Local JTAG” 1x10 header J10 is used for programming access to the ECP3 and ispPAC devices. The “XO JTAG” 1x8 header J4 is used to program the MachXO device which is pre-programmed to create an on board USB 2.0 download cable capability that can also program the ECP3. The JTAG ports for the LatticeECP3 and ispPAC-POWR1220AT8 devices can be configured as loop-through connectors to allow for easy daisy chaining of multiple boards connected to the “Multi-board” JTAG 1x10 header J11. With proper jumper selection (see the next section) standard IDC ribbon cable can be used without the need to swap any wires on the cable. The “sysCONFIG” 2x17 header J5 provides connections for 7 additional modes of configuring the LatticeECP3 device: Slave SPI, Single SPI, Multiple SPI, Burst Flash, Slave SCM, Slave PCM, and Master PCM. See TN1169 for more information on the LatticeECP3

configuration modes. Figure 3 shows the 4 configuration headers with pin 1 on each header being the leftmost (and lowest) pin on the connectors.

**Lattice ispDOWNLOAD Cable**

An ispDOWNLOAD cable is included with each LatticeECP3 Advanced board. When using the 1x8 cable adapter, connect pin 1 of the cable to pin 1 of the 1x10 Local JTAG header J10. J10 is the “Local JTAG” connection, a 1x10 100mil header that is provided for use with an external Lattice download cable with fly-wire style JTAG connections. A Lattice parallel port or USB download cable can be attached to the board using J10.

**Important Note:**

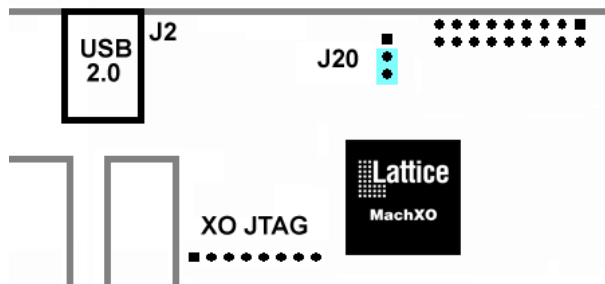
The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable or USB cable. Always connect an ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP3 FPGA and render the board inoperable.

**Built in USB 2.0 Download Cable**

The evaluation board has a USB 2.0 download cable built-in. The built-in cable consists of a USB Type-B connector (J2), a USB microcontroller, and a MachXO device.

To use the built-in USB 2.0 download cable, simply connect a standard USB cable from J2 to your PC (with ispVM System installed), set J20 as shown below in Fig 3 and Table 13, and then remove any cable connections on the Local JTAG connector J10. The USB Hub on the PC will detect the addition of the USB Function making the built-in USB 2.0 download cable available for use with Lattice’s ispVM System software.

**Fig 3. Built in USB 2.0 Enabled as Local JTAG Source at J2**



**Table 13. Built In USB vs. Ext Download Cable Selection**

J20 Position		Local JTAG	Connector	Attach Download Cable
Shunt pins 1-2	UP	J10	1x10 header	Lattice ispDOWNLOAD
Shunt pins 2-3	DOWN	J2	USB Type B	Standard USB cable

Use of the built-in USB 2.0 download cable through J2 must be mutually exclusive to the use of an external download cable on the Local JTAG connector J10. When using an external download cable on J10 rather than the built in USB 2.0 download cable on J2, the jumper on J20 must be

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moved upwards to shunt pins 1-2, this tri-states the MachXO device IO, preventing it from interfering with the external download cable connected to J10.

### LatticeECP3 Configuration Using JTAG

Two programming headers, J10 and J11, are provided on the evaluation board for access to the LatticeECP3 JTAG port and the ispPAC-POWR1220AT8 JTAG port. Note that in this discussion, the built in USB 2.0 download cable can be enabled as described in the previous section to directly access the J10 signals. The pinouts for the J10 and J11 headers are provided in Table 14.

**Table 14. JTAG Programming Headers**

Pin	Local Programming		Multi-board Programming	
	J10 Function	J11 Function	J10 Function	J11 Function
1	3_3V	Not used	3_3V	NC
2	TDO (from J9)	Not used	TDO (from J9)	TDO (from J9)
3	TDI	Not used	TDI	TDI (from J9)
4	PROGRAMN	Not used	PROGRAMN	PROGRAMN (from J18)
5	NC	Not used	NC	NC
6	TMS	Not used	TMS	TMS (buffered Local)
7	GND	Not used	GND	GND
8	TCK	Not used	TCK	TCK (buffered Local)
9	DONE	Not used	DONE	DONE
10	INIT	Not used	INIT	INIT (from J24)

J9 is a 6 pin header that controls the functions of the Local and Multi-board programming headers as shown in Table 15 below:

**Table 15. Selection of Local JTAG or Multi-board JTAG**

J9 Position	J10 and J11 Usage
Shunt pins 1-3	Local JTAG
Shunt pins 1-2, 3-4	Multi-board JTAG
Shunt pins 3-5	ECP3 Only JTAG

The “ECP3 Only JTAG” selection is non-functional in the Rev A boards as the ispPAC device requires an additional header to force TMS high during an ECP3 only JTAG operation.

Typically the evaluation board will be programmed in the Local JTAG configuration where both the ECP3 and ispPAC devices are visible for programming in ispVM. J17 allows bypassing the ECP3 device to allow only programming the ispPAC device as shown in Table 16 below:

**Table 16. Local JTAG Device Programming**

J17 Position	Local JTAG Programming
Shunt pins 1-2	ispPAC only
Open pins 1-2	ECP3 and ispPAC

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Additional instructions and recommendations for programming this board are provided later in this document in the “Configuring/Programming the Board” section.

### Switches

There is one 8-position switch (SW4) and 2 push-button switches (PB1 and PB2) for implementing basic user assigned input functions. Additionally, there are two 3-position switches (SW5 and S1) and 3 push-buttons (SW1, SW2, and SW3) for power manager and ECP3 configuration.

Switches PB1, PB2, SW1, SW2, and SW3 are momentary switches. The pull-up resistors associated with these switches are wired to 3.3V. Pushing the switches down produces a low (0), otherwise it produces a high (1). The signals controlled by SW1, SW2, SW5, and SW7 are debounced by MAX6817 devices (U23 and U24) before connecting to an LatticeECP3 I/O pin. Table 17 shows the control relationship between the switches, LatticeECP3 I/O pins, and USB controller U3.

**Table 17. Momentary Switches**

	Connection	User definable	Debounced
<b>PB1</b>	AM34 of LatticeECP3	Yes	Yes
<b>PB2</b>	AM33 of LatticeECP3	Yes	Yes
<b>SW1</b>	B34 of LatticeECP3 (PROGRAMN)	No	Yes
<b>SW2</b>	D33 of LatticeECP3 (GSRN)	Yes	Yes
<b>SW3</b>	Pin 9 of U3 (USB_RESETh)	No	No

SW4 on the lower side of the board is an 8-pin DIP switch with pullup resistors to the DDR3\_VDD (1.5v) supply. SW3 and S1 are 3-pin DIP switches with pull up resistors to 3.3v. A switch in the down position produces a low (0), the up position produces a high (1). Table 18 shows the SW4 connections to the LatticeECP3, Table 19 shows the S1 connections to ispPAC-POWR1220AT8 I/O pins, and Table 20 shows the SW3 connections to the LatticeECP3.

**Table 18. 8-position Switch SW4**

Switch (Position#)	LatticeECP3 I/O	SysIO Bank
SW4 (position#1)	AJ1	6
SW4 (position#2)	AM2	6
SW4 (position#3)	AM1	6
SW4 (position#4)	AC7	6
SW4 (position#5)	AC6	6
SW4 (position#6)	AD1	6
SW4 (position#7)	AD2	6
SW4 (position#8)	Y10	6

**Table 19. 3-position Switch S1**

Switch (Position#)	POWR1220AT8 I/O Pin	Pin Name
S1 (position#1)	4	IN1
S1 (position#2)	6	IN2
S1 (position#3)	7	IN3

**Table 20. 3-position Switch SW3**

Switch (Position#)	LatticeECP3 I/O	Pin Name	SysIO Bank
SW3 (position#1)	D32	CFG2	8
SW3 (position#2)	F30	CFG1	8
SW3 (position#3)	B33	CFG0	8

## LEDs

The eight user-definable LEDs are provided on the upper center of the board. These LEDs are each controlled by a separate general purpose I/O as defined in the Table 21. The LEDs will light when their associated IO is high and will have a current flowing through them of approximately 3ma, the value of which is set by the NPN current source connected transistors (Q6, Q12, Q13, Q14, Q15, Q16, Q17, Q18) and resistors (R155, R162, R164, R177, R189, R193, R195, R199). The LEDs are off when the IOs are set low.

**Table 21. Connection between LEDs and LatticeECP3**

LED	LatticeECP3 I/O	Bank	LED	LatticeECP3 I/O	Bank
D14	E11	0	D9	B7	0
D12	H13	0	D8	J16	0
D11	E16	0	D7	G17	0
D10	J14	0	D6	E4	0

Table 22 describes the three LEDs associated with the dedicated programming pins.

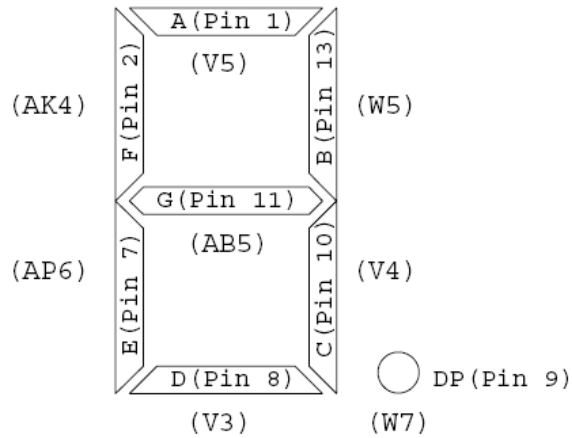
**Table 22. Programming LEDs**

LED	Pin	Color	Function
D4	PROGRAMN	Red	On when signal is low
D2	INIT	Red	On when initializing
D5	DONE	Green	On when config is complete

## Seven Segment Display

The 7-segment LED located near the eight LEDs is controlled by LatticeECP3 bank 6 I/O pins. The connections of the segments are shown below in Figure 3.

**Figure 3. Seven Segment Display**



The LED digit segments will light when their associated IO is high and will have a current flowing through them of approximately 3ma, the value of which is set by the NPN current source connected transistors (Q2, Q3, Q5, Q7, Q8, Q9, Q10, Q11) and resistors (R126, R133, R148, R150, R151, R152, R153, R154). The LED digit segments are off when the IOs are set low.

**LCD**

The LCD module connector (J32) is a 2x9 header. This 18-pin header is compatible with quite a few character LCD modules. Table 23 shows the pin function of the header and the connections to the bank 1 of the LatticeECP3 FPGA.

**Table 23. LCD Header Connection**

Pin #	Function	LatticeECP3 I/O	Pin #	Function	LatticeECP3 I/O
1	Anode	-	2	Cathode(GND)	-
3	VSS(GND)	-	4	VDD(5V)	-
5	VO	-	6	RS	D23
7	R/W	A23	8	E	K22
9	DB0	B23	10	DB1	K21
11	DB2	G22	12	DB3	A24
13	DB4	G23	14	DB5	B24
15	DB6	C23	16	DB7	H22
17	Anode	-	18	Cathode(GND)	-

The VR1 potentiometer is used to limit the current that flows through the backlight LED on the LCD module. The VR2 potentiometer is used to adjust the VO voltage that controls the LCD contrast.

When the following LCD modules are used, connect pin 1 to 16 to the backlight LCD module or connect pin 1 to 14 to the non-backlight LCD module:

Optrex:

- C-51505 Series : 20 characters x 2 lines

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When the following LCD modules are used, connect pin 3 to 18 to the backlight LCD module or connect pin 3 to 16 to the non-backlight LCD module.

Lumex :

- LCM-S01601 Series : 16 characters x 1 line
- LCM-S00802 Series : 8 characters x 2 lines
- LCM-S01602 Series : 16 characters x 2 lines
- LCM-S02002 Series : 20 characters x 2 lines
- LCM-S02402 Series : 24 characters x 2 lines
- LCM-S04002 Series : 40 characters x 2 lines
- LCM-S02004 Series : 20 characters x 4 lines
- LCM-S02404 Series : 24 characters x 4 lines

Varitronix:

- MDLS-20189 Series : 20 characters x 1 line
- MDLS-20265 Series : 20 characters x 2 lines
- MDLS-24265 Series : 24 characters x 2 lines
- MDLS-40266 Series : 40 characters x 2 lines

### Logic Analyzer Probe

The Logic Analyzer Probe connector (LA1) is set up for use with the Agilent 16760A Logic Analyzer probe. The connections between the connector pins and LatticeECP3 I/O are shown in table 18. All the pins are connected to bank 1 I/Os. The bank 1 supply voltage (VCCIO\_1) must be set using J41 to select the proper voltage level expected by the logic analyzer. See Table 24 for the Logic Analyzer probe connections to the ECP3 IO pins.

**Table 24. Logic Analyzer Connections**

Pin #	Function	LatticeECP3 I/O	Pin #	Function	LatticeECP3 I/O
1	5v	-	20	LA16	D19
2	-	-	21	LA17	J19
3	GND	-	22	LA18	K19
4	-	-	23	LA19	A20
5	LA1	E17	24	LA20	B20
6	LA2	F18	25	LA21	G19
7	LA3	A18	26	LA22	H19
8	LA4	B18	27	LA23	D21
9	LA5	J18	28	LA24	E21
10	LA6	H18	29	LA25	H20
11	LA7	D18	30	LA26	J20
12	LA8	E18	31	LA27	A22
13	LA9	G18	32	LA28	B22
14	LA10	F19	33	LA29	J22
15	LA11	A19	34	LA30	J23
16	LA12	B19	35	LA31	C22
17	LA13	K20	36	LA32	D22
18	LA14	L19	37	LA33	J21

19	LA15	C19	38	LA34	H21
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### High Current IO

The High Current IO connector J46 provides a means to evaluate multiple IOs connected in parallel to produce a higher combined output IO current exceeding that of a single IO. The three series resistors R37, R38, and R157 are placed physically close to the ECP3 pins and a 50 ohm signal trace connects the parallel side of the resistors to the SMA connector J46. For best results, the three output IOs at pins H25, H26, and A31 should be set for the FAST setting and driven by the same signal within the ECP3 internal routing.

### DDR3

The two 240-pin DIMM sockets provide a built-in 64-bit interface to standard 1.5V DDR3 SDRAM memory modules. The required VREF and VTT voltages, as well as termination of each signal to VTT are provided. Performance has been verified at above the ??? Mb/s data rate. Write mode dynamic ODT at the memory modules is fully supported, while read mode ODT at the controller (FPGA) is approximated with external terminations optimized for best performance. The connections between the connector pins and LatticeECP3 balls are shown in Table 25.

**Table 25. DDR3 Interface to DIMM Sockets (pin out is in process)**

Description	LatticeECP3 I/O	SysIO Bank	J36
DDR3_DQ0	R21	3	5
DDR3_DQ1	R20	3	7
DDR3_DQ2	N17	3	17
DDR3_DQ3	N16	3	19
DDR3_DQ4	P19	3	4
DDR3_DQ5	R19	3	6
DDR3_DQ6	T21	3	14
DDR3_DQ7	T20	3	16
DDR3_DM0	P16	3	10
DDR3_DQS0_P	T22	3	13
DDR3_DQS0_N	U22	3	11
DDR3_DQ8	K21	3	23
DDR3_DQ9	L21	3	25
DDR3_DQ10	M19	3	35
DDR3_DQ11	M20	3	37
DDR3_DQ12	M17	3	20
DDR3_DQ13	M16	3	22
DDR3_DQ14	M21	3	36
DDR3_DQ15	N21	3	38
DDR3_DM1	P21	3	26
DDR3_DQS1_P	M22	3	31
DDR3_DQS1_N	N22	3	29
DDR3_DQ16	G21	2	43

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DDR3_DQ17	F22	2	45
DDR3_DQ18	J17	2	55
DDR3_DQ19	K17	2	57
DDR3_DQ20	K18	2	44
DDR3_DQ21	L17	2	46
DDR3_DQ22	H22	2	56
DDR3_DQ23	G22	2	58
DDR3_DM2	J16	2	52
DDR3_DQS2_P	H21	2	51
DDR3_DQS2_N	J21	2	49
DDR3_DQ24	H20	2	61
DDR3_DQ25	G20	2	63
DDR3_DQ26	E19	2	73
DDR3_DQ27	F19	2	75
DDR3_DQ28	J20	2	62
DDR3_DQ29	H19	2	64
DDR3_DQ30	C22	2	74
DDR3_DQ31	B22	2	76
DDR3_DM3	H17	2	67
DDR3_DQS3_P	D22	2	70
DDR3_DQS3_N	E22	2	68
DDR3_A0	R18	3	102
DDR3_A1	R17	3	101
DDR3_A2	U21	3	100
DDR3_A3	V22	3	99
DDR3_A4	U20	3	98
DDR3_A5	V20	3	97
DDR3_A6	R16	3	94
DDR3_A7	T17	3	92
DDR3_A8	Y20	3	93
DDR3_A9	Y19	3	91
DDR3_A10	W22	3	105
DDR3_A11	G15	2	90
DDR3_A12	G16	2	89
DDR3_A13	F17	2	116
DDR3_BA0	P20	3	107
DDR3_BA1	P22	3	106
DDR3_BA2	F18	2	85
DDR3_CK0_P	G17	2	30
DDR3_CK0_N	H18	2	32
DDR3_CK1_P	B21	2	164
DDR3_CK1_N	C21	2	166
DDR3_CKE0	J19	2	79

DDR3_CKE1	C20	2	80
DDR3_S0_N	J18	2	110
DDR3_S1_N	H16	2	115
DDR3_RAS_N	K16	2	108
DDR3_CAS_N	L18	2	113
DDR3_WE_N	L19	2	109
DDR3_ODT0	P18	3	114
DDR3_ODT1	N18	3	119
DDR3_SDA	AA2	0	195
DDR3_SCL	Y2	0	197

### Ethernet PHY

In the lower right portion of the board is U18, a Marvell Gigabit Ethernet PHY (88E1111). The LatticeECP3 FPGA interacts with the PHY over a Serial Gigabit Media Independent Interface (SGMII). The PHY is connected to an RJ45 connector J53 on the Media Dependent Interface (MDI). The RJ45 connector J53 has built in magnetics and spark-gap capacitor.

The PHY is available on the board in order to demonstrate the Lattice Ethernet Media Access (MAC) IP core. However, it is also possible to use the PHY to evaluate a custom MAC solution.

Refer to the schematic and the Marvell 88E1111 Data Sheet for detailed information about the operation of the Ethernet PHY interface on this device. Refer to Table 26 for a description of the Ethernet PHY connections.

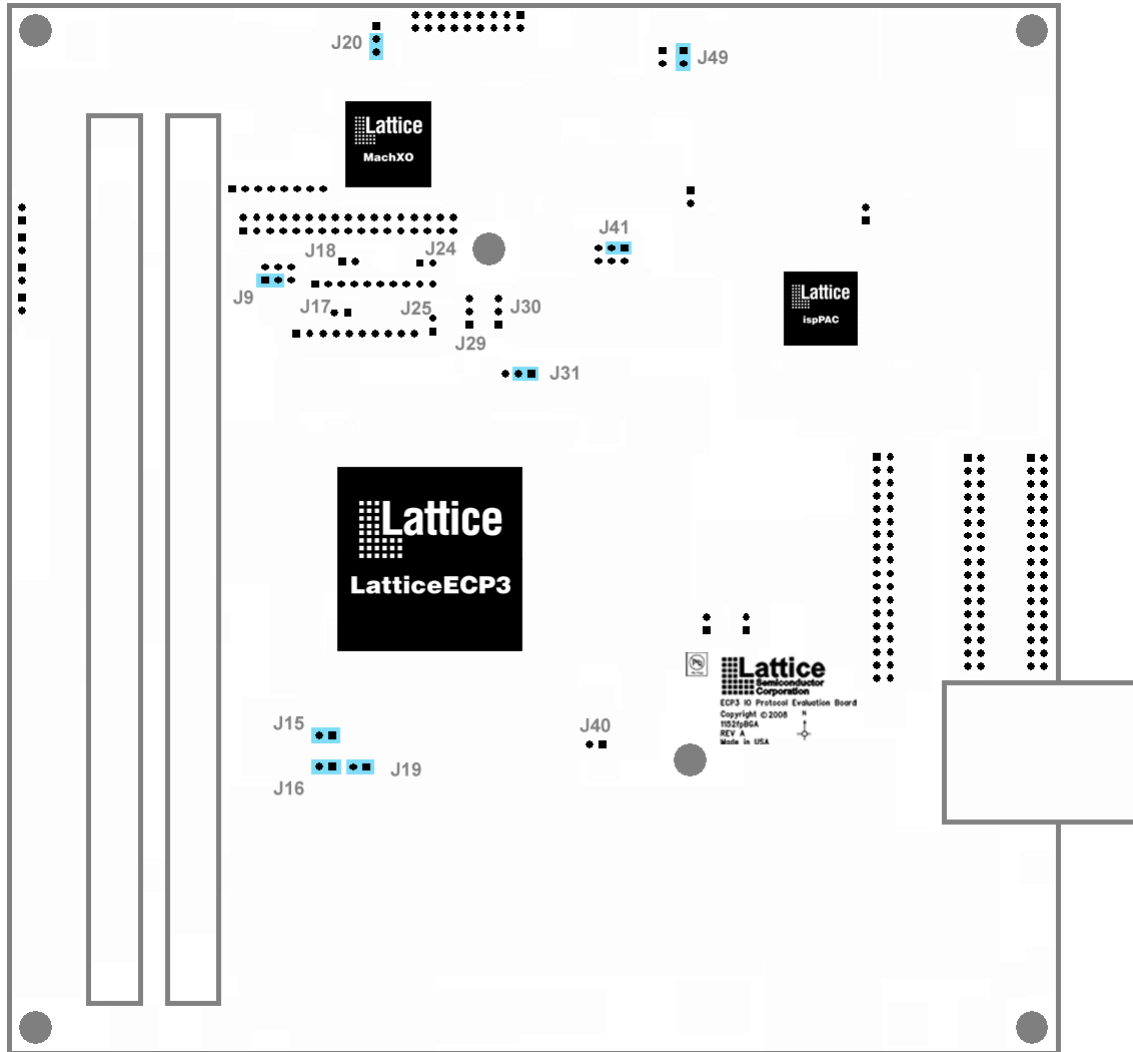
**Table 26. 10/100/1000 Ethernet PHY Connection Summary**

Description	LatticeECP3 I/O	SysIO Bank
ETH_SIN_P	AP21	SERDES
ETH_SIN_N	AN21	SERDES
ETH_SOUT_P	AL21	SERDES
ETH_SOUT_N	AK21	SERDES

### Default Jumper Settings

The evaluation board is shipped with default jumper positions as shown in Figure 4. Some jumper settings are required for bitstream downloading and display functionality.

**Figure 4. Default Jumper Settings**



## Configuring/Programming the Board (in process)

### Requirements

- PC with Lattice Semiconductor's ispVM System version 17.0 (or later) programming software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). *Note: An option to install these drivers is included as part of the ispVM System setup.*
- Any ispDOWNLOAD or Lattice USB Cable (pDS4102-DL2x, HW7265-DL3x, HW-USB-2x, etc.).

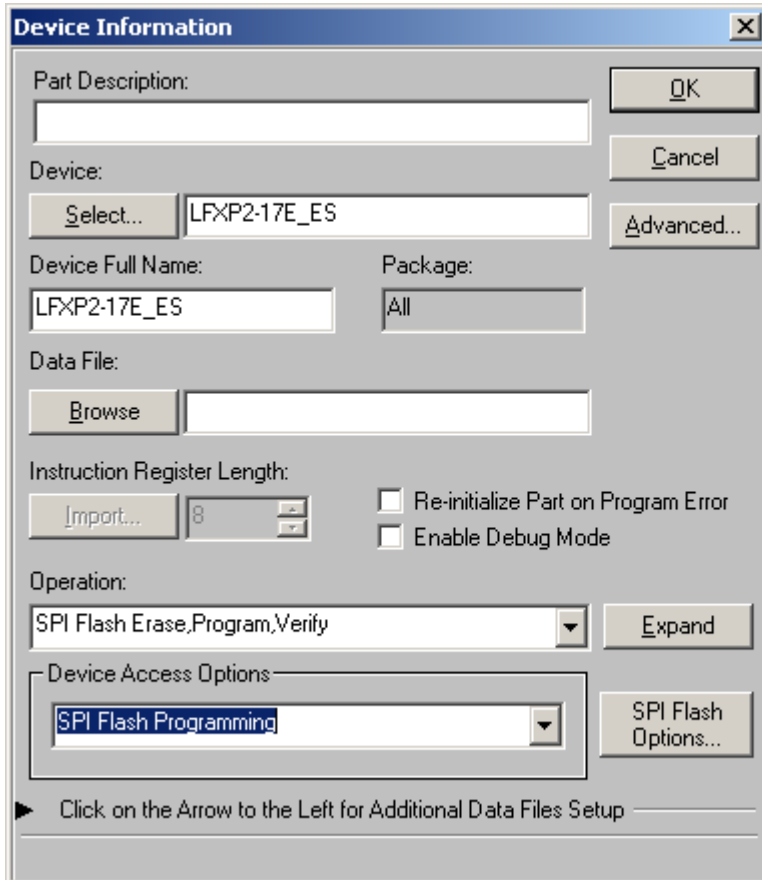
For a complete discussion of the LatticeECP3's configuration and programming options, refer to:

<http://www.latticesemi.com/documents/TN1141.pdf>

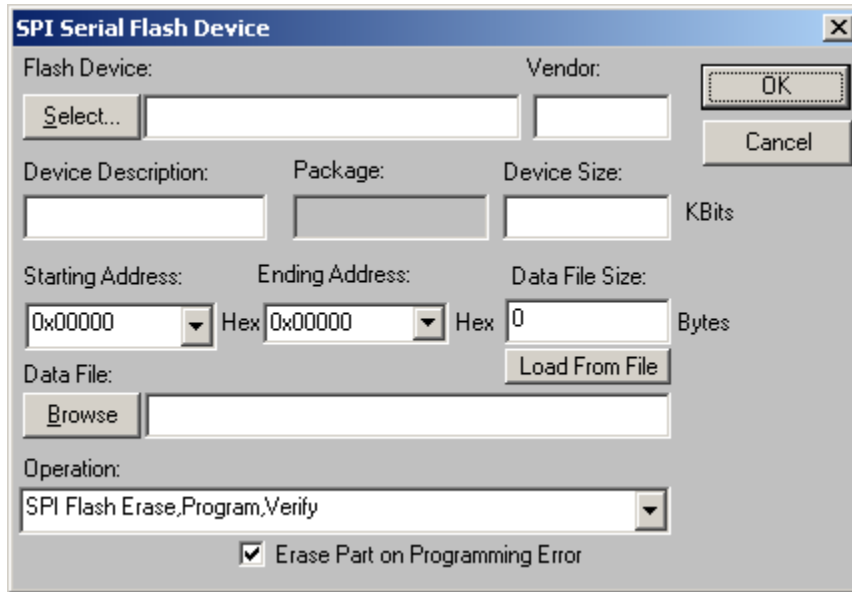


- 6.) Double-click the device as shown in Figure 5 to open the device information dialog, as shown in Figure 6. Select the Device Access Options and select “SPI Flash Programming” as shown in Figure 7.

**Figure 6. Device Information Dialog**

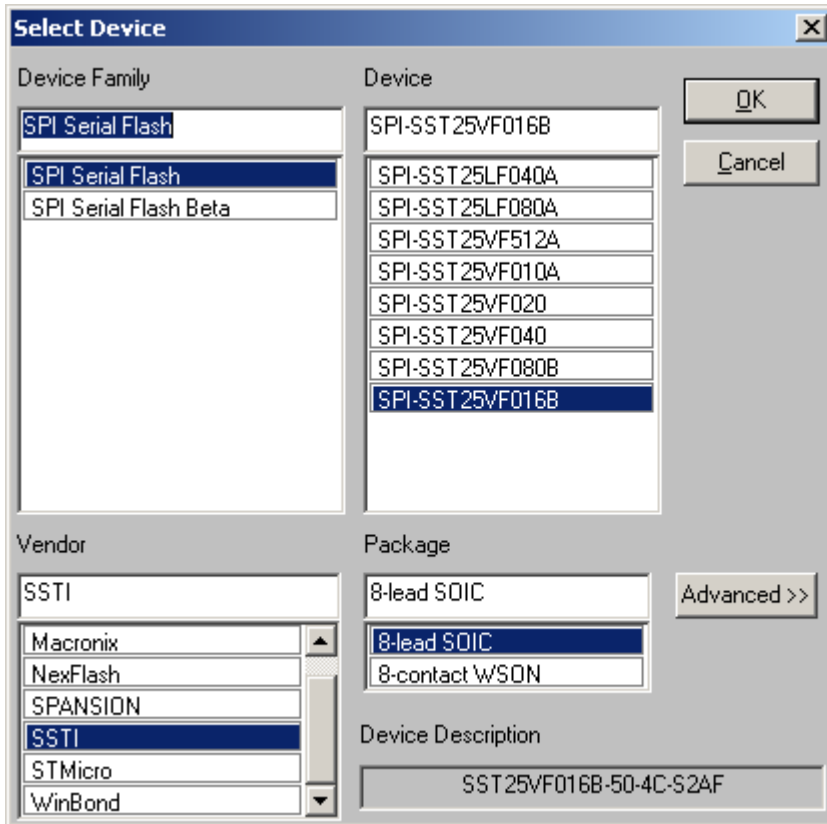


**Figure 7. SPI Serial Flash Device Dialog**



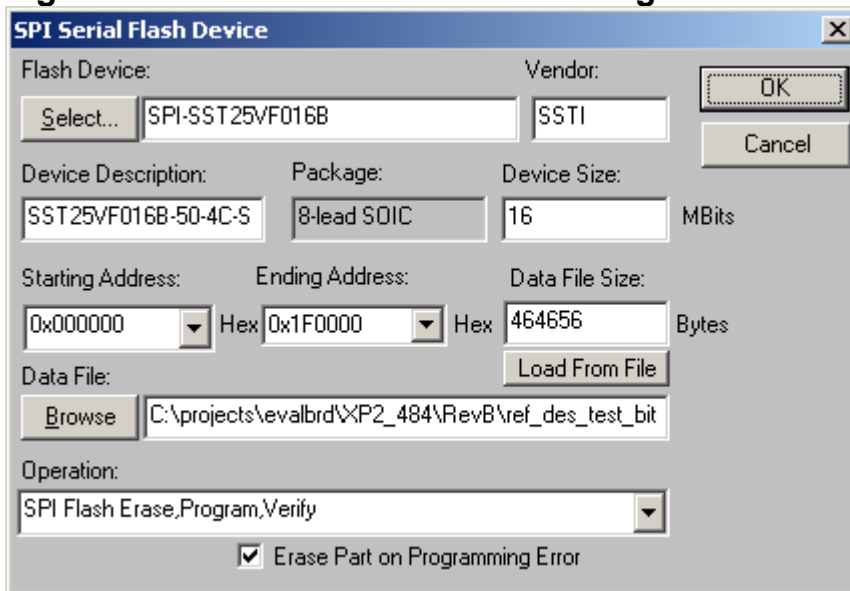
- 7.) Select "Browse" and point to the location of the bitstream file. Note that if you have a ".JED" file output from ispLever, you can convert it to a ".BIT" file using ispVM and selecting the UFW (Universal File Writer) icon with the input file being the ".JED" file from ispLever and the output file being a ".BIT" file.
- 8.) Select "Flash Device" and in the "Select Device" window, change the selections as shown in Figure 8. Press OK to close the "Select Device" window.

**Figure 8. Select Device Dialog**



9.) Check that the “SPI Serial Flash Device” window now appears as shown in Figure 9 then press OK to close the SPI Serial Flash Device window.

**Figure 9. SPI Serial Flash Device Dialog**



10.) Check that the “Device Information” window appears as shown in Figure 10, the press OK to close the “Device Information” window.



- 12.) To begin the download of the bitstream into the SPI Flash, press the “GO” menu button. You will see a small counter display window start up and then that window will change to a “Processing” address window. A blue section of that processing window will start to fill in from the left side until it reaches the right side of the window. When downloading to SPI Flash is complete, ispVM will then begin to verify the downloaded bitstream loaded into the SPI Flash with another small processing window and blue bar moving across it.
- 13.) Upon successful verification of the downloaded bitstream to SPI Flash, the ECP3 device can then be programmed by powering down the evaluation board and re-applying power.
- 14.) You should now see the ECP3 evaluation board’s LED digit display incrementing from 0-9 and a-f, the digit decimal point should be blinking, and the LEDs to the left of the digit should show the internal counter state while the digit count is incrementing.

## Appendix A. Schematic

<Attach schematic>