

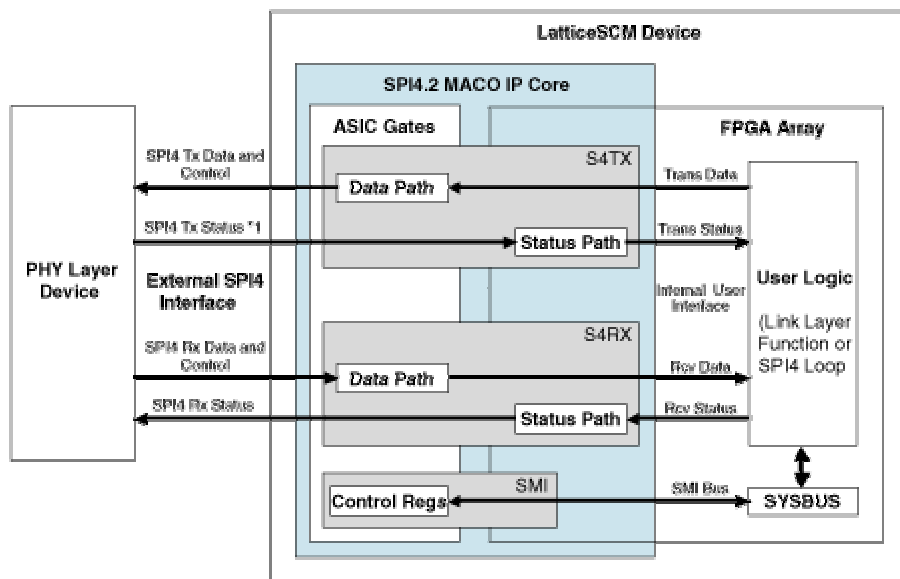


## LatticeSCM SPI4.2 MACO Core

### Overview

The LatticeSCM SPI4 MACO™ IP core implements an industry standard SPI4.2 interface used to transfer both variable length packets and fixed cell sizes between PHY and Link Layer devices in telecom and datacom applications. This flexibility makes it an attractive interface for Ethernet, SONET and ATM applications. Until now, this popular interface was only available as soft IP in FPGAs. The LatticeSCM device implements this core in an optimal combination of hard and soft gates to reduce the size of the core, reduce power and enhance user flexibility. Specifically, the Data Path is implemented in hard logic while the Status path is implemented in soft gates to enable designers to implement their own calendaring or prioritization schemes if they so choose.

This figure shows the SPI4 MACO Core implementation in the LatticeSCM



Note that the SPI4 IP Core is implemented using both MACO ASIC and soft logic in the FPGA array. Since a significant portion of the implementation is in MACO, more of the FPGA Array is left for the user.







## Features

- Fully compliant with OIF-SPI4.02.0 Specification
- Supports up to 256 logical ports
- 700 Mbps operation in Static Mode
- 1+ Gbps operation in Dynamic Mode
- Transmit/Receive Data Path
  - 16 bits wide, in-band port address, SOP, EOP indication, error control
  - LVDS I/O (IEEE 1596.3 – 1966 [1], ANSI/TIA/EIA-644-1995[2])
  - Source synchronous double edge clocking at 311MHz minimum
- Static and Dynamic Alignment Modes
  - Up to 1 Gbps Dynamic Phase Alignment
  - Up to 700 MHz Static Alignment
  - Additional Quarter Rate Mode for sub 10G traffic
- Transmit/Receive FIFO Status
  - 2 bit parallel FIFO status indication, in-band Start of FIFO status
  - LVTTTL I/O or optional LVDS I/O (IEEE 1596.3)
  - Source synchronous clocking
- Various run-time user controls:
  - Individual receiver/transmitter resets
  - De-skew only reset, ALL only reset
  - Force idles (transmitter)
  - Enable/Disable Packing (transmitter)
  - Training Pattern (CAL\_M, MAX\_T) Programmable burst modes to support NPU requirements
- Link Layer Buffer Management Options (NEW):
  - Shared or per-channel buffer manager
  - Up to 16 separate physical FIFOs per Tx/Rx direction
  - Transmit Bandwidth Manager and Receive Channel Mapper
  - Parameterizable packet overflow and packet error drop
  - Graceful packet overflow drop
  - Both store & forward as well as cut-through operation
  - Parameterizable independent buffer depth per transmit and receive direction
  - Per channel empty, almost empty, full and almost full status
  - Programmable almost empty and almost full thresholds per channel
  - Dynamic channel provisioning
  - Programmable sequencer based scheduler.





- Supported by System Bus and Serial Memory Interface (SMI) for in-circuit controllability
- Pre-engineered hard cores using MACO technology to conserve power, FPGA resources and designer time
- Multiple SPI4 IP core support per device
- Supported in Windows, Linux, or Unix based tool flows
- Supports both Verilog and VHDL tool flows

Software Requirements:

- ispLEVER version 7.0 or later
- MACO design kit
- MACO license file

For further information please contact your local Lattice contact at MSC Vertriebs GmbH.





## LOW COST LatticeECP2M DEVELOPMENT KIT

### Overview

Lattice offers Development Kits for key application markets such as connectivity, high-speed communications, and video/imaging. The kits typically include pre-configured demo bitstreams along with GUI/API and drivers for quick evaluation, source files for the GUI and drivers to recreate the demo and GUI, RTL project directory source files to use as a design template, and an evaluation board to take designs rapidly to hardware. Lattice's ispLEVER design tool suite is required in order to use the Development Kits.

The following Development Kits are currently available:

- [LatticeECP2M PCI Express Development Kit](#)

With Lattice Development Kits, designers can:

- Accelerate the time to create a prototype
- Enhance the design flow for better productivity
- Create a solution compliant to industry standards

### Accelerate Time to Prototype

Lattice Development Kits have been created to help accelerate the design cycle and get to prototyping quickly. The Development Kits provide a known good design and demo as a starting point for evaluation and design exploration. From there, you can rebuild the design, rebuild the demo and drivers, and then even modify the design and drivers to create your own implementation. This reduces design cycle time from weeks to days, and with a Lattice evaluation board, accelerates you to a working prototype.

### Enhanced Design Flow for Better Productivity

Each of the kits leverages the standard ispLever design flow and complements it with enhanced tools for better design productivity. The evaluation netlist bitstreams included in each Development Kit are pre-configured versions of Lattice's ispLeverCORE modules. Using these with the included demos,

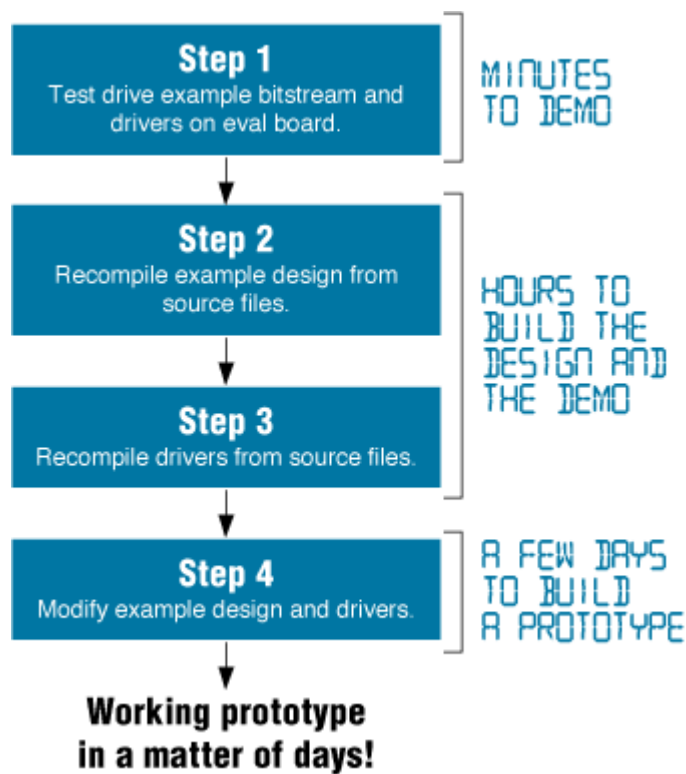




designers can set parameters and view results of typical system operation. RTL source files for top-level project directories are also included, so that designers can use them as an IP instantiation template or recreate the evaluation bitstreams using the ispLEVER design flow. Drivers can also be regenerated as well using the supplied driver source files. Designers can also configure IP and generate their own bitstreams by accessing the IP modules through the IPexpress flow of the ispLEVER design tool suite. Using this design flow, trial designs can be conceived and prototyped on an evaluation board in minutes.

### Compliance to Industry Standards

Several of the IP cores and evaluation boards included in Lattice Development Kits have been subjected to compliance and interoperability testing with industry standards bodies such as PCI-SIG. This gives designers confidence that an application developed with a Lattice Development Kit is high quality, reliable, and interoperable with existing systems based on those standards.



For further information please contact your local Lattice contact at MSC Vertriebs GmbH.

