

LatticeSC FPGA Family

Innovation, Integration, and PURESPEED™

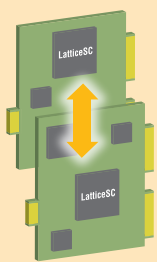
The LatticeSC™ (System Chip) family of FPGAs combines a high-performance FPGA fabric, 3.4Gbps SERDES and PCS, high-performance I/Os, large embedded RAM, and embedded ASIC blocks in a single industry-leading architecture. This FPGA family is fabricated on a state-of-the-art Fujitsu 90nm technology to provide the highest performance FPGA in the industry.

This family of devices includes specific features to meet the needs of today's high-speed connectivity-based system designs. These features include SERDES, the industry's most advanced embedded PCS (Physical Coding sub-layer), up to 7.8Mb of Embedded Block RAM (EBR), and dedicated I/O logic to support source synchronous I/O standards such as RapidIO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. A plethora of hierarchical clock routing and clock management resources are provided to support the precise programmable logic timing needed in today's high-end system designs. High-speed I/O with bandwidths up to 2Gbps per pin make this family ideal for high throughput systems. And for low-cost system-level integration, the LatticeSC family offers up to 12 embedded structured ASIC blocks per device with a variety of pre-engineered IP blocks.

High-Speed Connectivity Solutions

BACKPLANE / HIGH SPEED SERIAL

- Integrated high-speed SERDES
- Supports SONET, GbE, XAUI, PCI Express, Fibre Channel and more
- More SERDES channels for greater flexibility and easier customization



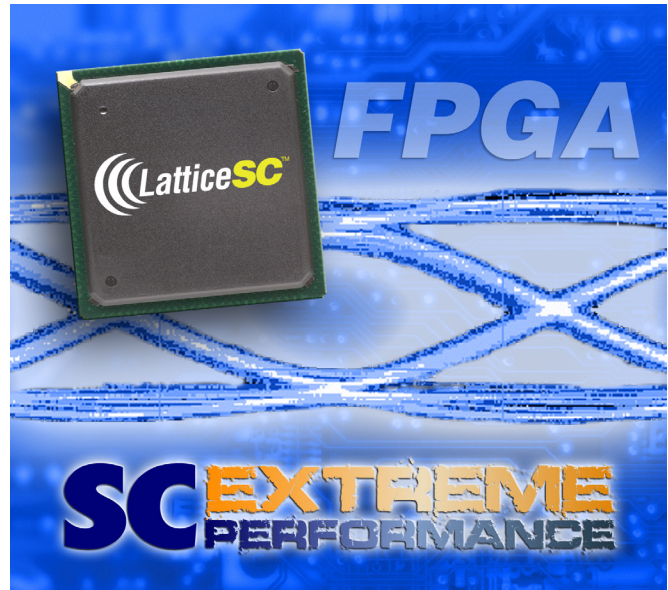
CHIP-TO-CHIP / CHIP-TO-MEMORY

- Lattice PURESPEED™ I/O technology enables connectivity to virtually any digital device
- Each PURESPEED I/O buffer supports up to 2Gbps
- Supports parallel I/O standards, from 2Gbps LVDS to PCI/PCI-X
- Dedicated interface logic seamlessly handles SDR/DDR/QDR memories



NETWORKING DATAPATH

- Ideal for bridging ASSPs
- LatticeSC devices include: high-speed logic, embedded RAM, fast clocking schemes, and ample routing for maximum utilization



Key Features and Benefits

- **High Performance FPGA Fabric**
 - 15K to 115K Four-Input Look-up Tables (LUT4s)
 - 139 to 942 I/Os
 - 700MHz global clock; 1GHz edge clocks
- **High Speed SERDES and flexiPCS™**
 - 4 to 32 SERDES per device @ 600Mbps to 3.4Gbps
 - Tx pre-emphasis and Rx equalization
 - Low power (100mW per channel)
 - Embedded Physical Coding Sublayer (PCS) supports: PCI Express, GbE, XAUI, SONET, 1G Fibre Channel, 2G Fibre Channel and Serial Rapid IO
- **PURESPEED™ Technology: 2Gbps Parallel I/O**
 - Input Delay (INDEL) and Adaptive Input Logic (AIL) dynamically aligns data for robust high performance source synchronous I/O support
 - Supports generic DDR up to 2Gbps; generic SDR up to 1Gbps; DDR memories up to 800Mbps
 - Comprehensive standards support: LVCMOS; LVTTTL; PCI, PCI-X; LVDS, Bus-LVDS, MLVDS, LVPECL; with programmable On Die Termination (ODT) options
- **Memory Intensive FPGA**
 - 1Mb to 7.8Mb Embedded Block RAM @ 500MHz
 - Additional Distributed RAM: 240K to 1.8Mbits
- **sysCLOCK™ PLLs and DLLs**
 - Eight PLLs per device and twelve DLLs per device
 - Spread spectrum support on PLLs
- **Masked Array for Cost Optimization (MACO)**
 - On-chip structured ASIC blocks provide pre-engineered IP at lower power and cost
- **System Level Support**
 - IEEE Standard 1149.1 boundary scan
 - IEEE Standard 1532 in-system configuration
 - Embedded PowerPC microprocessor interface
 - Embedded system bus

LatticeSC Architecture

Architecture Overview

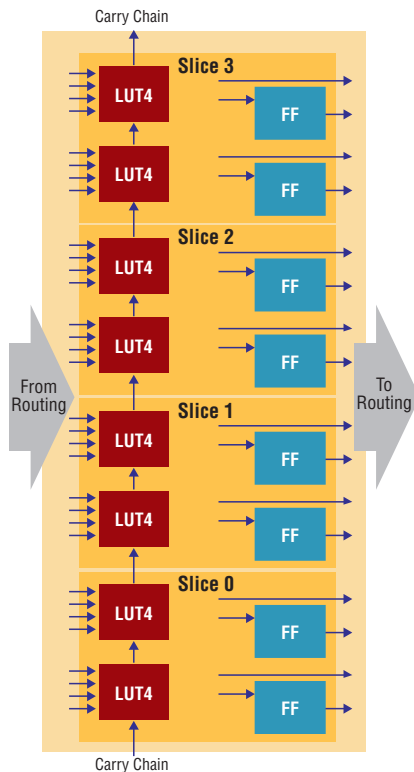
The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, structured ASIC blocks, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated on Fujitsu's state-of-the-art 90nm CMOS process technology to provide one of the highest performance FPGAs in the industry.

Programmable Function Unit Blocks (PFU)

The core of LatticeSC devices consists of Programmable Functional Units (PFUs). The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

- Four Slices per PFU
- Each Slice Individually Programmable
- Slices can be Concatenated for Longer Functions
- PFUs can be Concatenated for Complex Functions

PFU BLOCK DIAGRAM

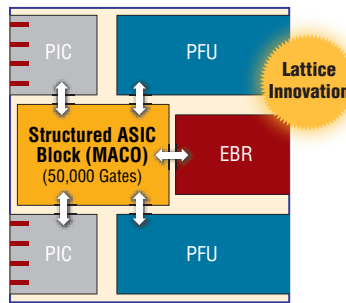


MACO Masked Array for Cost Optimization (MACO™)

LatticeSC FPGAs feature multiple structured ASIC Blocks, each containing 50,000 ASIC gates for low-power, high-performance needs. MACO blocks are the perfect solutions for cost-effective IP implementations giving maximum performance. LatticeSCM devices include pre-engineered IP such as a memory controller, flexiMAC™ multiprotocol engine, and SPI4.2 interface.



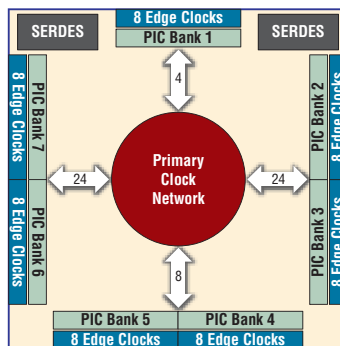
MACO BLOCK LAYOUT



Extreme Clocking Performance

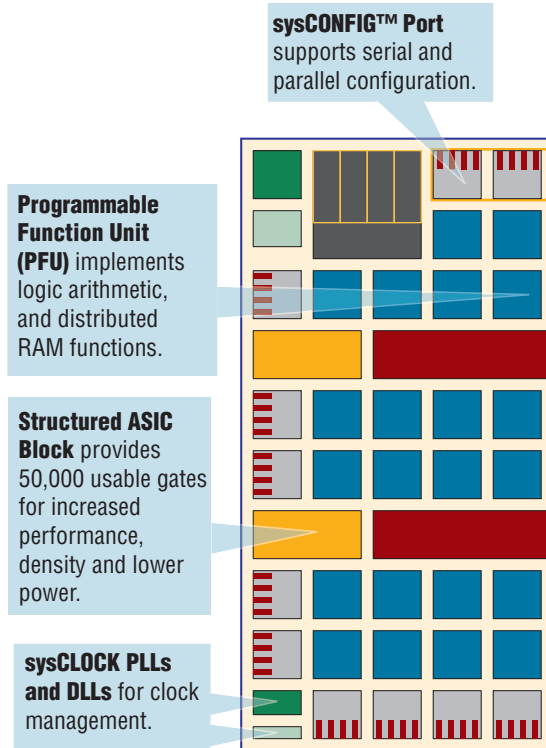
To support an internal fabric capable of 500MHz performance, LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks; secondary clocks; and edge clocks. In addition, the LatticeSC is the only FPGA that combines, on one device, multiple programmable PLLs and DLLs for clock multiplying, dividing and phase shifting.

EDGE AND PRIMARY CLOCKS



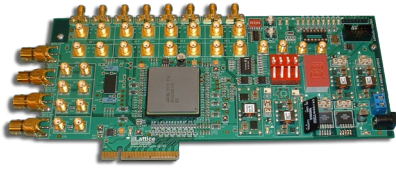
Lattice offers the most advanced portfolio of innovative packaging solutions available today. With up to 942 I/Os and 32 SERDES channels in a device, the LatticeSC family is offered in wire-bonded BGA and Flip Chip packages to 1704 balls.

LatticeSC Block Diagram



sysCLOCK PLLs & DLLs for Tight Timing Control

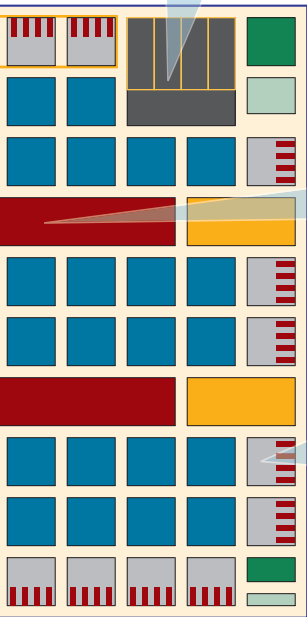
- PLLs Feature:
 - Output 1.56MHz to 1GHz
 - VCO 100MHz to 1GHz
 - Input 15MHz to 1GHz
 - Low output jitter
 - Dynamic reconfiguration of loop parameters
 - Programmable M, N dividers (1x–64x)
 - Spread Spectrum generation support
- DLLs Feature:
 - Output 1.56MHz to 700MHz
 - Input 100MHz to 700MHz
 - Output dividers (1/2, 1/4)
 - Digital control for use with INDEL
 - Duty cycle correction
- Additional Clocking Features
 - Phase matched clock dividers
 - Dynamic clock switching



The LatticeSC evaluation board provides a platform to fully evaluate the benefits of **Extreme Performance** in a lab setting.

gram

Quad SERDES + Embedded PCS – each channel runs from 600Mbps to 3.4Gbps with 100mW power dissipation and excellent Tx and Rx jitter characteristics.



sysMEM Embedded Block RAM offers configurable memory densities to 7.8Mbit per device.

Programmable I/O Cells (PICs) include PURESPEED buffers that support over 20 I/O standards.

SERDES and flexiPCS

Lattice pioneered the concept of combining SERDES and optimized PCS on a programmable device.

- Up to 32 Channels per Device
- Speeds from 600Mbps up to 3.4Gbps
- High Rx Jitter Tolerance (0.8UI @ 3.2Gbps)
- Low Tx Jitter (0.29UI @ 3.2Gbps)
- Receiver Programmable Coupling (AC or DC)
- Channel Bonding on a Single Device and/or between Devices
- Tx Pre-emphasis and Rx Equalization for Improved BER over Long FR-4 Trace Lengths (>60")
- Very Low Power (100mW/Ch Typical @ 3.125Gbps)
- PCS Compliant to a Number of Current and Emerging Standards



Lattice's innovative flexiPCS technology provides embedded multi-protocol Physical Coding Sublayer (PCS) functionality in LatticeSC FPGAs.

sysMEM™ Embedded Block Memory

Each 18Kb sysMEM block can implement single port, true dual port, pseudo dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation.

- 1Mb to 7.8Mb of Block Memory per Device
- 500MHz Operation
- Configurable Width/Depth
- Bus Size Matching
- RAM Initialization & ROM Operation
- Memory Cascading

FLEXIBLE sysMEM BLOCKS

Memory Mode	Configurations	
Single Port	16,384 x 1	2,048 x 9
	8,192 x 2	1,024 x 18
	4,096 x 4	512 x 36
True Dual Port	16,384 x 1	2,048 x 9
	8,192 x 2	1,024 x 18
	4,096 x 4	512 x 36
Pseudo Dual Port	16,384 x 1	2,048 x 9
	8,192 x 2	1,024 x 18
	4,096 x 4	512 x 36
FIFO	16,384 x 1	2,048 x 9
	8,192 x 2	1,024 x 18
	4,096 x 4	512 x 36

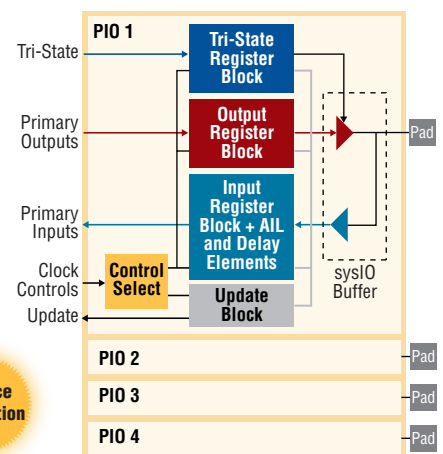
PURESPEED

Extreme Performance I/O Technology

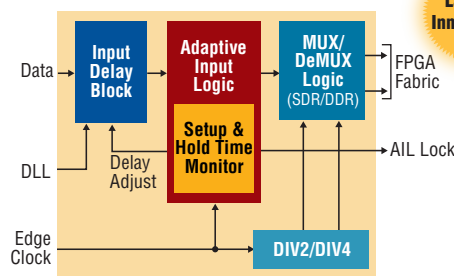
Programmable I/O Cells

Each Programmable I/O Cell (PIC) contains four programmable IOs (PIOs) connected to their respective buffer which are then connected to the device pads. The PIO contains innovative capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces. In addition each pin features digitally controlled on-chip output impedance and input termination.

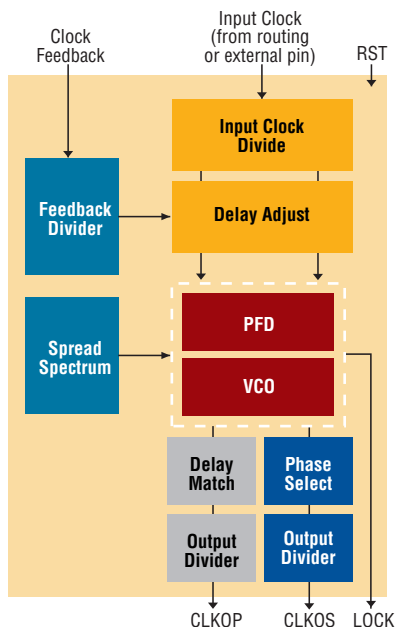
PROGRAMMABLE I/O CELL (PIC) BLOCK DIAGRAM



INDEL AND AIL BLOCK DIAGRAM



sysCLOCK PLL BLOCK DIAGRAM



ispLeverCORE™ Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used functions. Factory supported IP cores targeted to the LatticeSC FPGA family include:

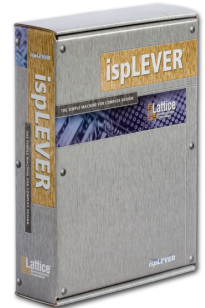
- PCI Express
- Serial RapidIO
- SPI4.2
- 10GbE MAC
- PCI 33MHz
- PCI 66MHz
- DDR1/DDR2
- Triple Speed MAC
- ASI
- SGMII
- OBSAI
- CPRI
- DMA



For additional IP cores, go to www.latticesemi.com/ip. Lattice's ispLeverCORE Connections partners also offer a wide range of IP for Lattice FPGA families.

ispLEVER Design Tools

Lattice's ispLEVER® software is a comprehensive design environment for the LatticeSC architecture. The ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floorplanning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Mentor Graphics and Synplicity are included with ispLEVER.



LatticeSC Device Selection Guide

Parameter	LFSC15	LFSC25	LFSC40	LFSC80	LFSC115
Logic Resources – LUTs (K)	15.2	25.4	40.4	80.1	115.2
sysMEM EBR RAM Blocks (18Kb / Block)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.80
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Max. # of SERDES Channels (3.4Gbps)	8	16	16	32	32
DLLs	12	12	12	12	12
PLLs	8	8	8	8	8
MACO Blocks	4	6	10	10	12
Packages	I/O / SERDES Count				
256-ball fpBGA (17 x 17 mm)	139 / 4				
900-ball fpBGA (31 x 31 mm)	300 / 8	378 / 8			
1020-ball ffBGA (33 x 33 mm)		484 / 16	562 / 16		
1152-ball fcBGA (35 x 35 mm)				660 / 16	660 / 16
1704-ball fcBGA (42.5 x 42.5 mm)				904 / 32	942 / 32

Note: Preliminary Information. For information on MACO enabled LatticeSCM devices, please refer to the LatticeSC data sheet.

Applications Support

1-800-LATTICE (528-8423)
 (503) 268-8001
techsupport@latticesemi.com
www.latticesemi.com

Copyright © 2006 Lattice Semiconductor Corporation. Lattice Semiconductor, L (stylized) Lattice Semiconductor Corp., and Lattice (design), flexiMAC, flexiPCS, ispLEVER, ispLeverCORE, LatticeSC, MACO, PURESPEED, sysCLOCK, sysCONFIG, sysIO, and sysMEM are either registered trademarks or trademarks of Lattice Semiconductor Corporation in the United States and/or other countries. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.



February 2006
 Order #: I0181