



# ispXPGA

**Non-Volatile Infinitely-Reconfigurable Instant-On FPGAs**

## The World's First FPGA to Offer Non-Volatility and Reconfigurability

The ispXPGA™ family of devices allows the creation of high-performance logic designs that are both non-volatile and infinitely reconfigurable. Other FPGA solutions force a compromise, being either re-programmable, or reconfigurable, or non-volatile. This family offers *all* of these



capabilities with a mainstream architecture containing the features required for today's system-level design. We call this concept ispXP™, for eXpanded Programmability.

## ispXPGA Programming / Configuration

- Auto-configure at Power-up in Microseconds
- Reconfigure In-System
- Reprogram During System Operation
- Configure from On-Chip E<sup>2</sup> or CPU
- Set Security Bits to Prevent Readback
- No External Configuration Memory
- Totally Secure from Bit-Stream Snooping

## Key Features and Benefits

- **Non-Volatile, Infinitely Reconfigurable**
  - Power-up in Microseconds via On-Chip E<sup>2</sup> Cells for Instant-on Usage
  - Reconfigure SRAM-based Logic In-System
  - In-System Programmable
  - No External Configuration Memory
- **System-Level Integration**
  - 139K to 1.25M System Gates
  - Up to 496 I/Os
  - Up to 414Kb Embedded Memory
- **High Performance Logic Blocks (PFUs)**
- **Block and Distributed Memory**
- **Variable-Length-Interconnect™ Routing**
- **sysCLOCK™ PLLs for Clock Management**
- **sysIO™ for High Performance Interfacing**
- **sysHSI™ for 850Mbps Serial Communications**
- **1.8V, 2.5V, and 3.3V Operation**

Instant-on  
Non-Volatile &  
Reprogrammable

## ispXPGA Family

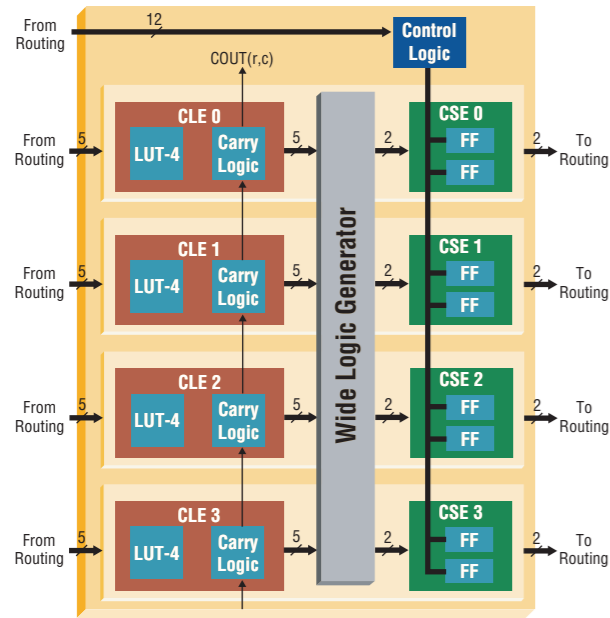
Family Member	System Gates	PFUs	LUT-4	Logic FFs	Block RAM	Distributed RAM	sysHSI™ Channels	User I/O	Vcc	Packaging	Body Size
<b>ispXPGA 125</b>	139K	484	1936	3.8K	92K	30K	4	160 176	1.8, 2.5, 3.3V	256 fpBGA 516 fpBGA*	17x17mm 31x31mm
<b>ispXPGA 200</b>	210K	676	2704	5.4K	111K	43K	8	160 208	1.8, 2.5, 3.3V	256 fpBGA 516 fpBGA*	17x17mm 31x31mm
<b>ispXPGA 500</b>	476K	1764	7056	14.1K	184K	112K	12	336 336	1.8, 2.5, 3.3V	516 fpBGA* 900 fpBGA	31x31mm 31x31mm
<b>ispXPGA 1200</b>	1.25M	3844	15376	30.8K	414K	246K	20	496 496	1.8, 2.5, 3.3V	680 fpSBGA* 900 fpBGA	40x40mm 31x31mm

\* Thermally enhanced

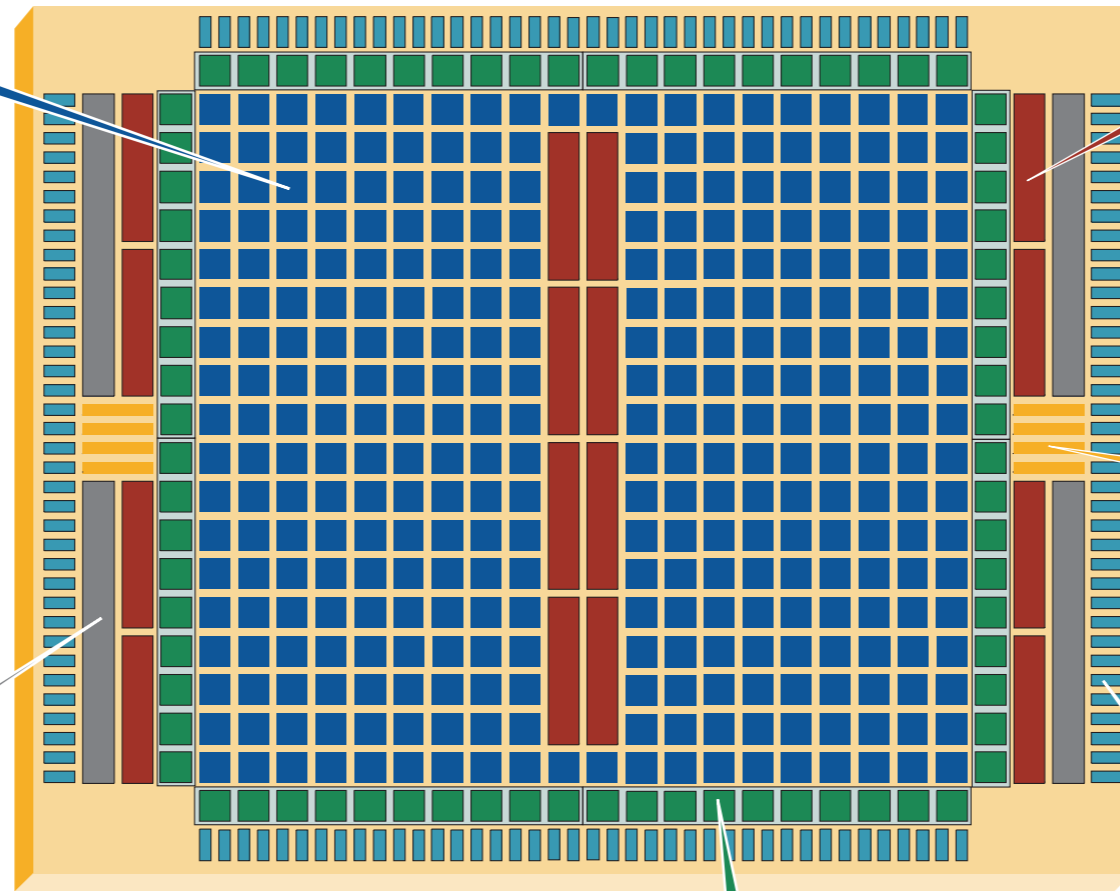
# ispXPGA Architecture

## Programmable Function Unit (PFU)

- Dedicated Arithmetic Logic
- Up to 20-Input Logic Functions
- Dual Flip Flop per LUT-4 for Pipelining
- 64 Bits of Distributed Memory
  - Single-Port, Dual-Port or Shift Register

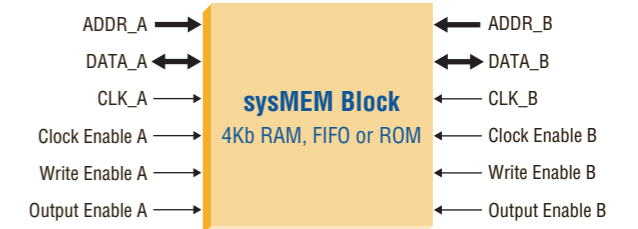


## ispXPGA Block Diagram



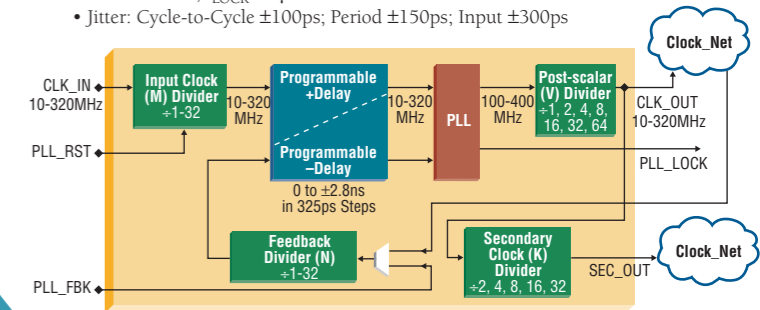
## sysMEM™ Embedded RAM Blocks

- Up to 414Kb of Dedicated Memory per ispXPGA
- Configurable as Single- or Dual-Port RAM, FIFO or ROM
- 512x9 Bits or 256x18 Bits
- Cascadable Width and Depth
- Sub-3ns Access Times



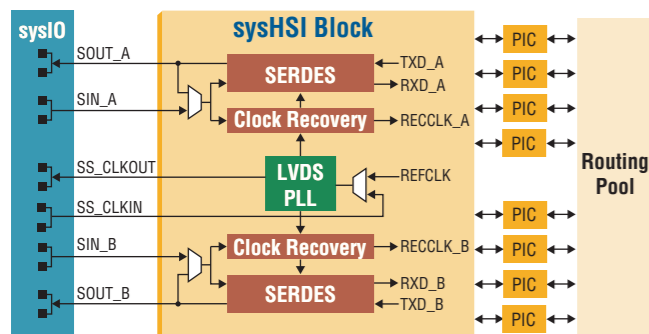
## sysCLOCK Phase Locked Loops (PLL)

- 8 PLLs per Device
  - Plus 8 Global Clocks
  - Plus 8 Low-Skew Clock Nets
- Clock Frequency Synthesis
- Multiple Clock Signal Generation
- Device or Board Clock Alignment
- 10 - 320MHz,  $t_{LOCK}$  25  $\mu$ s
- Jitter: Cycle-to-Cycle  $\pm$ 100ps; Period  $\pm$ 150ps; Input  $\pm$ 300ps



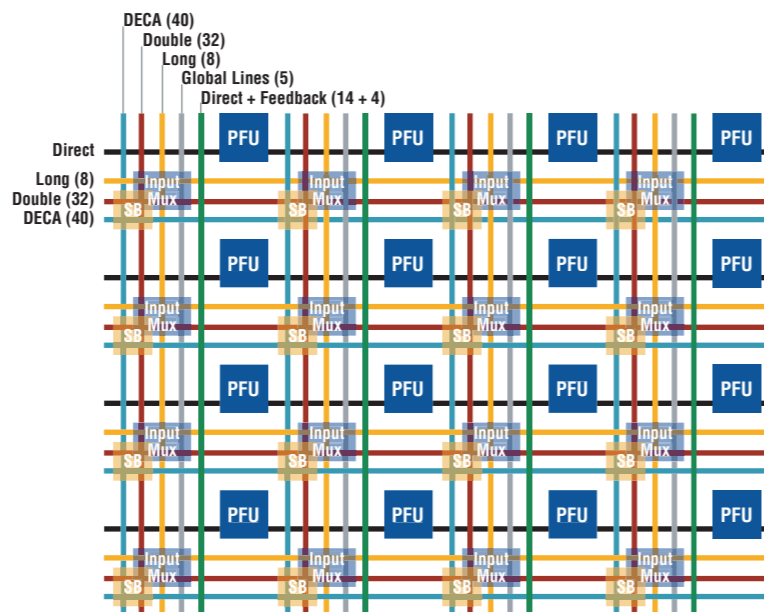
## sysHSI Blocks

- Dedicated High-Speed Interface (HSI) Circuits
- Built-in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)
- 850 Megabit LVDS, Up to 20 Channels per Device
- Can be utilized separately to allow multiple reference clocks and data rates
- 8B/10B and 10B/12B Coding
- Up to 34 Gbps



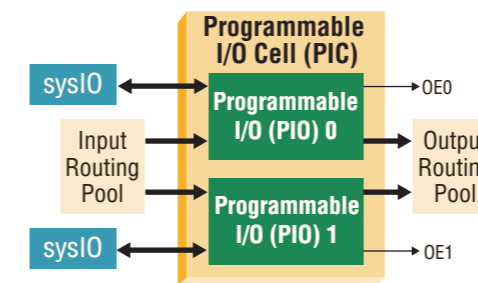
## Optimized Routing Resources

- Segmented Routing for Superior Fitability and Performance
- Intra-PFU Feedback
- Direct, Double, Deca and Long Connects



## Flexible I/O Cells

- Separate Input, Output and OE Registers
- Flexible Set, Reset, Clock Enable and Polarity
- Input Register Offers Delay Option for Zero  $t_{HOLD}$
- Programmable Output Slew Rate



## sysIO High Speed Interface

- Supports Multiple Interface Standards
- Programmable Drive Strength for Series Termination
- Programmable Bus Maintenance
- Multiple Banks for Easy Control

Chip to Memory	Chip to Chip	Chip to Backplane
SSTL2 I and II	LVTTL	PCI33_3
SSTL3 I and II	LVC MOS 3.3	PCI66_3
HSTL I	LVC MOS 2.5	PCI-X
HSTL III	LVC MOS 1.8	GTL+
HSTL IV	Prog. Impedance	AGP
CTT		Bus-LVDS
↓		LVDS
SDRAM		LVPECL
DDR SRAM		
QDR SRAM		
ZBT SRAM		

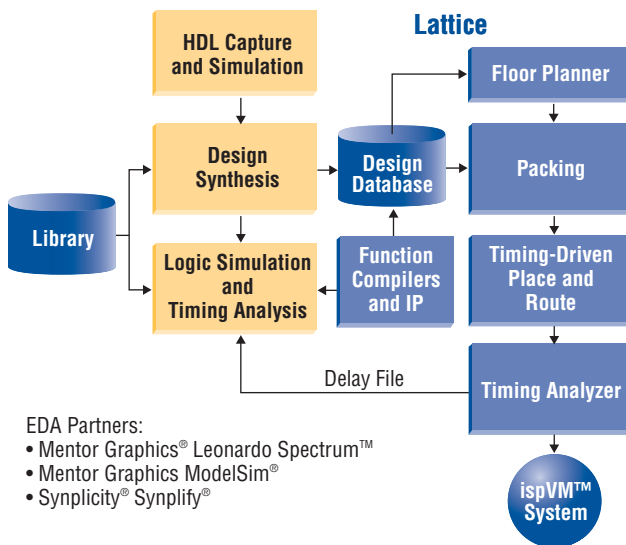
## ispLEVER™ Design Software

Lattice's ispLEVER is a new generation of PLD design tool equipped to provide a complete system for FPSC, FPGA, ispXPLD™, CPLD, ispGDX® and SPLD design. ispLEVER includes a fully integrated, push-button design environment and advanced features for interactive design optimization and debug.

### Features

- Fully Integrated Synthesis and RTL and Timing Simulation Tools
- Complete Design Flow for All In-System Programmable (ISP™) Lattice Device Families
- Advanced Timing-Driven Placement and Routing
- IP Manager and Module Generator
- Fast, Efficient Run Times and Competitive Device Performance and Utilization
- Supported by Libraries from Leading CAE Vendors
  - Aldec
  - Cadence
  - Innoveda
  - Mentor Graphics
  - Synopsys
  - Synplicity
- Windows® and UNIX® Solutions

### ispLEVER Design Software Flow Chart



## ispXPGA Select Performance

T<sub>A</sub> = 25° C; V<sub>CC</sub> = 1.8V

Function	Speed	
4-Input LUT Delay		440ps
Synchronous Counter	8-bit	334MHz
Loadable Up/Dn Carry-Ripple Counter	64-bit	156MHz
Carry-Ripple Adder	64-bit	232MHz
Multiplexer	64:1	237MHz
De-Multiplexer	1:64	371MHz
Shift Reg Up/Dn, Circular Shift	64-bit	315MHz
Barrel Shifter	64-bit	184MHz
PLL Frequency	Min	10 MHz
	Max	320 MHz
LVDS with Clock Recovery	Max	850Mbit

### Applications Support

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