

Introduction

The Lattice Semiconductor ispPAC10 In-System-Programmable (ISP™) Analog Circuit allows designers to build analog circuits such as gain stages and active filters without the use of external feedback resistors or capacitors. This technology brings in-system programmability to the analog world. Device functionality as well as parameters such as gain and frequency response can be set by the user and changed on-the-fly by reprogramming the device. A standard JTAG IEEE 1149.1 interface allows the user to reconfigure the ispPAC10 while in-system using on-chip non-volatile E²CMOS[®] technology.

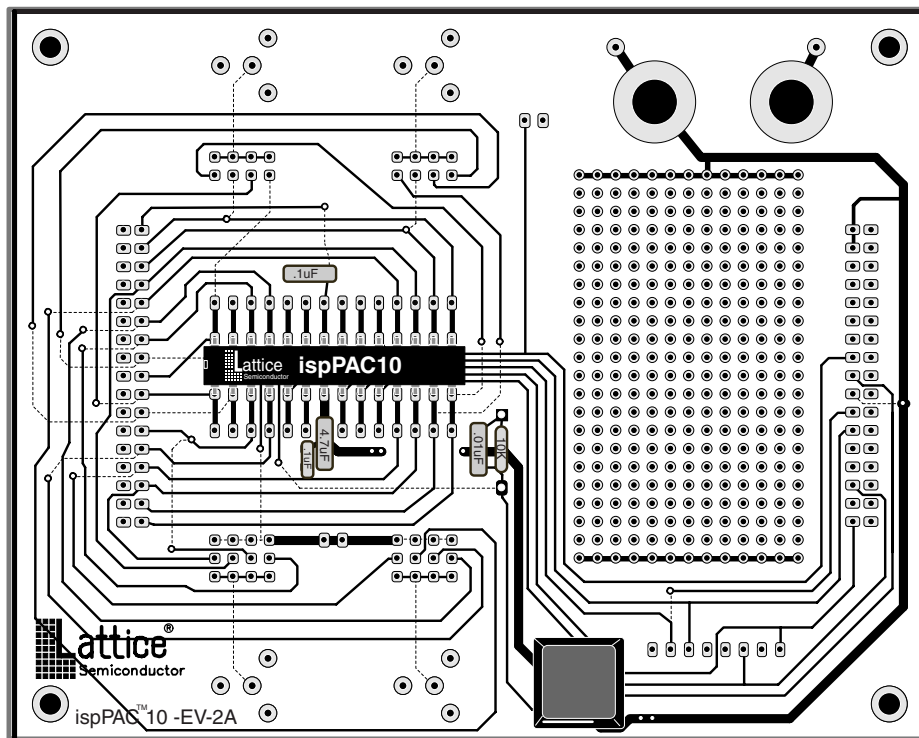
ispPAC10 Evaluation Board

The ispPAC10 Evaluation Board (Figure 1) allows the user to quickly configure and evaluate the ispPAC10 on a fully assembled PC board. The double sided board supports a 28-pin DIP package, connectors for Input and Output signals, a JTAG programming cable interconnect and a prototype array section for additional circuitry to be

added by the user. In-system programming is accomplished through the JTAG port. The JTAG signals are driven from the parallel port of a PC through an isp-DOWNLOAD[®] Cable.

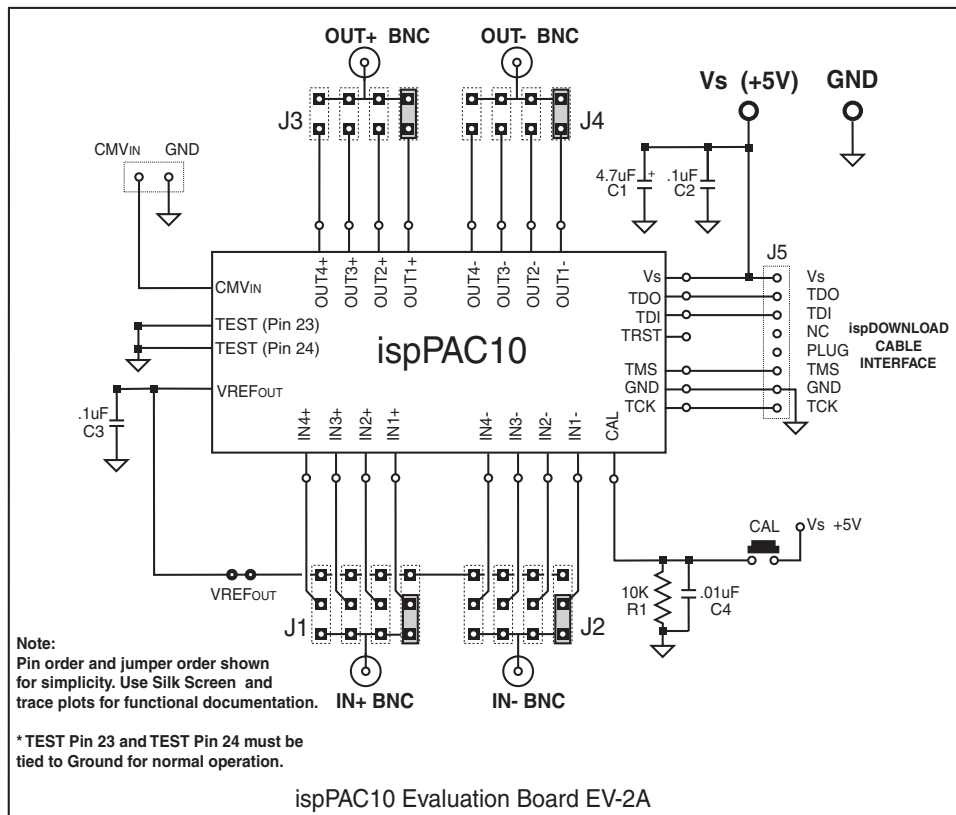
The ispPAC10 utilizes four programmable analog modules called PACblocks. Each of these PACblocks has differential instrumentation inputs and differential outputs. Each input and output is accessible to the user through BNC connectors and jumpers (Figure 3). The four JTAG programming signals have dedicated pins which are tied directly to the ispDOWNLOAD programming header J5. As an expansion feature, the programming interface signals, as well as all analog signals, are connected to dual rows with 34 pads for ribbon cable or board-to-board pins. Additional jumpers allow the user to tie any input to the internal "VREFOUT" common reference circuit. The board contains a momentary push-button switch that can be used to initiate a calibration. The calibration adjusts output offset and nulls the offset errors to a fraction of a millivolt.

Figure 1. ispPAC10 Evaluation Board EV-2A



ispPAC10 Evaluation Board ispPAC10EV-2A

Figure 2. ispPAC10 Evaluation Board EV-2A, Schematic Representation



Programming Interface

The ispPAC10 Programming Interface consists of the ispDOWNLOAD Cable that connects the PC Parallel Port DB-25 connector to an 8-pin connector header on the ispPAC10 Evaluation Board. The ispDOWNLOAD Cable contains a buffer circuit inside the DB-25 connector at the PC end. The cable is 6 feet in length and has an 8-pin flat receptacle at the board interface end.

Prototype Array

The board contains an array of 286 prototype holes that can be used for experimental evaluation and project interfacing. All inputs and outputs, as well as programming signals have connections to the 34-pin headers and through-hole pads located adjacent to the appropriate pins of the ispPAC10 device. Users can build additional analog circuitry in the prototype area and interface this with the ispPAC10 inputs and outputs.

Power Supply Considerations

A clean 5V supply should be used for the V_S supply. Decoupling and bypass capacitors are located on the

board near the ispPAC10 device. Two banana plug receptacles are available for V_S and Ground connections. A third pin is used when the optional CMV_{IN} reference voltage is externally supplied.

Jumper Connections

The Evaluation Board interfaces to a signal source or other test equipment through the BNC connectors. There are a pair of BNC connectors for the inputs and a pair for the outputs. The selection for input pins is made with Jumpers J1 and J2 (Figure 3). These jumpers tie the input BNCs to any input pin, and they can also be used to tie an input to the 2.5V reference pin VREFOUT. Figure 3 shows the input BNCs tied to IN1+ and IN1- through J1 and J2.

The output pins are routed to the output BNCs through Jumpers J3 and J4. These jumpers each select one of four output pins of the ispPAC10. Figure 3 shows the output BNCs tied to OUT1+ and OUT1- with Jumper Blocks J3 and J4.

ispPAC10 Evaluation Board ispPAC10EV-2A

Figure 3. Jumper Configurations for Inputs and Outputs

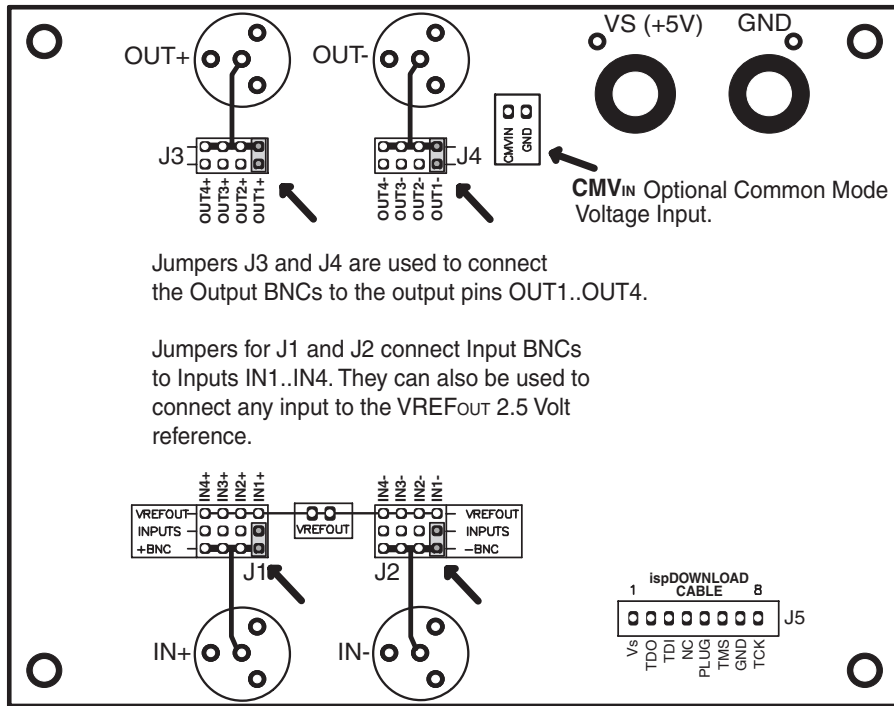
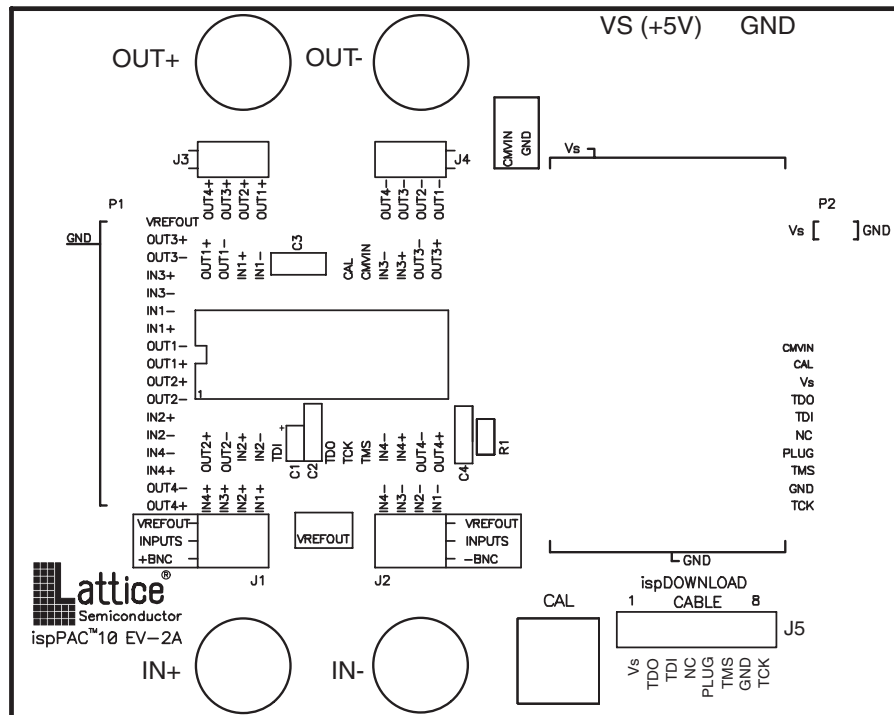


Figure 4. Silk Screen Top Layer



ispPAC10 Evaluation Board

ispPAC10EV-2A

Figure 5. PCB, Top Side (Bottom Side Traces Shown as Dotted Lines)

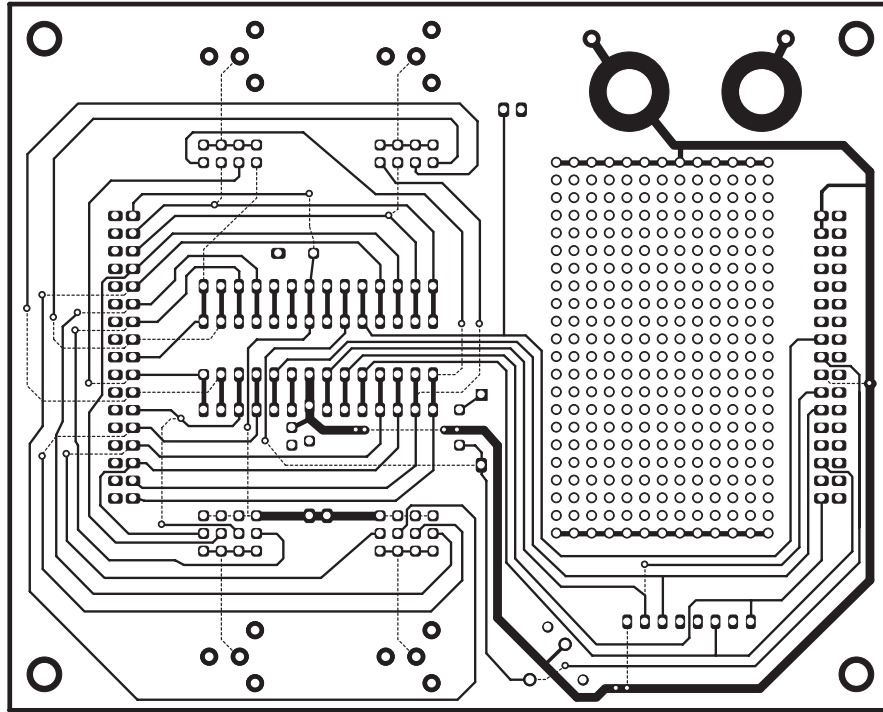
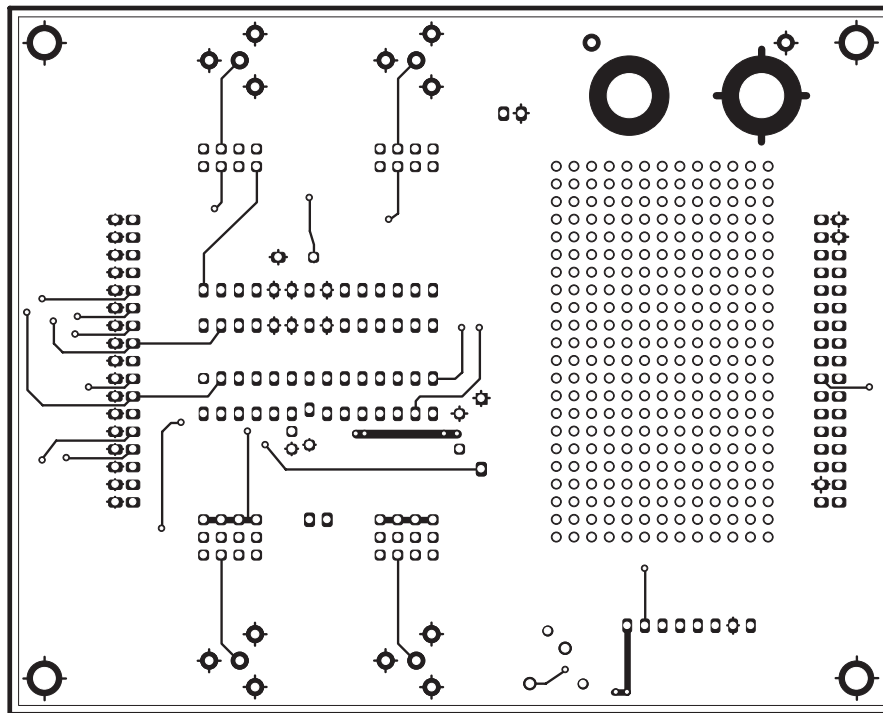


Figure 6. PCB, Bottom Side (Ground Plane Pour Not Shown)



Component List

- (1) PCB, (4.0 x 5.0") .063 FR4 with solder mask/silk screen
- (4) BNC connectors
- (2) 3 x 4 position jumper headers for inputs
- (2) 2 x 4 position jumper headers for outputs
- (1) 8-pin header for JTAG programming interface (J5)
- (1) Push-button switch (momentary, normally open)
- (2) Banana jacks for Vs and GND
- (1) .01uF capacitor (C4)
- (1) 4.7uF capacitor (C1)
- (2) .1 uF capacitor (C2,C3)
- (1) 10K Ohm resistor (R1)
- (1) 28-pin DIP socket
- (2) ispPAC10 28-pin DIP sample
- (4) Rubber bumper feet
- (4) Shorting jumpers

Technical Support Assistance

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