

Introduction

This application note describes how to use the ispPAC10 as a complete, differential analog front-end for an Analog-to-Digital Converter (ADC). The ispPAC10 will be used to amplify the output of a floating bridge, provide anti-alias filtering and drive the inputs of a 12-bit, differential input ADC. The ispPAC10 will also be used to develop the bridge excitation and reference for the ADC.

ispPAC10 Overview

The ispPAC10 contains four programmable analog modules called PACblocks and a programmable interconnect system. Refer to Figure 1 for the basic structure of the PACblock. Each PACblock contains a differential-output summing amplifier (OA) and two differential-input instrumentation amplifiers (IA) with excellent common-mode rejection and variable gains of ± 1 to ± 10 in integer steps. The OA's feedback path contains a resistive element that can be selectively used, as well as a programmable capacitor array that allows for more than 120 poles when the PAC device is used as an active filter. Thus, each PACblock has the ability to sum two differential signals with independently selectable gain and inversion settings and to act as a gain element (with the feedback switch closed) or as an integrator (with the feedback switch open). Cascading PACblocks can realize more complex circuits such as biquad and ladder filters. PAC-Designer[®], a Windows[®]-based design tool for the ispPAC10, includes software macros to speed the design of these more complex circuit functions.

The gain settings, feedback, capacitor values and interconnects between PACblocks are configurable through non-volatile E²CMOS[®] cells internal to the ispPAC10. The device configuration is set by software and downloaded to the device via an ispDOWNLOAD[®] cable.

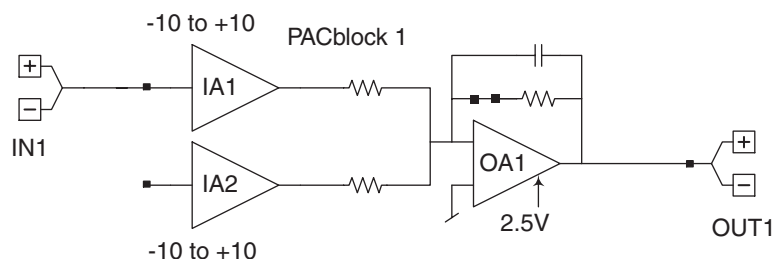
Differential Signal Processing

Most modern charge-redistribution ADCs are designed with a differential input stage. This differential input improves system accuracy by attenuating common mode noise and allows greater flexibility in the design of the analog front end (AFE). Many ADCs also offer differential reference inputs. This allows the reference to be derived from two voltage sources other than ground, further improving noise performance.

Transducers used to convert physical parameters (i.e., pressure, temperature, flow, etc.) to electrical signals often have differential outputs. It is desirable to process these output signals differentially to realize the inherent benefits of improved power supply rejection, increased signal to noise performance and ease of signal detection, as compared to a single-ended system. The low-level nature of transducer outputs often requires the use of an amplification stage to produce usable signal levels. Traditionally, an instrumentation amplifier with very high input impedance to minimize loading errors is used. Most instrumentation amplifiers convert the differential input to a single-ended output thereby sacrificing the benefits of differential signal processing and sampling. Digitizing a signal requires that the frequency components of that signal be known. A lowpass filter, or anti-alias filter is often used to band limit the input signal prior to data conversion.

The ispPAC10 uses a fully differential architecture from input to output, preserving the benefits of differential signal conditioning. It features instrumentation grade, differential input amplifiers ($10^9\Omega$ input impedance), a differential output, and all the necessary components to act as a complete, integrated analog front end providing gain and anti-alias filtering. In addition, the ispPAC10 has a stable, 2.5V bandgap reference on-chip that can be

Figure 1. PACblock Simplified Block Diagram



ispPAC10: Complete Interface for Bridge Sensor to 12-Bit ADC

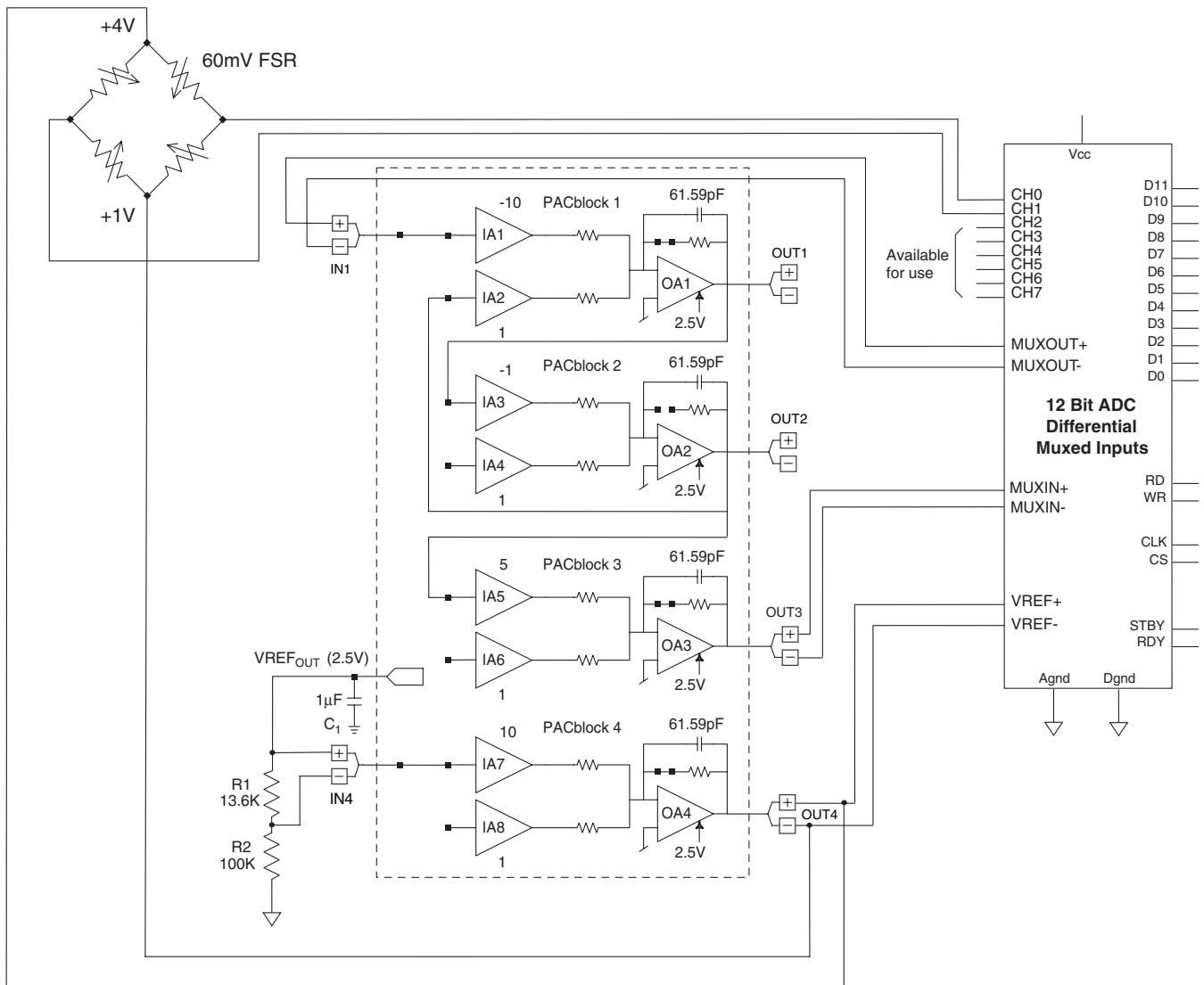
used to develop the reference source for the ADC as well as power the transducer. Driving the ADC and the transducer from the same reference source avoids many of the issues associated with variations due to temperature and time by forming a ratiometric measurement. Changes in the reference voltage are seen equally by the entire system and are canceled out when using this type of measurement technique.

Bridge Excitation and Reference Source

Figure 2 shows the ispPAC10 performing bridge excitation, differential, amplification and anti-alias filtering to form a complete AFE for a 12-bit ADC.

PACblock 4 and the internal reference are used to develop a stable 3V differential voltage centered at 2.5V. This differential voltage is used to drive the reference inputs of a 12-bit ADC, defining a 3V full-scale input range, and to provide excitation voltage for the bridge. The 2.5V reference output is divided externally to create a .3V differential input to PACblock 4. It is recommended that the series impedance of the divider be greater than 100kΩ to minimize loading effects on the internal reference. The .3V differential signal is amplified by 10 and is present at the outputs of PACblock 4. The outputs of any PACblock are capable of sourcing 10mA, more than sufficient to excite the bridge and drive the reference inputs of the ADC. Driving the bridge with this differential

Figure 2. Complete AFE for 12-Bit ADC



ispPAC10: Complete Interface for Bridge Sensor to 12-Bit ADC

voltage sets the output common mode voltage of the bridge to 2.5V. The bridge used in this example has an input impedance of 5000Ω and a full-scale output (FSO) voltage of 60mV when excited by a 3V source.

Signal Path Analysis

The output of the bridge is multiplexed to the inputs of PACblock 1 by using CH0 and CH1 of the ADC configured as a differential pair. The other input channels are available for use throughout the system. When the ispPAC10 is placed between the multiplexer and the ADC inputs as connected in Figure 2, all input signals experience the same gain and filter characteristics which minimizes channel-to-channel mismatch errors. If the system requires unique values of gain or unique filter characteristics for the other inputs, simply place the

ispPAC10 in series with the bridge output to allow separate gain or filter stages to be designed for each channel.

The inputs of PACblock1 have a typical input impedance of $10^9\Omega$ which makes the loading effects on the bridge negligible. The instrumentation amplifier of PACblock 1 is configured for a gain of 10 to amplify the bridge signal to 600 μ V full scale. PACblock 3 provides an additional gain of 5 so that the full-scale output applied to the ADC is 3V using the entire input range. The LSB size of the ADC is 732 μ V allowing detection of a 14.6 μ V change in the bridge output. Note that the fully differential architecture of the ispPAC10 allows both positive and negative inputs by supporting a 6Vpp dynamic range on a single 5V supply. Furthermore, PACblock 1 and PACblock 2 are configured as a second order biquad filter to attenuate alias products. A detailed application note (AN6003:

Figure 3. Gain Plot

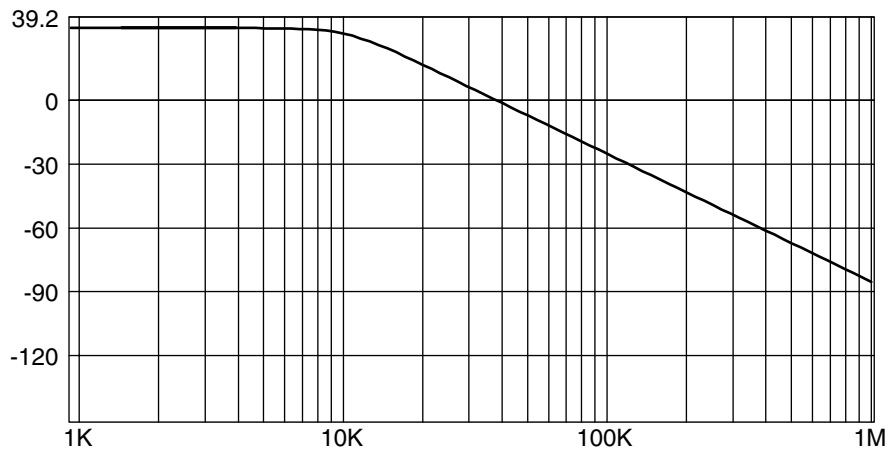
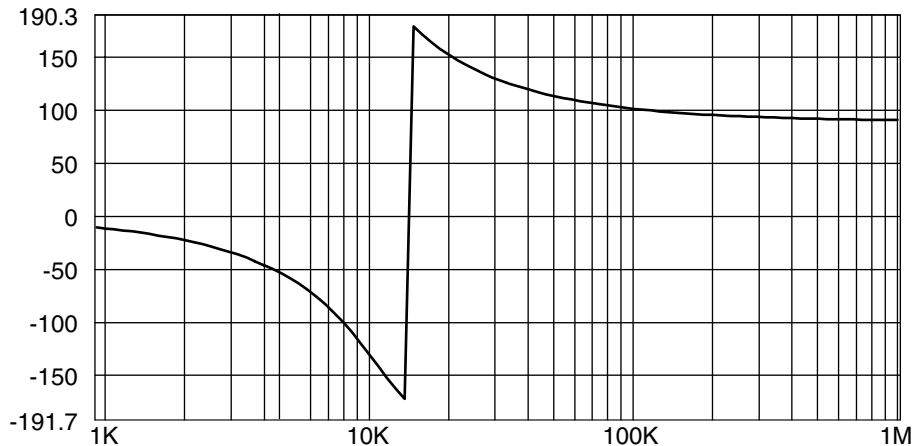


Figure 4. Phase Plot



ispPAC10: Complete Interface for Bridge Sensor to 12-Bit ADC

ispPAC10 Biquad Filter Implementation) discusses the specifics and the implementation of this filter topology using the ispPAC10 and PAC-Designer.

Performance Characteristics

PAC-Designer is a PC-based design tool used to program the ispPAC10. A user designs a circuit using a graphical interface and is able to simulate circuit response. When satisfactory results are obtained, the configuration parameters are downloaded to the ispPAC10 through an IEEE 1149.1-compliant serial port. More complex functions, such as the biquad filter used in Figure 2, are supported with a software macro tool included in PAC-Designer. A user chooses the filter's corner frequency, filter Q and pass-band gain and the filter generator designs the circuit. Simulated filter response is also calculated and graphically displayed by PAC-Designer to aid in circuit design.

The filter designed in this example has a corner frequency of 10kHz, pass-band voltage gain of 10 (20dB) and a filter Q of 1.0. The output of the biquad is amplified by PACblock 3, which also adds another pole at the corner frequency, improving the roll-off rate to 60dB/decade. Measured corner frequency accuracy is typically within $\pm 1\%$ of the simulated value. Figures 3 and 4 are the simulated response for gain and phase of the combined filter circuit designed in Figure 2.

Typical signal to noise performance (SNR) of the ispPAC10, when band limited to 10kHz, is 123dB, well below the quantization noise floor of a 12-bit ADC. Total harmonic distortion (THD) at an input frequency of 100Hz at a gain of 10 is typically 90dB. Dynamic performance characteristics at this level demonstrate the viability of the ispPAC10 for 12-bit applications.

Summary

The ispPAC10 represents a new level of flexibility in analog signal processing. This application note demonstrates the ispPAC10 as a bridge amplification stage, an anti-alias filter, a reference source and a bridge excitation source to act as a complete AFE for a 12-bit ADC. The ispPAC10 provides a high level of integration along with in-system programmability while maintaining the benefits of differential signal processing. The software design tools used to program the ispPAC10 contain powerful software macros that speed the design of an AFE as well as simulate the circuit performance.

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