

Introduction

This application note outlines the capabilities of the ispPAC[®]10 when used as a gain stage for differential analog signals. The ispPAC10 contains four programmable analog modules called PACblocks. Refer to Figure 1 for the basic structure of the PACblock. Each PACblock contains a differential-output summing amplifier (OA) and two differential-input instrumentation amplifiers (IA) with variable gain of ± 1 to ± 10 in integer steps. The OA's feedback path contains a fixed-gain element which can be switched in or out, as well as a programmable capacitor array that allows for more than 120 poles when the ispPAC device is used as an active filter. Each PACblock has the ability to sum two differential signals with independently selectable gain and inversion settings and to act as a gain element (with the feedback switch closed) or as an integrator (with the feedback switch open).

The gain settings, feedback, capacitor values and internal interconnects between PACblocks are configurable through nonvolatile E²CMOS[®] cells internal to the

ispPAC10. The device configuration is set by software and downloaded via a JTAG download cable. Refer to the ispPAC10 data sheet for more details on the specifics of the device.

Programmable Gain Steps

In normal operation, the gain of PACblocks can change in integer steps. If fractional gain settings are needed or if an application requires adjustment of gain in smaller step sizes than integers, the configuration in Figure 2 can be used. This configuration allows users to set the gain for each input in finer steps. An external voltage divider derives a small fraction of the input signal while maintaining its differential nature. This voltage is then amplified and fed to the summing amplifier to provide small attenuation or gain factors.

For this application, gain stages IA2 and IA3 are used to set the small-step gain. Since they can each be programmed for gain values up to ± 10 , a 100-step adjustment range results. The step value or increment is a function

Figure 1. A Single PACblock

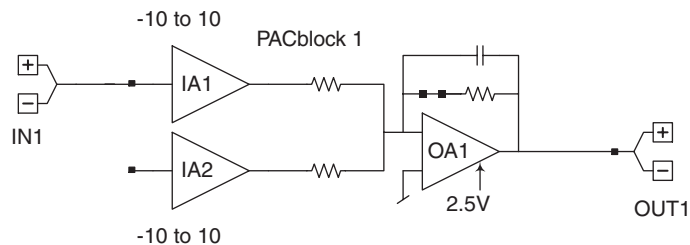
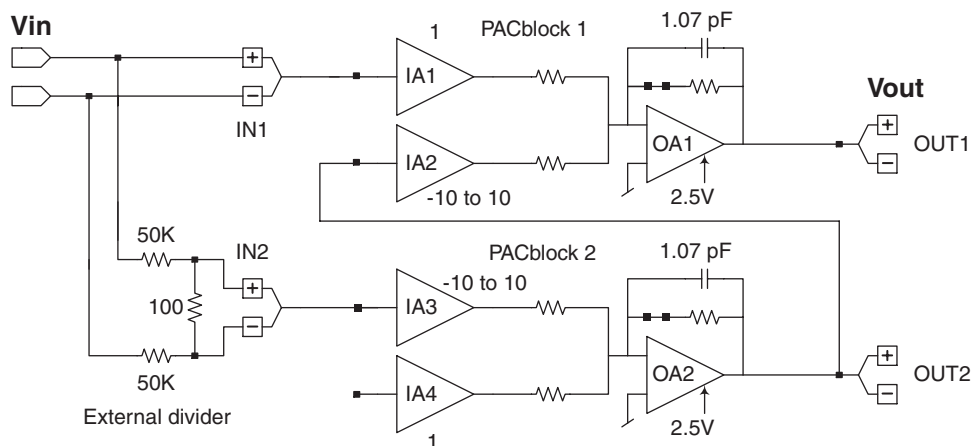


Figure 2. Two PACblock Fractional Gain Configuration



In-System Programmable Gain with Fractional Gain Adjustments

of the resistive divider multiplied by the gains of IA2 and IA3. For example, if an adjustment increment of 0.1% is required, the resistive divider factor should be 1/1000 and the total “gain trim” range becomes $\pm 10\%$. Or, for a 1% step size, change the divider factor to 1/100 and the range becomes $\pm 100\%$. In-System Programmability (ISP™) of the polarity and gain of the small-step gain stages provides the means for increasing or decreasing the circuit gain in small, precise steps.

The divider network values shown in Figure 2 demonstrate the 1/1000 ratio from the input signal, using values that add up to 100K ohms or more to reduce loading on the input. The resulting signal is fed through two stages, each capable of up to ± 10 gain factors (the IA3 stage of PACblock 2 and the IA2 stage of PACblock 1). The resultant signal is summed with the IA1 input stage signal. Note again that all inputs and outputs of the ispPAC10 are differential.

In this example, if the input were 1 Volt rms at V_{in} , the voltage divider network would result in approximately 1 mV rms across the 100 ohm resistor. Therefore the maximum gain adder at the summing node would be $\pm 100\text{mV}$, if IA2 and IA3 are each set to 10. Examining the transfer function for DC gain yields:

$$V_{out} = (V_{in} * IA1) + (V_{in} * IA3 * IA2 * K)$$

“K” represents the ratio value of the voltage divider network (1/1000, which can be easily changed to any other value). The ratio should be low enough that the small-step gain times the ratio is always less than one. Note that the external resistors are only needed for setting the fractional K factor, not to set the coarse gain.

As noted above, if more gain-adjustment range is needed, the 100 ohm resistor can increase in value, up to a maximum of 1.01K ohms (at which value the total adjustment range becomes $\pm 100\%$). Changing the resistor to 1.01K ohms increases the step size to 1%.

Gain Stages used (See Figure 2):

IA1 = ± 10 (Integer steps)

IA2 = ± 10 (Integer steps)

IA3 = ± 10 (Integer steps)

K = 1/1000

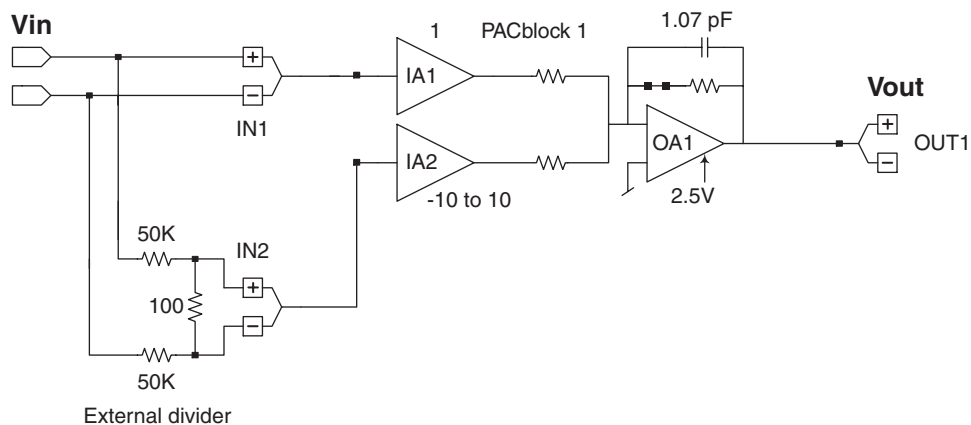
An alternate method to the one discussed above can be used if a small step adjustment with just ± 10 steps is required. Referring to Figure 3, the IA1 gain element sets the primary gain, and the incremental gain steps are set using IA2. The polarity of IA2 can be set to either attenuate or amplify by the small incremental value. The overall gain is a function of the divider network and the gain of the two IA stages. The 100-ohm resistor gives a $\pm 1\%$ adjustment range and a 1.01K resistor would give a $\pm 10\%$ range. Because only a single PACblock is used, three PACblocks are still available for other uses.

Equations:

$$V_{out} = (V_{in} * IA1) + (V_{in} * IA2 * K)$$

“K” again represents the ratio value of the voltage divider network, (1/1000 in this case), which can be easily changed to any other value.

Figure 3. One PACblock Fractional Gain Configuration



In-System Programmable Gain with Fractional Gain Adjustments

Integer Ratios

There is also an easy method of making fractional gains with no external components. Gains with integer ratios (such as 1/4, 2/3 or 3/2, etc.) can be accomplished by feeding back the output to the summing node of the OA through the second input amplifier. When the feedback switch is open so that the output is fed back only through the second IA, the gain is set by the ratio of the IA1/IA2 gain factors. For more information, refer to Application Note AN6008, *Gain Stages and Attenuation Methods*.

Summary

This application note shows how to achieve any gain value with various degrees of programmable range. Moreover, gains that are simple integer fractional ratios can be accomplished without an external divider network using the technique described in the “Integer Ratios” section of this document.

The flexible architecture of the ispPAC10 and its in-system programming capability allow analog designers options previously unavailable in standard analog systems. The capability to reconfigure device parameters such as gain, inversion and filter characteristics is easily attained using PAC-Designer® software. The ability to download to the device through a JTAG cable connected to the PC parallel port opens many new options during prototype and production. Because of this versatility, embedded solutions can also benefit from using the ispPAC10.

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