ispPAC®10 Gain Stages and Attenuation Methods

Introduction

This application note shows several techniques for obtaining gains of arbitrary value using the integer-gain steps of ispPAC10. It also explores ways to get attenuation from the ispPAC10. All of the techniques mentioned here are valid primarily for differential applications.

The ispPAC10 contains four integrated programmable analog macrocells known as PACblocks and a programmable interconnect system. Refer to Figure 1 for the basic structure of the PACblock. Each PACblock is composed of a differential-output summing amplifier (OA) and two differential-input instrumentation amplifiers (IA) with variable gains of ±1 to ±10 in integer steps. The OA's feedback path contains a resistive element which can be switched in or out, as well as a programmable capacitor array that allows for more than 120 poles when the ispPAC device is used as an active filter. Each PACblock has the ability to sum two differential signals with independently selectable gain and inversion settings and to act as a gain element (with the feedback switch closed) or as an integrator (with the feedback switch open).

The gain settings, feedback, capacitor values and internal interconnects between PACblocks are configurable through nonvolatile E^{2}CMOS® cells internal to the ispPAC10. The device configuration is set by software and downloaded via an ispDOWNLOAD® cable. Refer to the ispPAC10 Data Sheet for more detailed information about the device.

Normal Gain Settings

In normal operation, the gain of PACblocks can be changed in integer steps, from ±1 to ±10. This gain value is calculated from input to output, regardless of the fact that there are two gain blocks inside a PACblock, and placed adjacent to the appropriate IA in the schematic. For example, to obtain a gain of 4 from IN1 to OUT1 in Figure 2, set the gain of IA1 to 4. To obtain a gain of -4, set the IA1 gain value to -4.

An extension of this scheme can be made if you want a gain of up to and including 20 (see Figure 3). If IA2 is not otherwise going to be used in your circuit, the same input signal can be run to IA1 and IA2 in parallel. When their inputs are connected in parallel, the gains of IA1 and IA2 add. With both IA1 and IA2 set for gains of 10, the gains add to 20. In fact, this technique can be used to obtain any integer gain from 1 to 20, again, as long as IA2 is not otherwise going to be used.

Figure 1. A Single PACblock

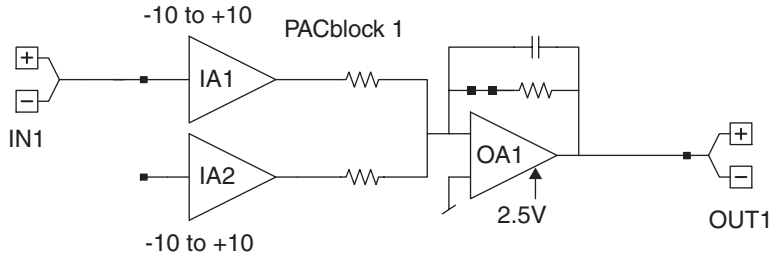


Figure 2. A Single PACblock with an Integer Gain of 4

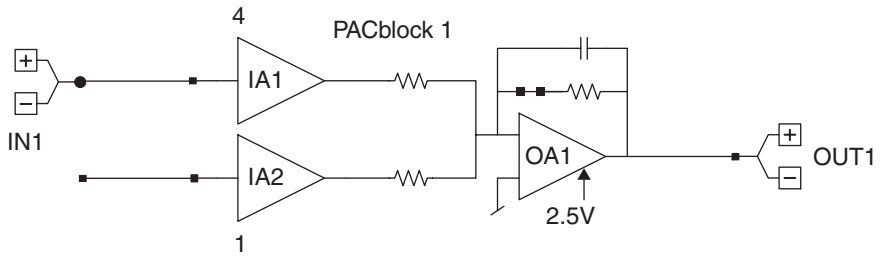


Figure 3. A Single PACblock with a Gain of 20

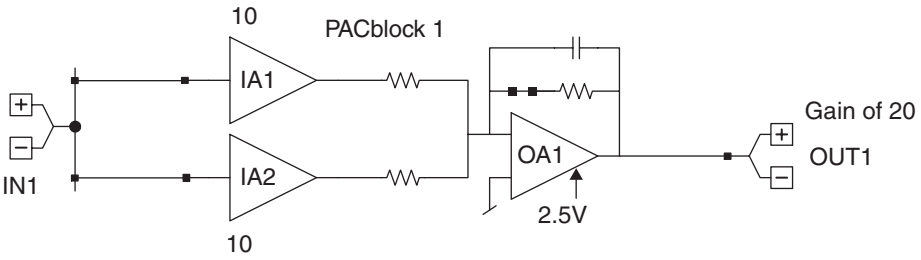
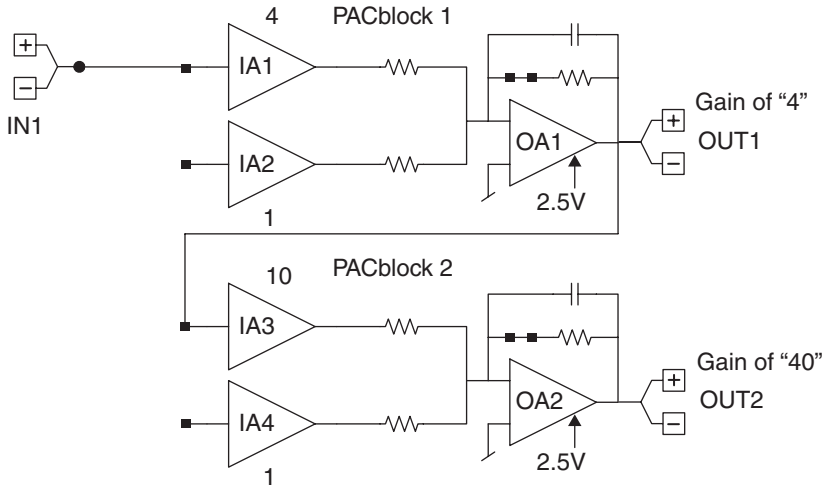


Figure 4a. Two PACblocks with a Gain of 40



There are many applications where IA2 will not be available for use in this manner, and a more conventional hook-up will be required to obtain gains exceeding 10. If the desired gain is >10 but ≤100, then a second PAC gain stage must be added in series. If the desired gain is >100 but ≤1000, then a third PAC gain stage must be added. When PACblocks are added together in series, their individual gains multiply. For example, to get a gain of 40, place two PACblocks in series and give the first a gain of 4 and the second a gain of 10 (Figure 4a). It is recommended to place the lower gain element first because the current-mode input amplifiers in the ispPAC10 do not have a significant increase in noise as their gains are increased, but their common-mode range improves as the gain is lowered. This is evident from Table 1 in the ispPAC10 Data Sheet. In fact, if a gain of 40 is needed, consider making the first stage have a gain of 2 and the second stage a gain of 20, for an even wider common-mode range (Figure 4b). As mentioned, there can be no other use of IA4 in Figure 4b if this configuration is used.

For a gain of 47, add a gain of 7 to a gain of 40. To do this, set up the gain of 40 as described above (series connections multiply gains), and use IA4 to add a gain of 7 from the original input (parallel connections add gains). Refer to Figure 5. Note that the Figure 4b scheme to obtain a gain of 40 cannot be used here because IA4 is needed to add a gain of 7 to the input. Note also that phase delays through the PACblocks may impact the effective gain at higher frequencies. The PAC-Designer® simulator gives a good estimate of the useful frequency range of an ispPAC circuit. For example, adding a gain of 7 to the gain of 40 does not affect the circuit's cutoff frequency (approximately 381 kHz), but it does introduce a slight phase lead which becomes noticable by about 1.5 MHz if both C_F capacitors are at their minimum values.

Figure 4b. Two PACblocks with a Gain of 40, Alternate Version

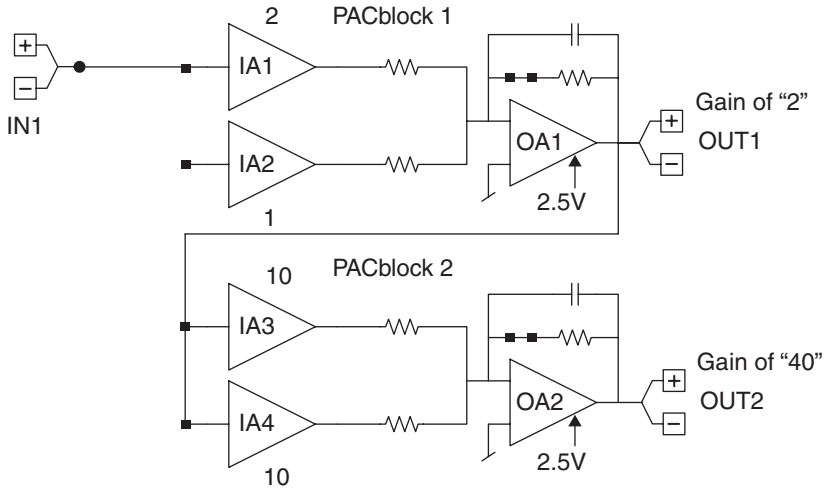


Figure 5. Two PACblocks with a Gain of 47

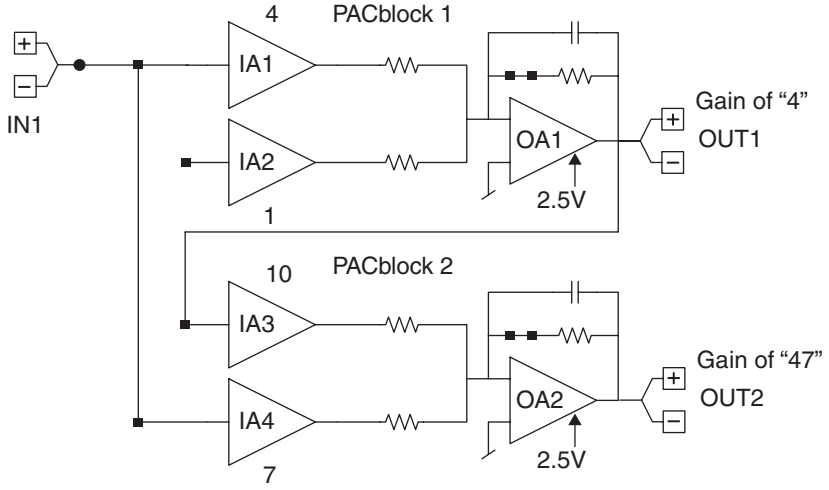
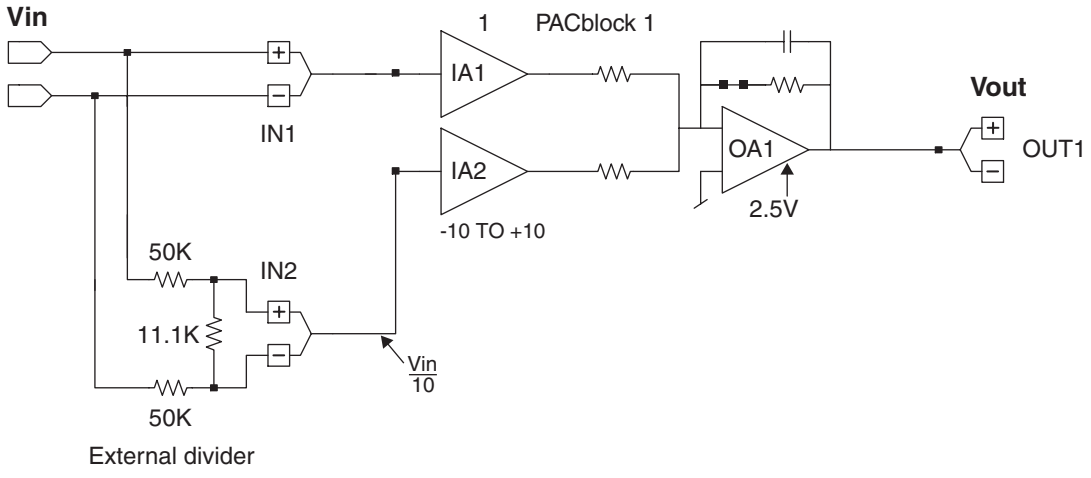


Figure 6. External Resistive Divider Permits Gain with Steps of 0.1



Fractional Gain Values, Part 1

If, instead, a gain of 40.7 is desired, begin with a gain of 40 and add an additional gain of 0.7 from input to output. There are two ways to add a gain of 0.7 to an ispPAC10 design. In the first of these, the input is divided by 10 to give (0.1 x Vin). This voltage is then amplified by 7 in another PACblock, giving a level of (0.7 x Vin). Using the technique of Fractional Gains covered in Application note number AN6007 *In-System Programmable Gain with Fractional Gain Adjustments,* an external resistor divider network is added to obtain Vin divided by 10. To avoid loading the input, use resistors whose values add up to 100 kΩ or more. Figure 6 shows two 50 kΩ resistors and an 11 kΩ resistor, resulting in a divisor of 0.0991, giving an error of approximately 0.9% if the resistors are accurate (the 11.1 kΩ resistor gives exactly a divisor of 10). The previously shown gain of 40 section has been left out to simplify Figure 6.

Integer Ratio Gains

An alternate method to obtain some gain factors smaller than unity, including all tenths values, is to use the Integer Ratio Gain technique. If the OA's feedback element switch is opened, IA1 and IA2 can be used to provide gains in the ratio of their gain values if IA2 is connected to the OA's output. Note that the gain of IA2 must be set to a negative number (-10 in this case) for this technique to work properly. To obtain a gain of 0.7, set IA1 to 7 and IA2 to -10. Figure 7 shows this connection. Refer to Table 1 for a list of all the gains available using this technique. The value of C_{F1} should be increased slightly if you discover that this circuit's small high-frequency peak is affecting the accuracy of the measurement. The default C_{F1} value is adjusted at final test to give a flat frequency response when the feedback switch is closed, and is generally a little smaller than the value needed if the gain of IA2 is set to -10. Use of this technique makes an external resistive divider network unnecessary and maintains the 1 x 10^9 Ω input impedance.

Figure 7. Integer Ratio Gain Technique Example

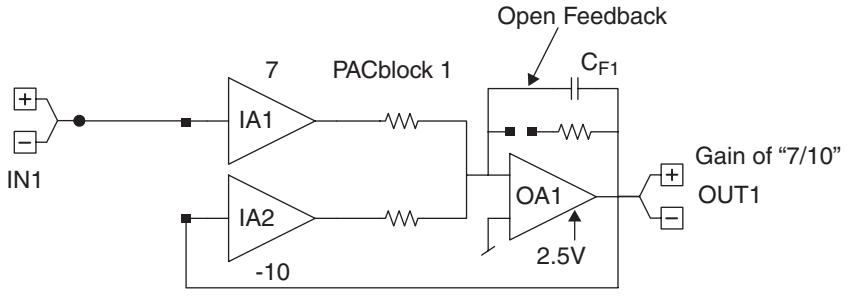


Table 1. Integer Ratio Gains Using IA2 as a Feedback Element (OA Feedback Switch Open). Note that "Gain" is IA1/IA2.

	IA1									
IA2	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
-1	1	2	3	4	5	6	7	8	9	10
-2	0.5	1	1.5	2	2.5	3	3.5	4	4.5	5
-3	1/3	2/3	1	4/3	5/3	2	7/3	8/3	3	10/3
-4	0.25	.5	.75	1	1.25	1.5	1.75	2	2.25	2.5
-5	0.2	0.4	0.6	0.8	1	1.2	1.4	1.6	1.8	2
-6	1/6	1/3	0.5	2/3	5/6	1	7/6	4/3	1.5	5/3
-7	1/7	2/7	3/7	4/7	5/7	6/7	1	8/7	9/7	10/7
-8	.125	.25	.375	.5	.625	.75	.875	1	1.125	1.25
-9	1/9	2/9	1/3	4/9	5/9	2/3	7/9	8/9	1	10/9
-10	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1

Fractional Gain Values, Part 2

If a “gain” of less than 1 is needed that is not found in Table 1 or is less than 0.1, then the resistive divider approach must be used to derive a smaller fraction of the input signal. Either divide by the exact number needed or divide by a convenient number and use the gain of a second PACblock to get the desired “gain” value. Application note number AN6007, *ISP Gain with Fractional Gain Adjustments*, shows how to obtain step sizes of 1% or 0.1% if a range of gain values is needed. For example, if you need a gain of 40.27, use the resistive divider approach to derive the input divided by 100 (Figure 8). Use a 1.0 kΩ resistor with two 50 kΩ resistors to get the desired (Vin x 0.01) value within 1%, or use a 1.01 kΩ resistor to give exactly (Vin x 0.01) if all resistor values are exact. Take the (Vin x 0.01) value and multiply it by 27 to get (0.27 x Vin), and then add the resulting voltage to the gain-of-40 stage. Note that Figure 8 has been simplified to primarily show the (Vin x 0.27) gain section. Two PACblocks in series can give gains of up to 100 times the (Vin x 0.01) signal. If a gain of only 10 or less times the (Vin x 0.01) signal is needed, then only one additional PACblock needs to be added. The gain accuracy of this scheme depends on the accuracy of the resistor divider network, with better accuracy being necessary for absolute gain matching at higher gain ratios. While this technique uses two PACblocks, it is an accurate method for obtaining fractional gains with the ispPAC10, and the gain values can be re-programmed in 0.01-unit steps without removing the PAC10 from its circuit board.

Summary

This application note shows how to configure the ispPAC10 for arbitrary gain values, even though the basic device has only integer gain steps. It also shows two ways to get gains of less than unity. The primary advantages of In-System Programmability (ISP™), including on-board re-programmability for gain, inversion and filter characteristics, enhance the functionality of these circuits. PAC-Designer software can be used to reconfigure the device from a PC or host microprocessor, downloading the design to the ispPAC device right on the circuit board. The flexible architecture of the ispPAC10 thus allows analog designers options previously unavailable in standard analog systems.

Technical Support Assistance

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Figure 8. External Resistive Divider Permits Gain in Steps of 0.01