

Introduction

This application note outlines the capabilities of the ispPAC10 device when used for interfacing to single-ended signals on both the input and output stages.

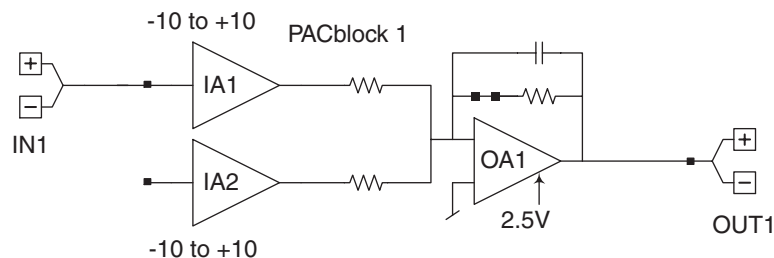
The ispPAC10 contains four programmable analog modules called PACblocks and a programmable interconnect system. Refer to Figure 1 for the basic structure of the PACblock. Each PACblock contains a differential-output summing amplifier and two differential-input instrumentation amplifiers with excellent common-mode rejection and variable gains of ± 1 to ± 10 in integer steps. The op amp's feedback path contains a resistive element that can be selectively used, as well as a programmable capacitor array that allows for more than 120 poles when the PAC device is used as an active filter. Thus, each PACblock has the ability to sum two differential signals with independently selectable gain and inversion settings and to act as a gain element (with the feedback switch closed) or as an integrator (with the feedback switch open).

The gain settings, feedback, capacitor values and internal interconnects between PACblocks are configurable through non-volatile E²CMOS[®] cells internal to the ispPAC10. The device configuration is set by software and downloaded to the device via a JTAG download cable.

Input Architecture

The ispPAC10 has eight differential instrumentation amplifiers. Both maximum input signal range and corresponding common-mode voltage range are a function of the input gain setting. The maximum input voltage times the gain of an individual cell cannot exceed the output range of that cell or clipping will occur. The maximum guaranteed input range is 1V to 4V, with an extended typical range of 0.7V to 4.3V for a 5.0V supply.

Figure 1. A Single PACblock



Differential Architecture

The architecture of the ispPAC10 is designed to best benefit differential signals on the input as well as the output. The four differential input pins can be interfaced directly to differential signals that are within the input limits. The input impedance for each input is $1 \times 10^9 \Omega$. The high input impedance is maintained regardless of the polarity or gain configuration of the instrumentation amplifier front end.

The input voltage levels range from 1V to 4V with the common mode normally centered at 2.5V. The output is also differential and is re-referenced to 2.5V regardless of the input common mode voltage. This value is based on an internal bandgap circuit that is used for the VREF_{OUT} pin. The value of the output common mode voltage can be set by applying a voltage to the CMV_{IN} pin. This pin allows the user to re-reference the output common mode voltage. The option to use the CMV_{IN} for each output pair is set using PAC-Desinger[™] software. When this function is not enabled, the differential output common mode uses the internal 2.5V reference.

Single-Ended Signal Interfaces

Single-ended signals may be connected to the ispPAC10 input and one-half of the differential output may be used to drive single-ended loads. So, in addition to fully differential input and output characteristics, either the input, output or both may be used in single-ended applications.

For systems that contain both single-ended paths and differential signal paths, the ispPAC10 can easily be used to interface to both types of circuits.

Using the ispPAC10 in Single-Ended Applications

Single-Ended Input

To interface the ispPAC10 differential input to a single-ended signal, one of the differential inputs needs to be connected to a DC bias, preferably the $V_{REF_{OUT}}$ signal, 2.5V. The input signal must be either AC coupled or have a DC bias equal to the DC level of the other input. Since the input voltage is defined as $(V_{IN+} - V_{IN-})$, the common mode level is ignored.

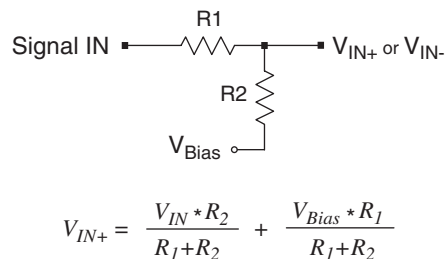
If the input signal level is near 2.5V, then it may be connected directly to the ispPAC10 input. If the DC level is not near 2.5V, a biasing circuit must be added to adjust the DC level to 2.5V. A simple resistive arrangement can be used to bias the signal to 2.5V (Figure 2). Note that the input signal is attenuated as shown in the equation.

For signals that are AC coupled, a DC bias of 2.5V for the ispPAC10 input is necessary. A simple bias network can consist of two resistors along with the capacitor used in the coupling circuit (Figure 3). This network forms a high-pass filter with a cut-off frequency of $(1/2\pi RC)$. The DC reference should equal $V_s/2$. $V_{REF_{OUT}}$ or an output from an unused PACblock can be used. When using the $V_{REF_{OUT}}$ pin, the resistors should be 100K Ω or greater. If using a PACblock output, they can be as low as 600 Ω .

Single-Ended Output

For applications that require single-ended outputs, simply use one-half of the differential output pair. The other output of the pair should be left open. The DC level of the output will be 2.5V if the optional CMV_{IN} pin is not used. If the load is not AC coupled, it will draw a constant current. Using one of the differential outputs halves the available output voltage swing (3V_{PP} versus 6V_{PP}). Since the output current is the same whether differentially or

Figure 2. Biasing Circuit

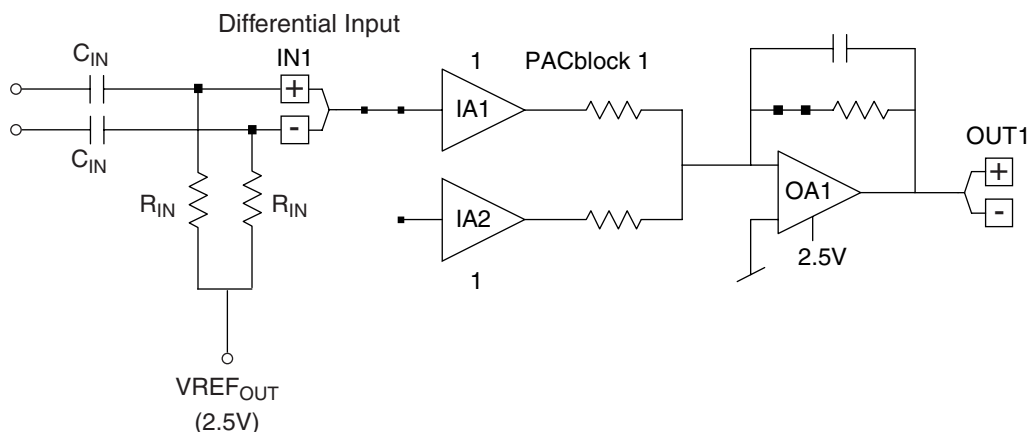


single-ended, a single output can drive twice the load as a differential output (300 Ω versus 600 Ω or 2000pF versus 1000pF). If the load requires DC current, the amount available for voltage swing is reduced. The output is capable of 10mA, so any DC current raises the minimum allowable load impedance.

When interfacing to other circuits using traditional op amps, it is easy to convert a differential output signal from the ispPAC10 to a single-ended signal with a standard Diff-Amp configuration shown in Figure 4.

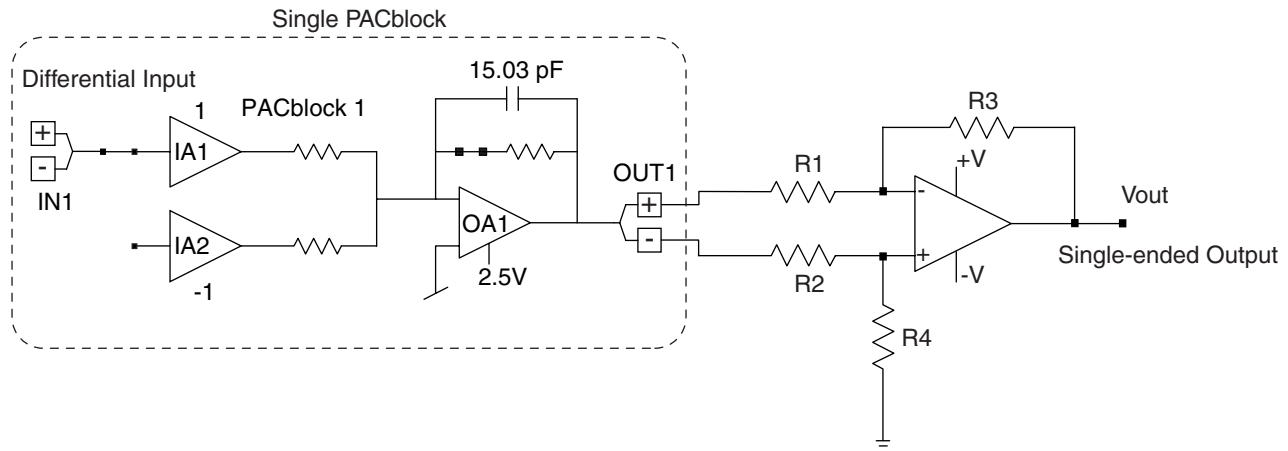
When the output is used single-ended there is some degradation in performance, primarily in output offset, PSR and THD. Because the architecture is differential, “common mode” offsets and errors are rejected by the architecture from input to output. When the output is used single-ended, common mode errors associated with the output stage cannot be canceled. The DC offset of either V_{OUT+} or V_{OUT-} has ± 15 mV variation about $V_{REF_{OUT}}$. Additional single-ended output performance characteristics are described in the specifications section of the ispPAC10 Data Sheet.

Figure 3. AC Coupled with 2.5V Bias



Using the ispPAC10 in Single-Ended Applications

Figure 4. ispPAC10 Driving Diff-Amp



Summary

The ispPAC10 differential architecture helps minimize noise associated with common mode signals. However, both differential inputs and differential outputs can be used with single-ended signals and still take advantage of the In-System Programmability (ISP™) of the ispPAC10 device.

The flexible architecture of the ispPAC10 and its in-system programmability provide designers with options previously unavailable in standard analog systems. The capability to reconfigure device parameters such as gain, inversion and filter characteristics after the device is soldered onto a circuit board is easily attained using PAC-Designer® software. The ability to download to the device through a JTAG cable connected to the PC parallel port opens many new options during prototype and production. Because of this versatility, embedded solutions can also benefit from the ispPAC10, where the device can be configured by a resident microprocessor.

Technical Support Assistance

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