

Introduction

The ispPAC Family of analog components from Lattice Semiconductor promises unsurpassed flexibility in many general-purpose analog signal-processing applications by bringing the concept of in-system-programmability (ISP™) to the circuit designer. Circuits are designed and simulated in Windows®-based, PAC-Designer® software and downloaded to the device to change characteristics as well as circuit topology in milliseconds—directly on the printed circuit board. In-system-programmability allows a designer to immediately evaluate design changes in solid state and allows field upgrades to be accomplished with installed hardware. Configuration data is stored in non-volatile E²CMOS® memory enabling a device to retain circuit designs while power is turned off. The configuration memory is accessible dynamically as well, to change circuit response and function, giving designers true in-system-programmability.

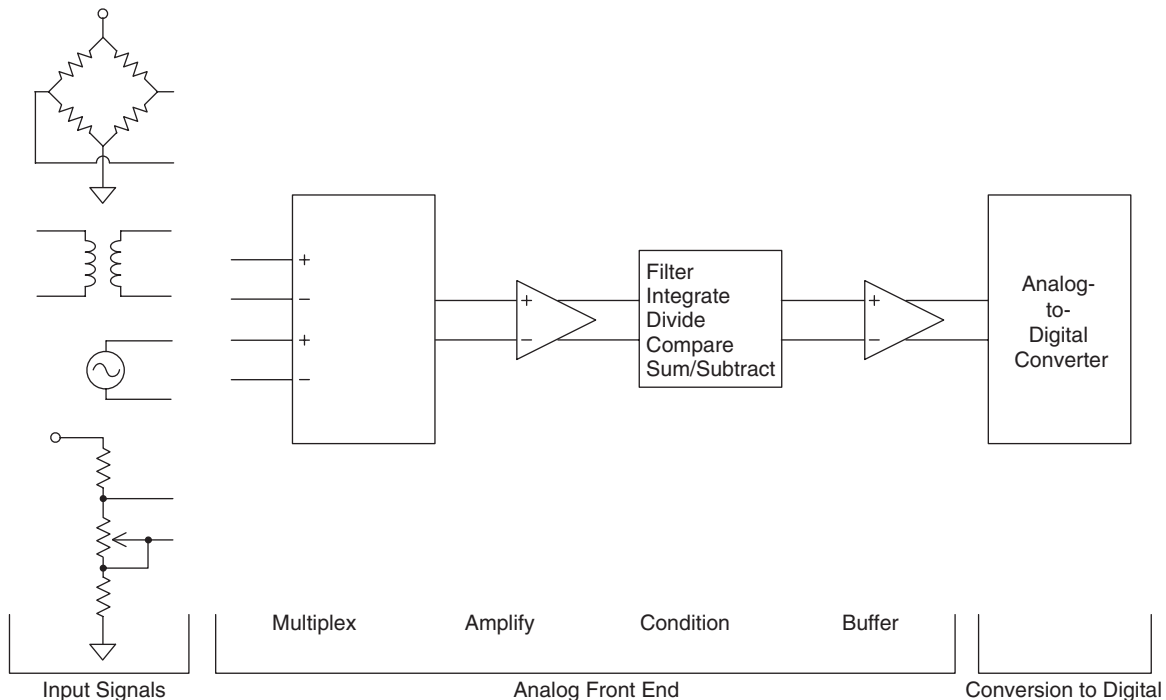
Analog building blocks with programmable characteristics replace traditional analog components such as op amps, active filters and comparators, eliminating the need for most external resistors and capacitors. Building blocks are internally connected through an analog rout-

ing pool that allows for the blocks to act independently or for cascading and paralleling of multiple stages. This application note describes the ispPAC20 and how it can be applied in analog front-end (AFE) design for analog-to-digital converters (ADCs).

AFE Signal Chain Analysis

The popularity of microprocessor-based systems has solidified the requirement of analog front-end design. Physical parameters under control or used as a transmission media must be digitized to be mapped in the discrete domain for processing. The process of converting a physical parameter to a digital representation consists of three distinct phases: input signal detection, signal conditioning (amplify, filter, etc.) and analog-to-digital conversion. Often, system requirements determine the specifications of the ADC and the choice of available, qualified transducers or the transmission media determines the signal detection requirements. It is the responsibility of the AFE to marry the often weak, noisy input signals to the full-scale range of an ADC while maintaining system accuracy. A block diagram showing some common analog signal conditioning functions of AFE design is shown in Figure 1.

Figure 1. Typical Circuit Functions in AFE Design



ispPAC20 Fills Many Roles as AFE for ADCs

AFE design requirements are often unique from one application to the next. Transducers used to convert physical parameters to an analog value have output signals with varied characteristics. For example, AFE designs in process control environments must take into consideration a transducer's output impedance, DC offset, signal magnitude and type (i.e., voltage, current, etc.), temperature and time dependencies, frequency components and common mode voltage, to name just a few. Add to this the choices of input range available when selecting an ADC, and it is apparent that AFE designs benefit when using components with a high degree of flexibility.

ispPAC20 Overview

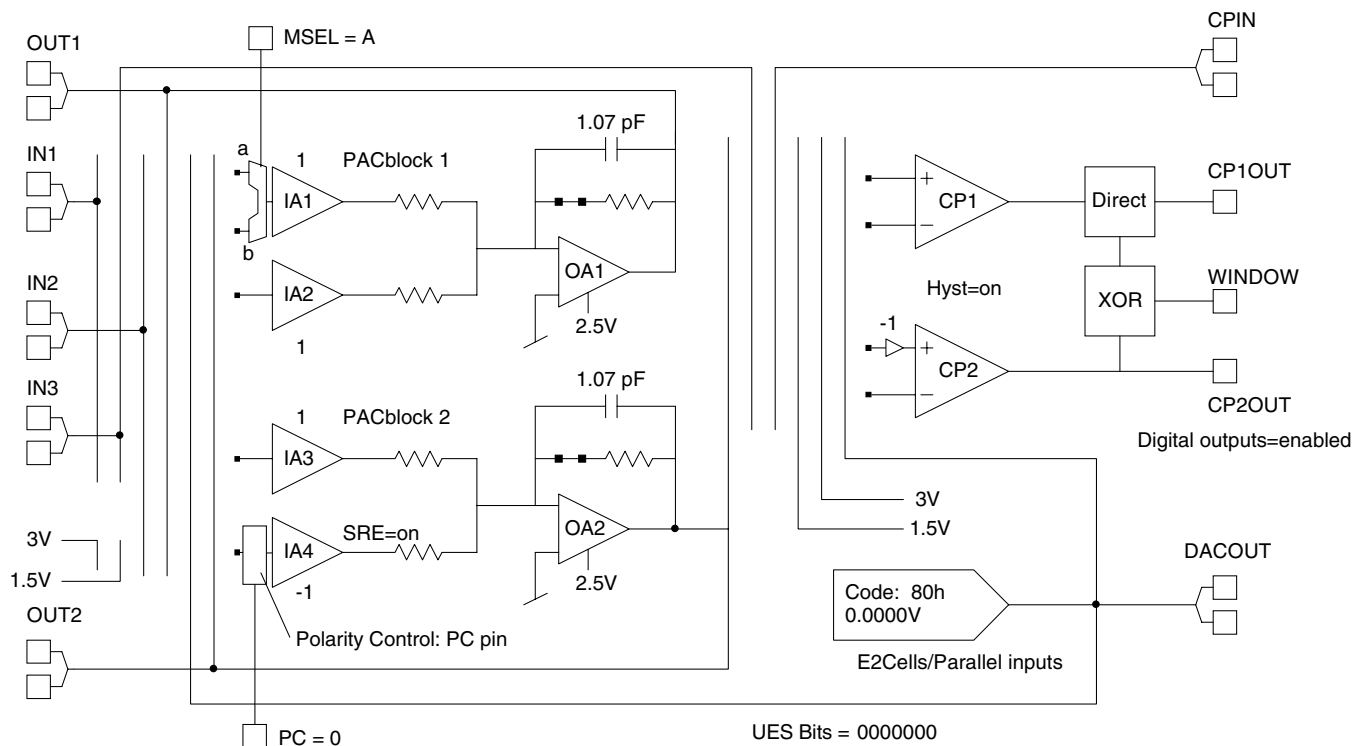
The ispPAC20 contains two general-purpose analog conditioning circuits known as PACblocks, an 8-bit Digital-to-Analog Converter (DAC), two comparators, a voltage reference, a two-channel multiplexer, auto-calibration circuitry and an analog routing pool that is used to connect the components internally. The design entry screen of the ispPAC20 (Figure 2) can be viewed as a simplified schematic of the device.

The ispPAC20 operates on a single 5V supply and is designed with a fully differential architecture from input to output. Inputs to PACblocks and comparators are differ-

ential, as well as the outputs of PACblocks and the DAC. Processing analog signals differentially realizes increased performance in signal-to-noise ratio, dynamic range and power supply rejection. Noise common to both inputs is greatly attenuated and dynamic range is effectively doubled given the bipolar nature of differential signals. Power supply variation effects are seen equally on both outputs, thereby preserving the signal's differential signal integrity. Transducers often output signals differentially to aid detection methods and many modern ADCs have differential inputs for many of these same reasons. This enables the ispPAC20 to condition a transducer output and drive the input to many ADCs directly in most applications, while preserving the benefits of differential signal processing. Single-ended inputs and outputs can also be accommodated with consideration given to the common mode voltage and gain settings of the design.

The components of the ispPAC20 can be connected internally through an analog routing pool. For example, the DAC output can be routed to the comparator inputs for setting a threshold such as an out-of-range or receive signal strength indicator or summed at one, or both, PACblock inputs to trim system offsets. Signals are connected to PACblock and comparator inputs through the analog routing pool with programmable polarity. The analog routing pool can be used to cascade PACblocks for higher order gains when digitizing low level transduc-

Figure 2. Design Entry Screen of ispPAC20



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ers or to provide higher order filter functions for alias protection. The non-volatile E² memory that configures the analog routing pool and circuit transfer characteristics can be accessed dynamically in embedded applications to vary circuit behavior “on-the-fly” or programmed once at board assembly.

ispPAC20 designs are entered, simulated and programmed with PAC-Designer, a Windows-based PC design tool. Designs are entered graphically using the keyboard and mouse or generated using a design macro utility. With macro-based design, the user enters desired circuit characteristics such as filter cutoff, Q and pass-band gain and PAC-Designer then generates the schematic. PAC-Designer simulates transfer characteristics of the PACblocks to aid the circuit designer. As many as four simulations can be displayed simultaneously for comparison. Once satisfied with simulated performance, the design is downloaded through a serial download cable that connects to the PC parallel port. The final, solid-state circuit is ready for prototype measurements. If a design requirement changes or a circuit response is not optimal, simply make adjustments in the design entry screen and click the download button.

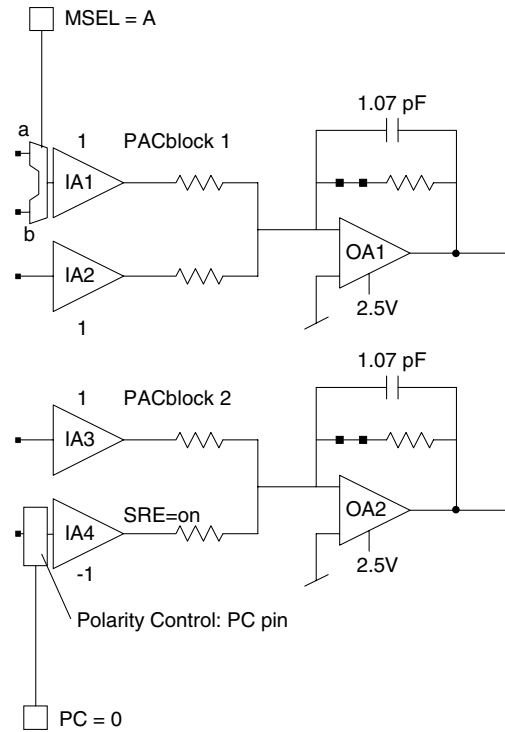
Component Overview

PACblocks 1 and 2

PACblocks 1 and 2 of the ispPAC20 are modeled in Figure 3.

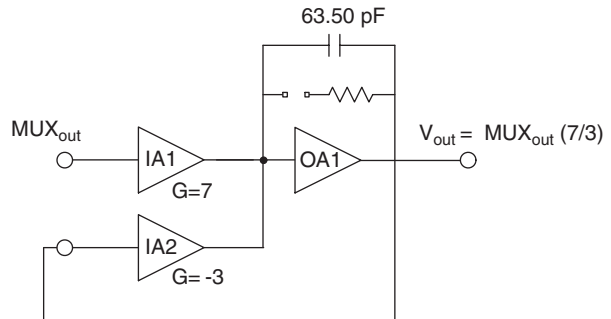
At the input of each PACblock are two, 10⁹ ohm input impedance, programmable gain instrumentation amplifiers (IA) that exhibit 69dB of common mode rejection (CMR). The gain range of each IA is ± 10 in integer steps. The outputs of the IAs are summed at the input of the output amplifier. The output amplifier has a user-programmable capacitive feedback element with 128 possible values over a range of 1pF to 64pF. The values have been chosen to optimize and concentrate pole spacing between 10kHz and 100kHz with 122 locations available. A minimum value of capacitance is set at the factory to optimize step response and limits the small signal bandwidth to 550kHz in a gain of 1. However, in a gain of 10 the typical bandwidth of a PACblock is 330kHz, giving a 3.3MHz gain bandwidth product. Because the PACblock is a composite amplifier comprised of three transimpedance amplifiers, bandwidth is not reduced in direct proportion to gain—a significant advantage of the PACblock architecture. More information on the PACblock architecture can be found in the theory of operation section of the ispPAC20 Data Sheet. The resistive feedback element of the output amplifier can be switched in or out to operate the PACblock as an integrator or as a

Figure 3. PACblock 1 and PACblock 2 of ispPAC20



gain block. Gain settings of the IAs are measured at the output of the PACblock and take into account the resistive feedback element switch being closed. Non integer gains are realized in a single PACblock by summing an amplified representation of the output voltage at the summing node and disabling the resistive feedback path. This method essentially uses the second IA of the PACblock to close the OA’s DC feedback path (Figure 4). When operating the PACblock in a fractional gain configuration, the polarity of the gain that determines the denominator must be inverted and the feedback capacitor should be maximized to improve stability. Please refer to application note number AN6008, *ispPAC10 Gain Stage and Attenuation Methods*, for more details on operating a PACblock in fractional gain.

Figure 4. PACblock 1 Configured in Fractional Gain Mode



ispPAC20 Fills Many Roles as AFE for ADCs

A two-channel multiplexer precedes the input to IA1 and a differential analog voltage inverter precedes the input to IA4. The multiplexers channel selection is controlled by an external pin (MSEL) while the inverter is controlled through the PC pin and other internal nodes in specific operating conditions.

The high input impedance of the IAs eases interfacing to low level, high impedance sources allowing a direct connection in many cases. With 10^9 ohm input impedance, PACblock inputs can be connected to a source impedance as high as $2.4M\Omega$ and still have less than one LSB of loading (gain error) in a 12-bit, 3V full-scale measurement. The input range of the PACblocks is $\pm 3V$ differentially with a common mode voltage of 2.5V (the internal reference voltage) which is also the default common mode output voltage. The output common mode voltage of either PACblock, however, can be independently set externally for increased flexibility. The output range of the PACblocks is $\pm 3V$ differential and capable of sinking or sourcing 10mA. The outputs remain stable ($< 3\%$ overshoot) with capacitive loads up to 700pF and settle to 0.1% to a 6V differential step in 4.0 μ s. This is ideal for driving many of the single 5V differential input charge balancing ADCs available on the market today. If the ADC input is truly differential and bipolar, a 6V_{pk-pk} dynamic range is realized on a single 5V supply when driving the ADC with a PACblock (i.e., $\pm 3V_{pk}$ differential = 6V_{pk-pk}).

The two PACblocks of the ispPAC20 can be cascaded to form a biquadratic filter. In this configuration a two-pole,

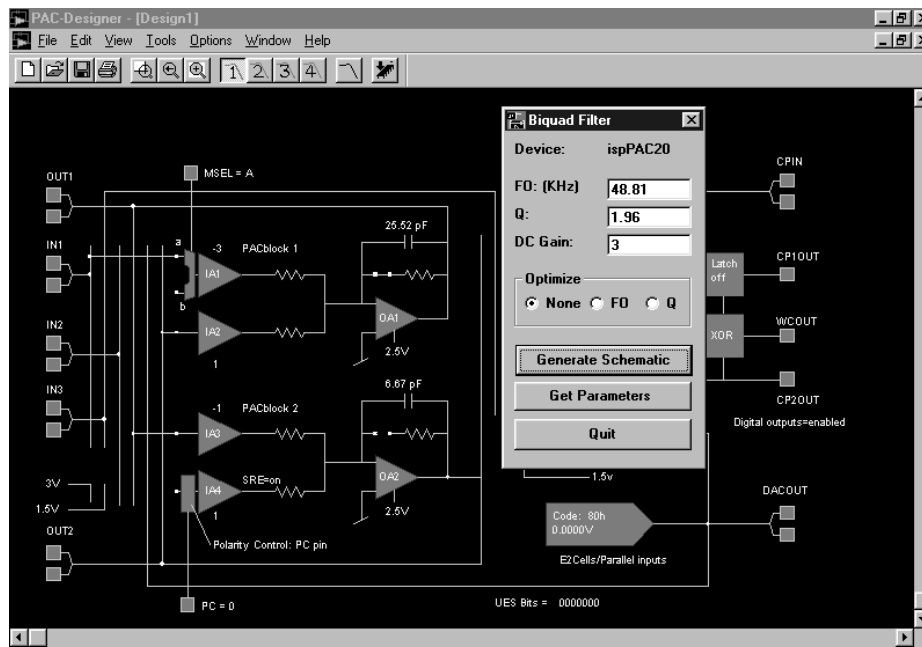
low pass filter with a corner frequency between 10kHz and 100kHz can be realized. PAC-Designer contains a software macro utility that aids the design of biquadratic filters. The user specifies filter characteristics and PAC-Designer generates the schematic design. Given that the capacitor and gain settings of the PACblocks are finite the user has the choice of having PAC-Designer optimizing the filter Q or gain when making calculations. The Biquad design entry dialog box is shown in Figure 5.

For more information on biquadratic filters please refer to application note number AN6003, *ispPAC10 Biquad Filter Implementation*.

The DAC

The ispPAC20 includes an 8-bit, differential voltage output DAC. The output of the DAC is available to all PACblock and comparator inputs through the analog routing pool and externally at the DAC output pins to source or sink up to 10mA. The DAC output has a 6V range ($\pm 3V_{pk}$ differential) resulting in an LSB size of 23.4mV and a common mode voltage of 2.5V. The DAC is guaranteed to be monotonic (DNL ≤ 1 LSB max) and has less than 0.5LSBs of INL. The DAC will settle within 0.1% in 6.0 μ s typically to a full-scale code transition. The combination of resolution, range and speed allow the DAC to correct for large system offsets at the AFE or for finer error calibration applications. One application of the DAC might have it drive the reference inputs of an ADC and power a transducer simultaneously, forming a ratiometric monitoring circuit. Using the DAC in this

Figure 5. Biquad Filter Macro Design Entry



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manner while using the PACblocks for adjustable gain and signal conditioning forms a complete AFE in many cases. The DAC input is set from either an E² memory address, which retains the setting during a power cycle, or can be dynamically changed through the JTAG/SPI compatible data I/O port. A complete description on the modes of operation for the digital I/O of the DAC is contained in the ispPAC20 Data Sheet.

In an AFE design, the DAC plays a critical role by giving the user the ability to null offsets or set thresholds at the comparator inputs acting as an adjustable reference source. The DAC can also be used to drive the reference inputs of an ADC to form a digital gain trim circuit. Data from the ADC can be analyzed by the microprocessor and the DAC used for error correction purposes. Circuit conditions such as an out-of-range input signal or receive signal strength indication can be detected and compensated for in-system by the processing intelligence.

The Comparators

The ispPAC20 has two double-differential input, 150ns voltage comparators. Input offset voltage is typically 5mV and the user has the option of adding 47mV (two LSBs of the DAC) of hysteresis at the inputs. The non-inverting input of CP2 has an analog voltage inverter, so that if a +1V differential signal is applied to the input, a -1V differential signal will be used for comparison purposes. This inverter makes deriving a window comparison from a single reference source possible. On the output of CP1 is a register that is clocked with the PC pin or can be bypassed. The outputs of CP1 and CP2 can be exclusive OR'd to complete the window comparison function or used to drive the S and R inputs of a flip flop. This logic functionality can be applied in an AFE design to set system alarms, trigger an AGC change, synchronize digitization to a circuit event or for out-of-range indications. A description describing the comparators modes of operation and interactions with the polarity inverter at IA4 is contained in the ispPAC20 Data Sheet.

The comparator inputs can be set with the DAC, a PACblock output, to a +3V or +1.5V reference point or externally by the CPIN pins. If using an external signal, it is important to be aware of the differential properties of the comparator inputs. The magnitude and polarity of the differential signal applied to each of the inputs determines the output of the comparators. For example, if a +1V differential signal is applied to the non-inverting input of CP1 and a -3V differential signal is applied to the inverting input the output will be high (logic '1'). If the polarity of the input applied to the inverting input is reversed, either internally or by switching connections of the CPIN pins, the output will be low (logic '0'). The input

range of the comparators includes both rails. The comparator inputs reject common mode voltages and only compare the magnitude and polarity of the differential voltage applied to the inverting and non-inverting inputs.

AFE Examples

Figure 6 shows the ispPAC20 applied in an AFE design for two DC signals. The inputs are multiplexed to the input of IA1 under microprocessor control. The selected signal will be amplified as determined by the gain setting of IA1 and the gain setting and input connection of IA2. A single PACblock can realize 73 different gain settings (Figure 6a). OA1 drives the input of IA4 through the polarity inverter, which is under the control of the PC pin, and the non-inverting input of CP2. The signal will experience another gain, as determined by the setting of IA4 and connection and setting of IA3 with, again 73 possible values. The total gain the selected input signal experiences is a multiple of the gain of PACblock 1 and PACblock 2 with over 2,500 unique values. The large number of unique gain settings benefits the user by allowing the ispPAC20 to be applied to a wide range of input sources. When used to amplify DC signals, the capacitive feedback element should be set at the maximum value to minimize noise and increase stability to step changes experienced when selecting input channels. OA2 drives the inputs of a pseudo-differential input ADC and CP1's non-inverting input. The DAC drives the reference inputs of the ADC and the inverting input of CP1. The output of CP1 will go high when the ADC input exceeds the full-scale range as determined by the DAC. This can signal the microcontroller to adjust the reference input by adjusting the DAC until the over range condition is eliminated or to program the PACblocks to a different gain setting.

A fair number of differential input ADCs on the market today have what are known as pseudo-differential inputs. The digitized signal is the difference between two input voltages, but in many cases the non-inverting input is not allowed to be negative relative to the inverting input and still produce usable data. Another way to think of this is that the ADC's differential input range is unipolar. The polarity inverter under control of the PC pin can be used to create a bipolar input range for such ADCs, effectively doubling the dynamic range. The output of OA1 is compared to 0V by CP2 to indicate when a change in polarity has occurred at the input. This indication is used to invert the signal using the polarity inverter at the input of IA4. In this configuration, the ADC can be used to digitize the magnitude of the differential signal and the output of CP2 can be used as a sign bit. A 12-bit ADC can be used to digitize a bipolar differential input to 13-bit resolution. The

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Figure 6. ispPAC20 AFE Design for Two DC Input Signals

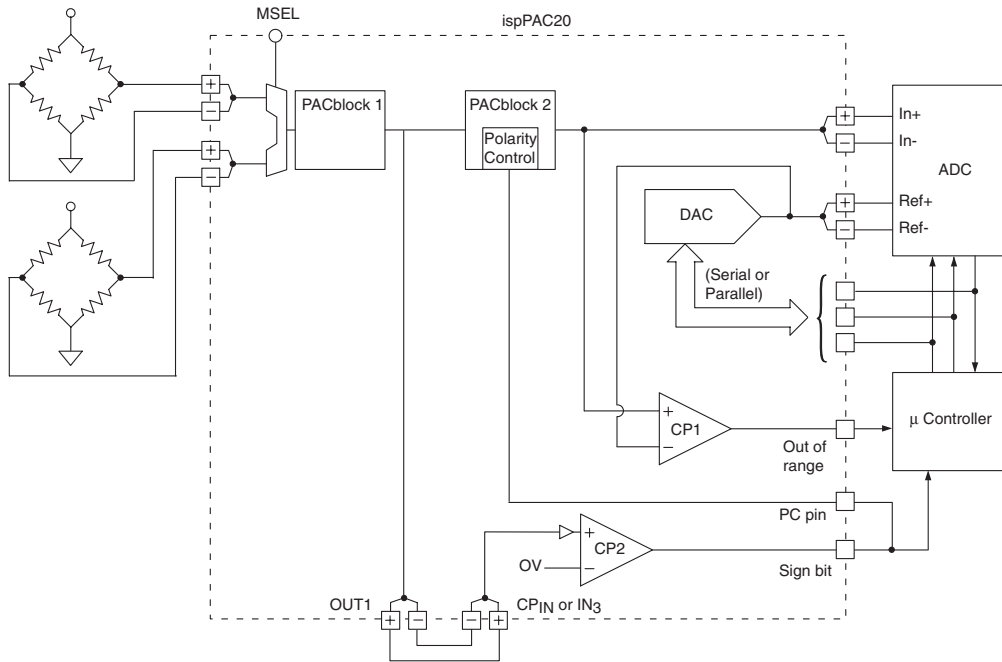
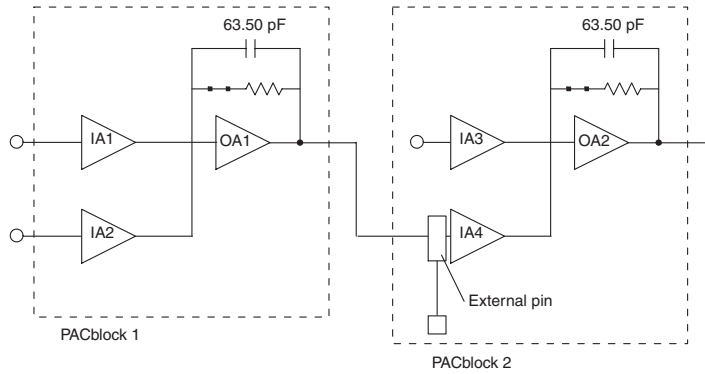


Figure 6a. PACblock Gain Setting Connection Diagram



PACblock Connection Diagram			
Gains Available	1, 2, 3, 4, 5, 6, 7, 8, 9, 10	11, 12, 13, 14, 15, 16, 17, 18, 19, 20	21, 22, 23, 24, 25, 26, 27, 28, 29, 30 Note: Feedback IA gain setting must be negative 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, 1/8, 1/9, 1/10 2/3, 2/5, 2/7, 2/9 3/2, 3/4, 3/5, 3/7, 3/8, 3/10 4/3, 4/5, 4/7, 4/9 5/2, 5/3, 5/4, 5/6, 5/7, 5/8, 5/9 6/5, 6/7 7/2, 7/3, 7/4, 7/5, 7/6, 7/8, 7/9, 7/10 8/3, 8/5, 8/7, 8/9 9/2, 9/4, 9/5, 9/7, 9/8, 9/10 10/3, 10/7, 10/9

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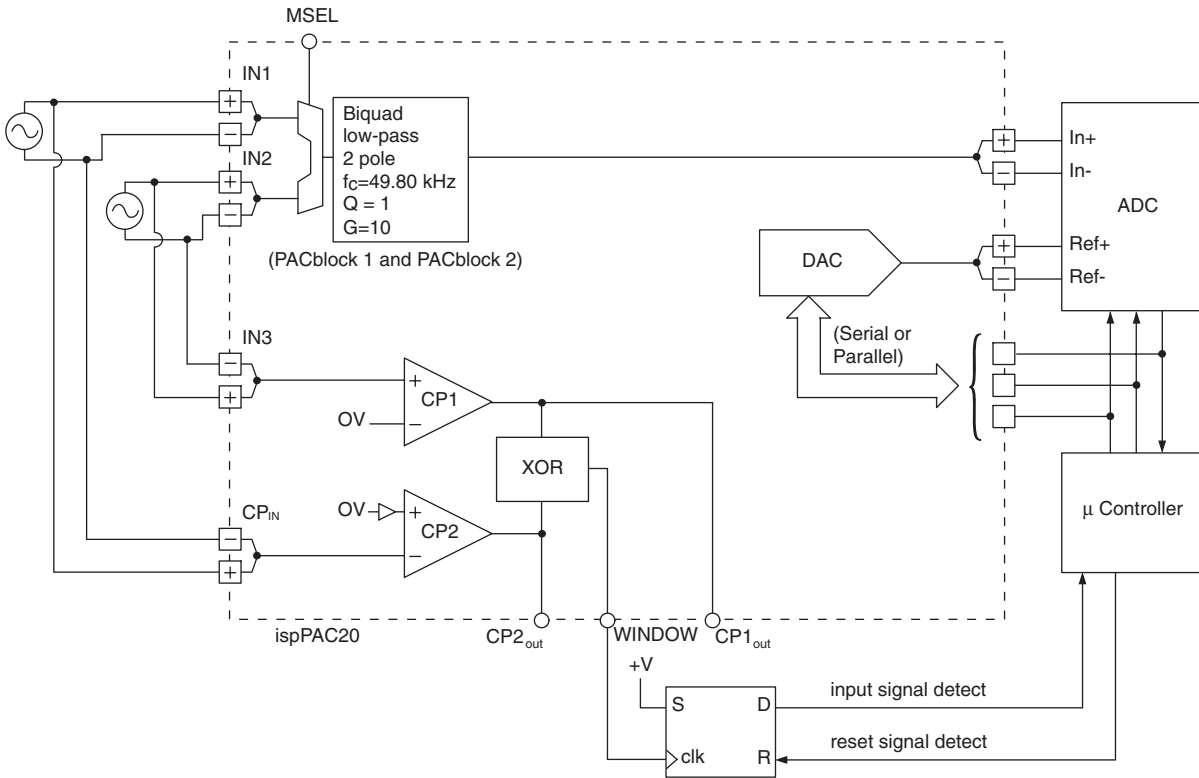
Table 1. Coding Scheme for Figure 6

Analog input	Binary output		Hexadecimal output	
	sign bit	ADC output	sign bit	ADC output
+ Full Scale	0	111111111111	0	FFF _H
⋮				
+ 1 LSB	0	000000000001	0	001 _H
Bipolar Zero (BPZ)	0	000000000000	0	000 _H
- 1 LSB	1	000000000001	1	001 _H
⋮				
- Full Scale	1	111111111111	1	FFF _H

resultant coding scheme of this circuit when using an ADC with a unipolar straight binary output is shown in Table 1. An ADC with a pseudo-differential input and a differential reference input that can be used in this manner is Linear Technology's LTC1296. The design can be modified to accommodate ADCs with a pseudo-differential input and single-ended reference inputs by using the DAC as a single-ended output. This will affect the out-of-range indication reference level.

Figure 7 shows the ispPAC20 used as an AFE digitizing two AC signals. The inputs are applied to the multiplexer preceding IA1. The microcontroller controls which channel is applied to PACblock 1 and PACblock 2, which are configured as a 2-pole low-pass filter for alias protection at the ADC input. The filter in this example is designed using the biquad software macro included in PAC-Designer with a corner frequency of 49.80kHz and a filter Q of 1. The gain of the pass-band is 10. The biquadratic filter designed in Figure 7 is detailed in Figure 8. It is

Figure 7. ispPAC20 AFE Design for Two AC Input Signals

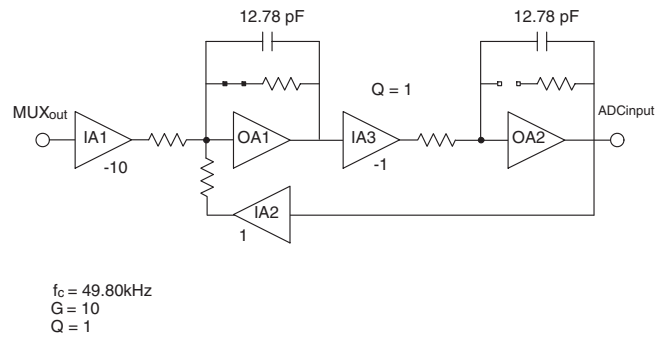


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possible to store multiple filter configurations in system memory and reconfigure so each input channel experiences unique characteristics. The output of the biquad drives the ADC inputs directly. When implementing such a design, it is important to select an ADC that has a bipolar differential input range. One such ADC available with this type of input is the National Semiconductor ADC12048. The DAC is used to set the input range of the ADC and can be adjusted by the processing intelligence for optimal performance.

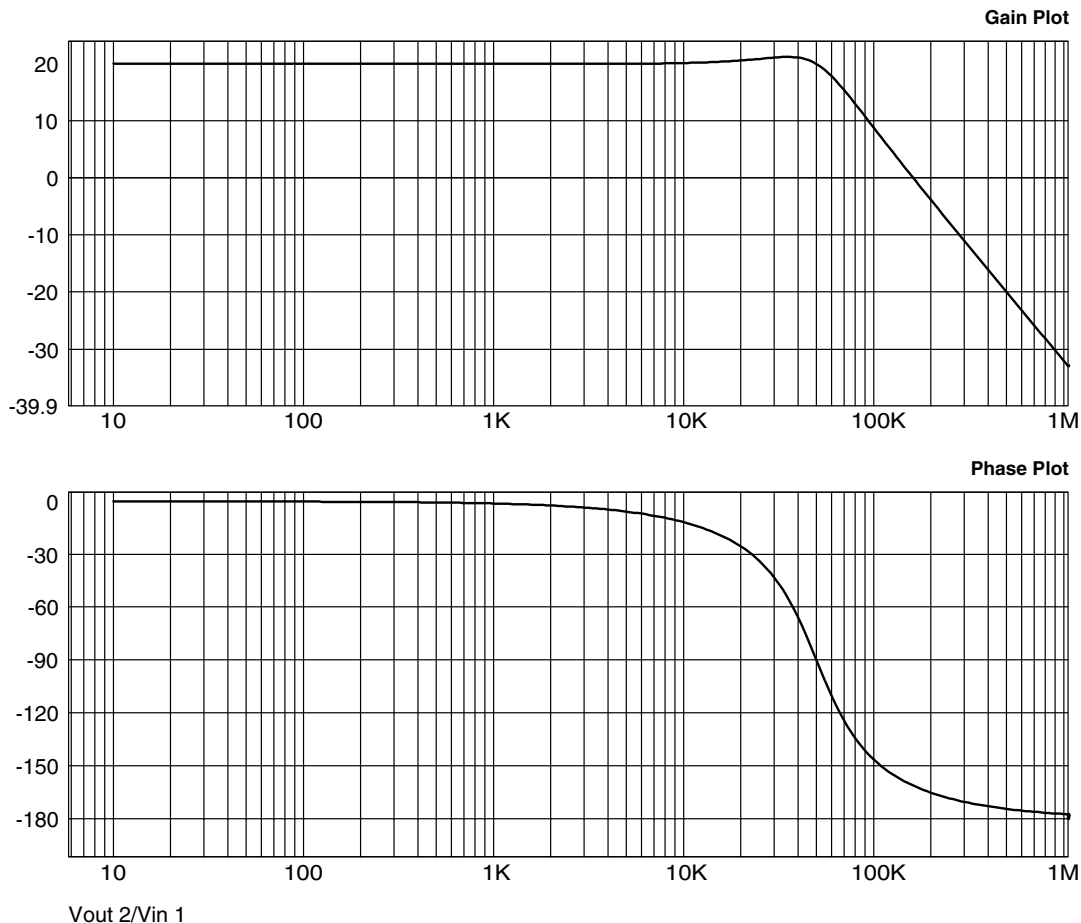
Both input signals are routed separately to the comparators. The comparators are used with external logic to indicate to the microprocessor when an input signal is present. The threshold for both comparators is 0V. Any signal on either input, regardless of common mode voltage, will cause a transition at the output of the window comparator and in turn sets the external register. The exclusive OR function of the ispPAC20 can be used to set the register if the signals vary in amplitude, phase or frequency. If the signals are identical and coincident, the output of the comparators can be OR'd and used to set

Figure 8. Biquad Filter Design Detail of Figure 7



the register. It is recommended to operate the comparators with the hysteresis turned on to avoid oscillations. The register output is used to signal the processor to initiate a data acquisition cycle. The processor can then poll CP1 and CP2 to determine which channel is present or perform a conversion on each channel and analyze the data. When polling the comparator outputs, it may be necessary to poll each output multiple times to determine

Figure 8a. Simulated Gain and Phase of PACblocks in Figure 8



which input signal is present. This is because the output of each comparator will be a '1' for only half of the input cycle. The processor resets the register when the acquisition cycle is complete and waits for the next input occurrence. This way, the processor can perform other system tasks and be alerted when an input channel requires digitizing. This saves valuable processing time by negating the need to continually monitor the input channels.

Conclusion

AFE design is a requirement in today's world of microprocessor-based systems. It is just as assured that the design of an AFE will have many variables. The ispPAC20 has been shown to be well suited to accomplish many of these designs. It contains many of the analog building blocks used today to implement an AFE design in discrete form. The analog routing pool and variable device characteristics allow a designer to accomplish these designs in an integrated package improving on reliability (integrated caps are much more reliable than their discrete counterparts) while dramatically reducing the design/prototype cycle time. Designs are realized in final silicon and are ready for characterization in seconds as opposed to days. In-system programmability also offers advantages in upgrading equipment installed in the field and in realizing adaptive systems. Device settings are stored on-chip in non-volatile E² memory, allowing configurations to be retained during a power cycle and eliminating initialization requirements. The easy-to-use software package aids the circuit designer by combining a fast, flexible design environment with simulation and programming capabilities without leaving the PC. Differential signal processing offers advantages in performance areas such as increased dynamic range, improved noise immunity and increased power supply rejection. The combinations of faster design time, improved reliability and increased performance make the ispPAC20 an excellent choice for AFE design.

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