

Introduction

The Lattice Semiconductor Corp. ispPAC20 In-System-Programmable Analog Circuit allows designers to build analog circuits such as gain stages, active filters, DAC functions and comparator functions without the use of external feedback resistors or capacitors. This technology brings In-System Programming (ISP™) to the analog world. Device functionality as well as parameters such as gain, comparator threshold, DAC output values and frequency response can be set by the user and changed on-the-fly by reprogramming the device. A standard JTAG IEEE 1149.1 interface allows the user to reconfigure the ispPAC20 while in-system using on-chip non-volatile E²CMOS[®] technology.

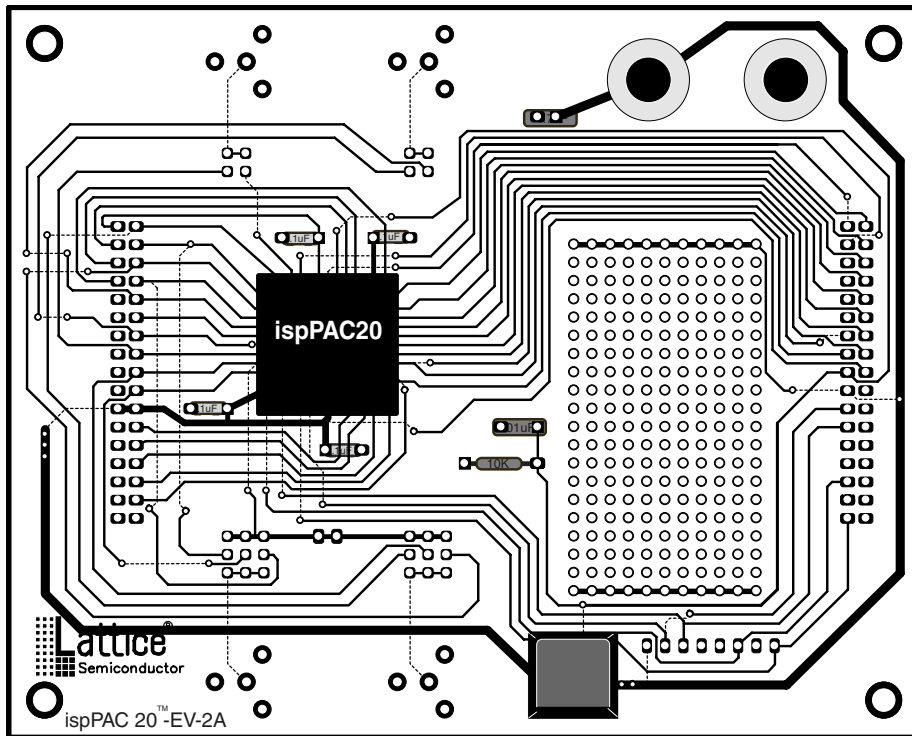
ispPAC20 Evaluation Board

The ispPAC20 Evaluation Board (Figure 1) allows the user to quickly configure and evaluate the ispPAC20 on a fully assembled PC board. The double-sided board supports a 44-pin PLCC package, connectors for input

and output signals, a JTAG programming cable interconnect and a prototype array section for additional circuitry to be added by the user. In-system programming is accomplished through the JTAG port. The JTAG signals are driven from the parallel port of a PC through an ispDOWNLOAD[®] cable. The functional board schematic is shown in Figure 2.

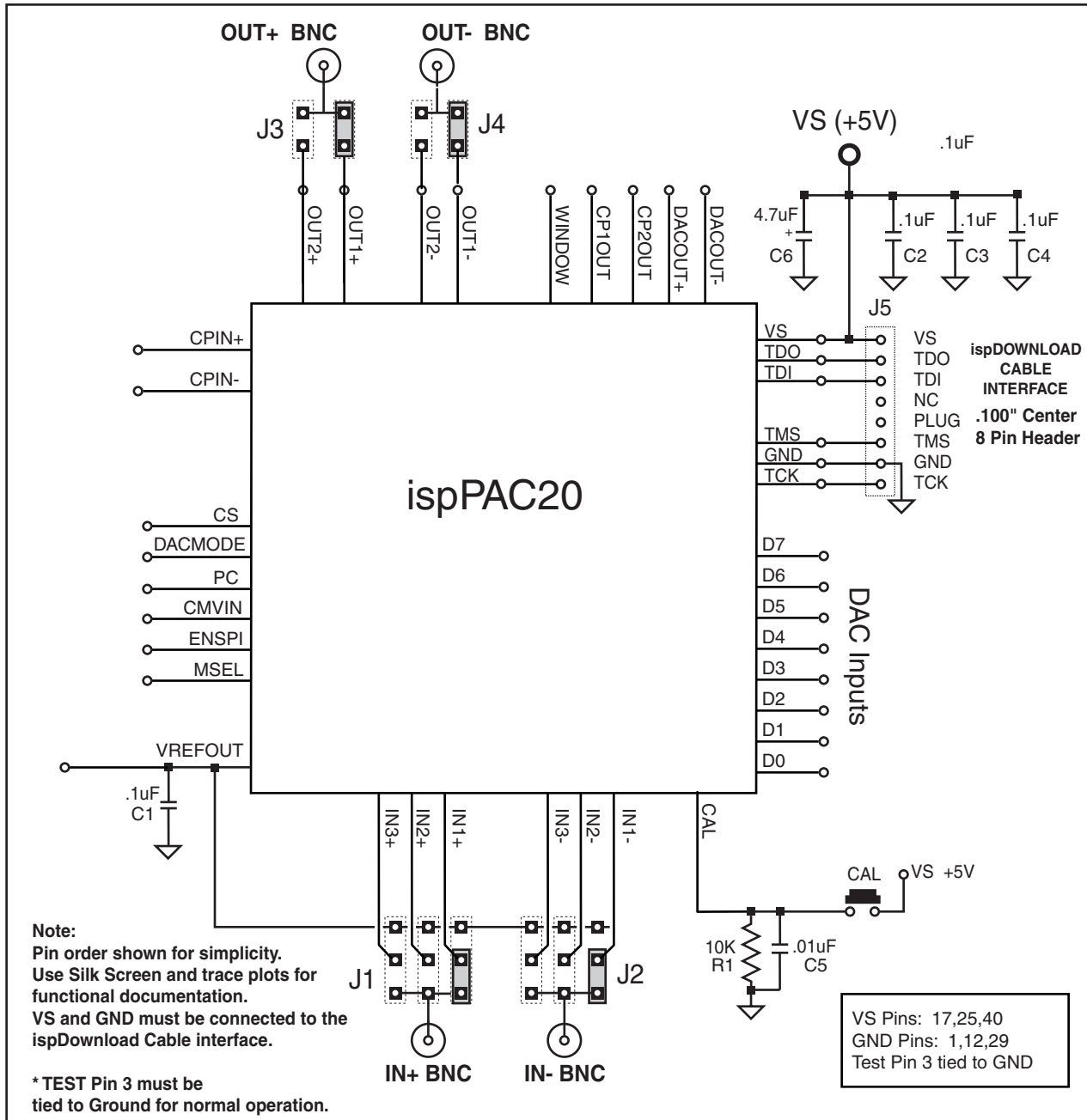
The ispPAC20 utilizes two programmable analog modules called PACblocks. Each of the PACblocks has differential instrumentation inputs and differential outputs. Each input and output is accessible to the user through BNC connectors and jumpers (Figure 3). The DAC inputs and other functions are accessible through a row of 34 position pads, with legend on the silkscreen. The four JTAG programming signals have dedicated pins, which are tied directly to the ispDOWNLOAD programming header J5. As an expansion feature, the programming interface signals as well as all analog signals and digital signals are connected to dual rows with 34 pads for ribbon cable or board-to-board pins. Additional jumpers allow the user to tie any input to the

Figure 1. ispPAC20 Evaluation Board EV-2A



ispPAC20 Evaluation Board ispPAC20EV-2A

Figure 2. Schematic Representation



internal "VREFOUT" common reference circuit. The board contains a momentary pushbutton switch that can be used to initiate a calibration. The calibration adjusts output offset and nulls the offset errors to a fraction of a millivolt.

Programming Interface

The ispPAC20 programming interface consists of the ispDOWNLOAD cable that connects the PC parallel port DB-25 connector to an 8-pin connector header on the

ispPAC20 Evaluation Board. The ispDOWNLOAD cable contains a buffer circuit inside the DB-25 connector at the PC end. The cable is 6 feet in length and has an 8-pin flat receptacle at the board interface end.

Prototype Array

The board contains an array of 220 prototype holes that can be used for experimental evaluation and project interfacing. All inputs and outputs, as well as programming signals have connections to the 34 pin headers.

ispPAC20 Evaluation Board ispPAC20EV-2A

Figure 3. ispPAC20 Evaluation Board Jumper Configurations for Inputs and Outputs

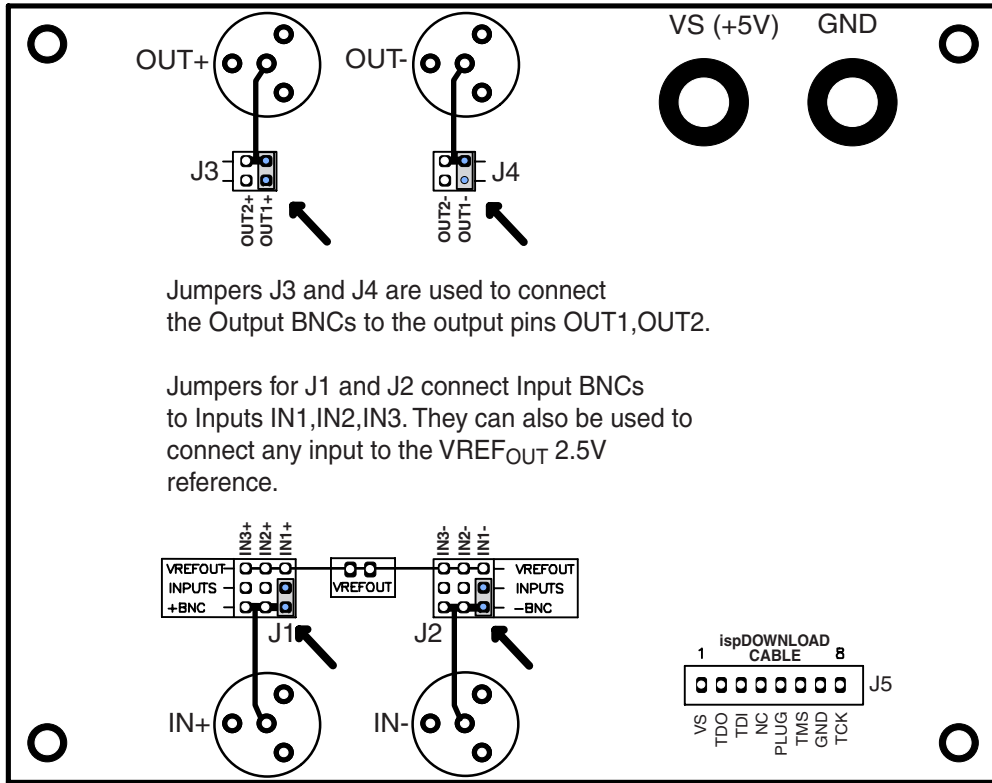
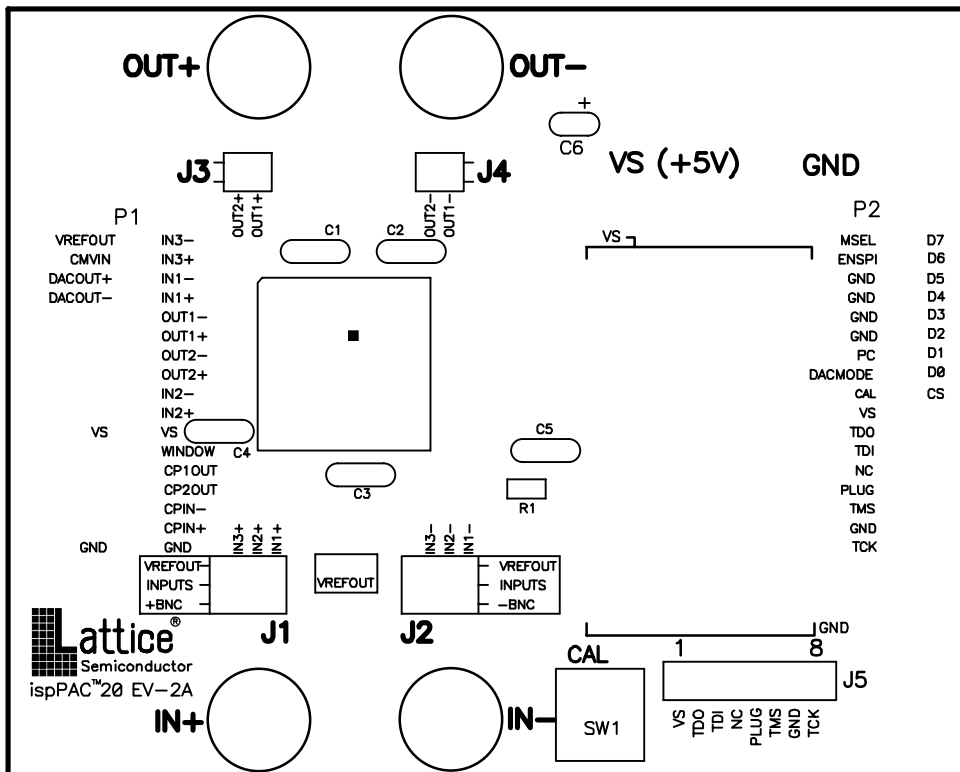


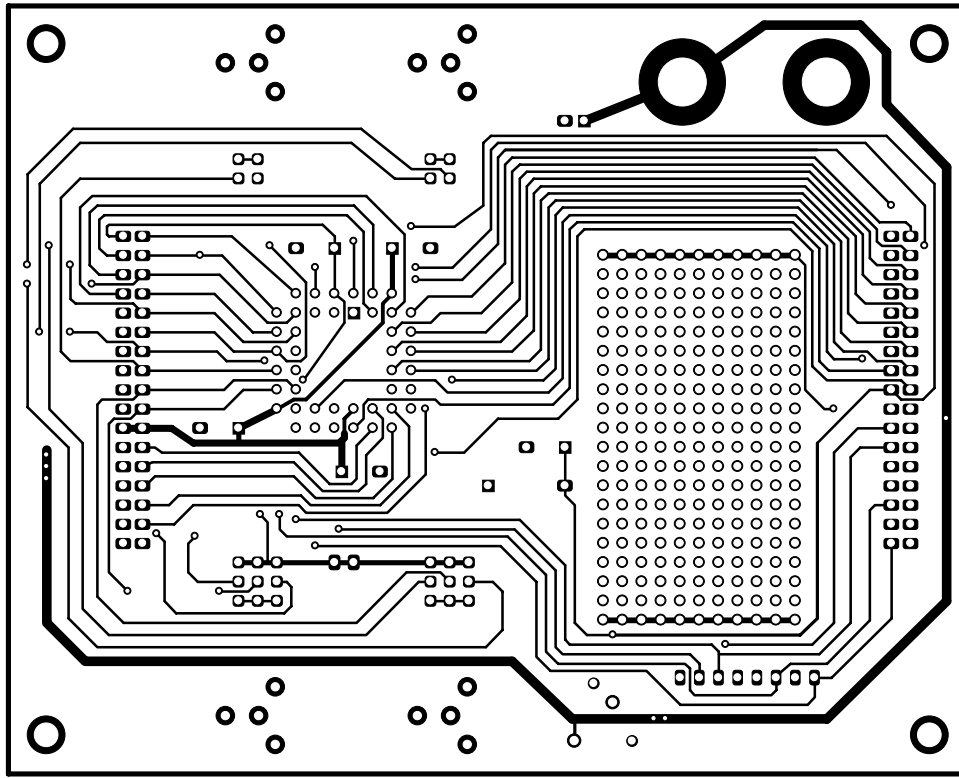
Figure 4. Silk Screen, Top Layer



ispPAC20 Evaluation Board

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Figure 5. PCB, Top Side (Bottom Side Traces Shown as Dotted Lines)



Users can build additional analog or digital circuitry in the prototype area and interface this with the ispPAC20 inputs and outputs.

Power Supply Considerations

A clean 5V supply should be used for the VS supply. Decoupling and bypass capacitors are located on the board near the ispPAC20 device. Two banana plug receptacles are available for VS and Ground connections. A reference voltage input pin (CMVIN) is used to adjust the output common mode voltage level. Refer to the ispPAC20 Data Sheet for further information as to the functions of $VREF_{OUT}$ and CMVIN pins.

Jumper Connections

The Evaluation Board interfaces to a signal source or other test equipment through the BNC connectors or 34 position connectors. There are a pair of BNC connectors for the inputs and a pair for the outputs. The selection for input pins is made with Jumpers J1 and J2 (Figure 3). These jumpers tie the input BNCs to any input pin, and they can also be used to tie an input to the 2.5V reference pin $VREF_{OUT}$. Figure 3 shows the input BNCs tied to IN1+ and IN1- through J1 and J2.

The output pins are routed to the output BNCs through jumpers J3 and J4. These jumpers each select one of four output pins of the ispPAC20. Figure 3 shows the output BNCs tied to OUT1+ and OUT1- with jumper blocks J3 and J4.

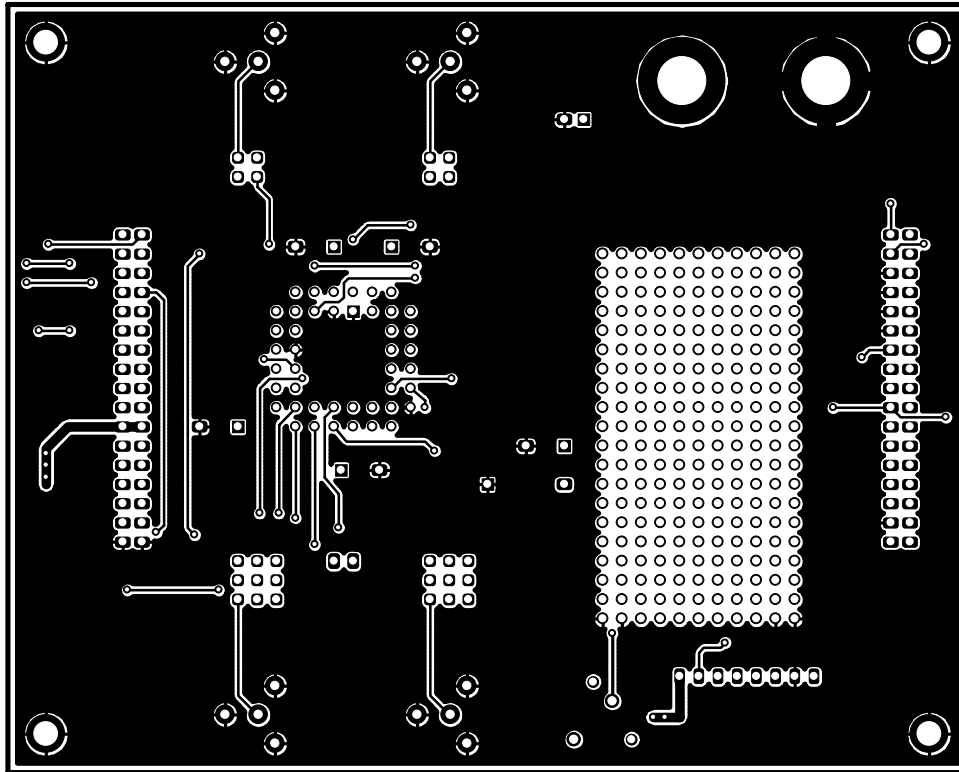
Component List

- (1) PCB, (4.0"x 5.0") .063 FR4 with Solder Mask/Silk Screen
- (4) BNC Connectors
- (2) 3x3 Position Jumper Headers for Inputs
- (2) 2x2 Position Jumper Headers for Outputs
- (1) 8-pin Header for JTAG Programming Interface (J5)
- (1) Pushbutton Switch (Momentary, Normally Open)
- (2) Banana Jacks for VS and GND
- (1) .01uF Capacitor (C5)
- (1) 4.7uF Capacitor (C6)
- (4) .1 uF Capacitor (C1,C2,C3,C4)
- (1) 10K Ohm Resistor (R1)
- (1) 44-pin PLCC Socket

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Figure 6. Bottom Side PCB with Ground-plane Copper Pour



- (1) ispPAC20 44-pin PLCC Sample
- (4) Rubber Bumper Feet
- (4) Shorting Jumpers

Technical Support Assistance

Toll Free Hotline: 1-800-LATTICE (Domestic)
International: 1-408-826-6002
E-mail: ispPACs@latticesemi.com
Internet: <http://www.latticesemi.com>