

Introduction

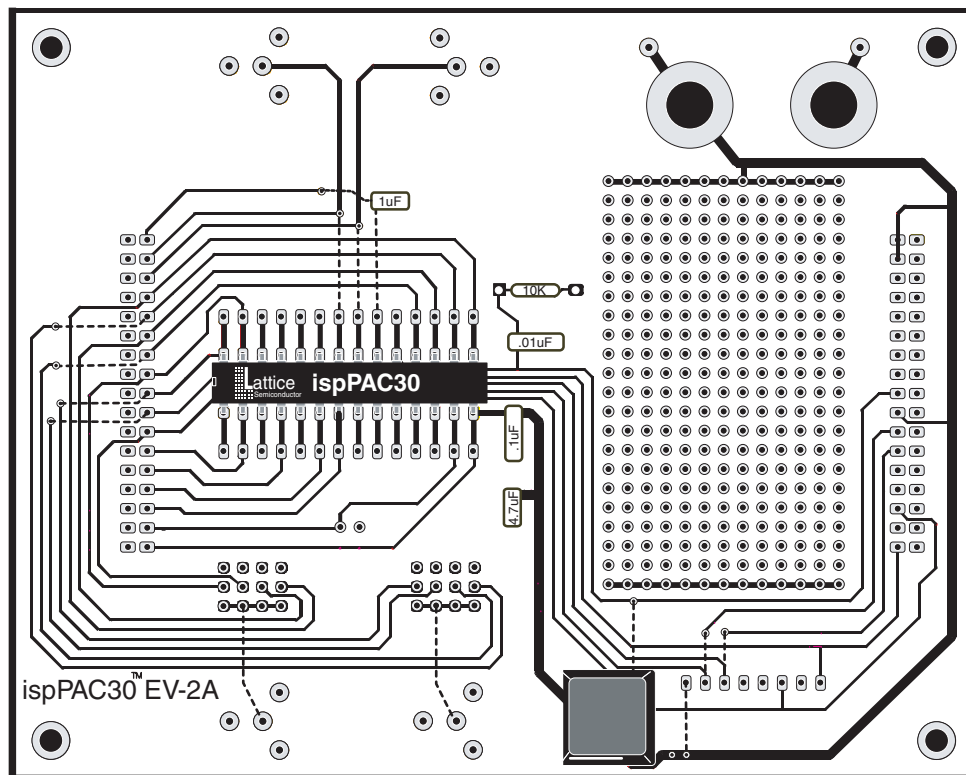
The Lattice Semiconductor ispPAC[®]30 In-System-Programmable Analog Circuit allows designers to build analog circuits such as gain stages and active filters without the use of external feedback resistors or capacitors. This technology brings ISP[™], In-System Programming, to the analog world. Device functionality as well as parameters such as gain and frequency response can be set by the user and changed on-the-fly by reprogramming the device. A standard JTAG IEEE 1149.1 interface allows the user to reconfigure the ispPAC30 while in-system using on-chip non-volatile E²CMOS[®] technology.

ispPAC30 Evaluation Board

The ispPAC30 Evaluation Board (Figure 1), allows the user to quickly configure and evaluate the ispPAC30 on a fully assembled PC board. The double sided board supports a 28-pin DIP package, connectors for Input and Output signals, a JTAG programming cable interconnect and a prototype array section for additional circuitry to be added by the user. In-system programming is accomplished through the JTAG port. The JTAG signals are driven from the parallel port of a PC through an ispDOWNLOAD[®] Cable.

The ispPAC30 utilizes several programmable analog modules called PACCells including two Multiplying DACs and two voltage references that can be interconnected through the Analog Routing Pool. The signals from the Analog Routing Pool drive two Output PACCells. Each of the Input PACCells has differential instrumentation inputs that can also be used as single-ended, ground-referenced inputs.

Figure 1. ispPAC30 Evaluation Board EV-2A

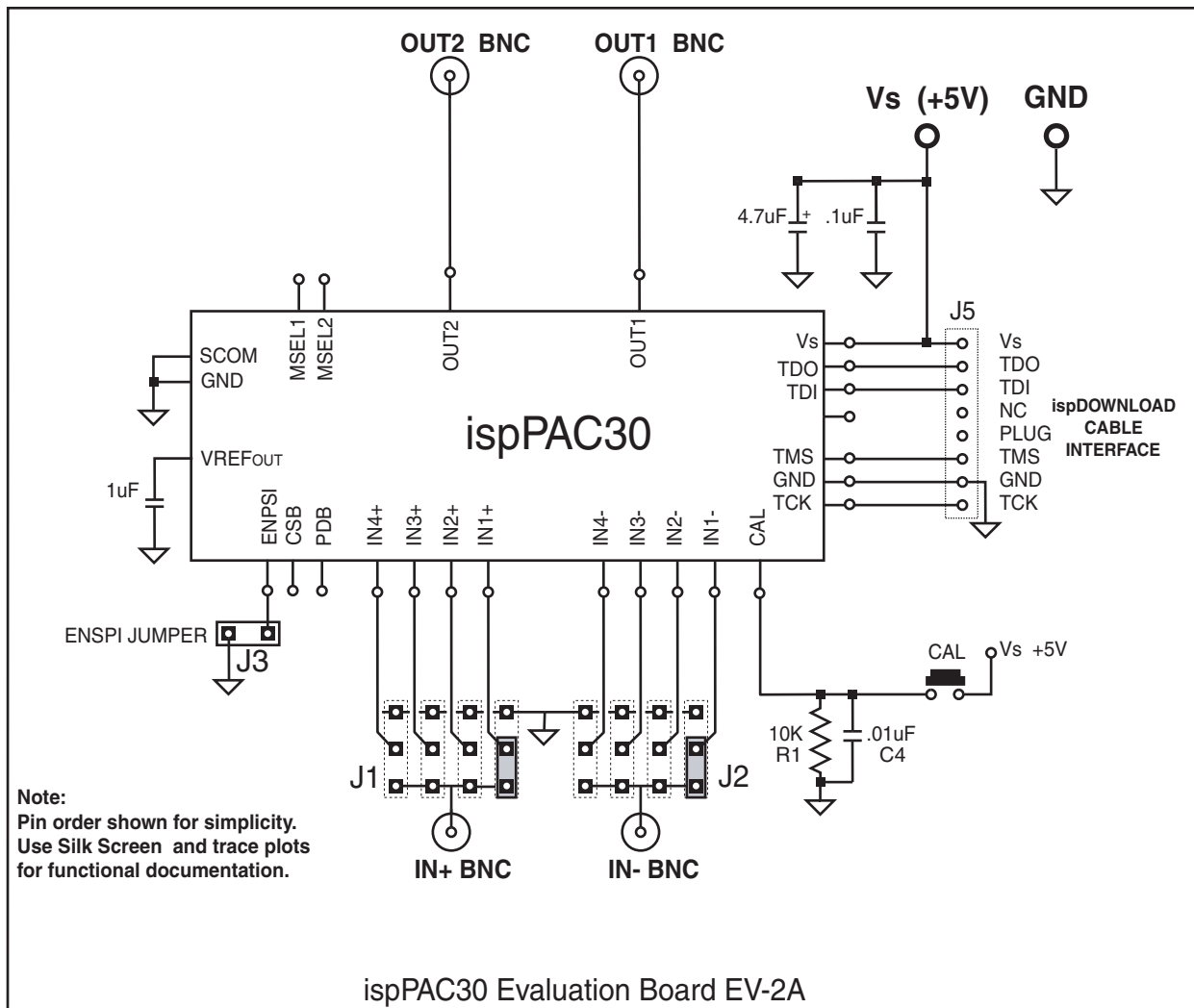


The inputs and outputs are accessible to the user through BNC connectors and jumpers (Figure 3). The four JTAG programming signals have dedicated pins, which are tied directly to the ispDOWNLOAD programming header J5. As an expansion feature, the programming interface signals as well as all analog signals are connected to dual rows of 34 solder pads for ribbon cable or board to board pins. Additional jumpers allow the user to tie any Analog Input to ground. The board contains a momentary push-button switch that can be used to initiate a calibration. The calibration adjusts output offset and nulls the offset errors to a fraction of a millivolt.

Programming Interface

The ispPAC30 Programming Interface consists of the ispDOWNLOAD Cable that connects the PC Parallel Port DB-25 connector to an 8-pin connector header on the ispPAC30 Evaluation Board. The ispDOWNLOAD Cable contains a buffer circuit inside the DB-25 connector at the PC end. The cable is 6 feet in length and has an 8-pin, 0.100" Molex connector.

Figure 2. Schematic Representation



Prototype Array

The board contains an array of 286 prototype holes that can be used for experimental evaluation and project interfacing. All inputs and outputs, as well as programming signals have connections to the 34 pin headers and through-hole pads located adjacent to the appropriate pins of the ispPAC30 device. Users can build additional analog circuitry in the prototype area and interface this with the ispPAC30 inputs and outputs.

Power Supply Considerations

A clean 5V supply should be used for the Vs supply. Decoupling and bypass capacitors are located on the board near the ispPAC30 device. Two banana plug receptacles are available for Vs and Ground connections

Jumper Connections

The Evaluation Board interfaces to a signal source or other test equipment through the BNC connectors or pads. There are a pair of BNC connectors for the inputs. The selection for input pins is made with Jumpers J1 and J2, see Figure 3. These jumpers tie the input BNCs to any input pin, and they can also be used to tie an input to ground. Figure 3 shows the input BNCs tied to IN1+ and IN1- through J1 and J2.

Jumper J3 is used to tie ENSPI to ground. ENSPI can be programmed with an internal pull-up or a pull-down resistor. The jumper allows this pin to be forced to ground to enable JTAG programming. When it is high, the device is in SPI Mode. ENSPI has internal programmable pull-up or pull-down resistors. The state of this pin defines the mode, whether SPI or JTAG, for programming. The Jumper J3 will allow the user to force JTAG mode if the pull-up was programmed from a previous pattern or design. The jumper will allow override in either state and allow the user access to the pull-up/down circuitry via the JTAG download.

Figures 4, 5 and 6 show the silk screen, top layer and bottom layer of the printed circuit board.

Figure 3. Jumper Configurations for Inputs and Outputs

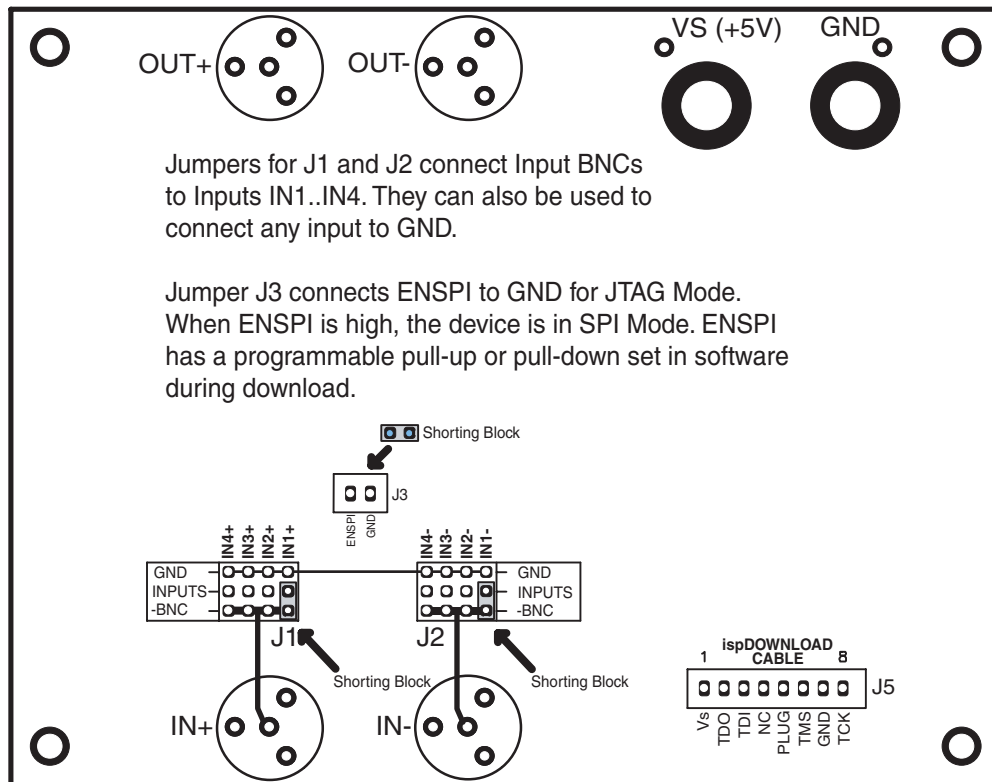


Figure 4. Silk Screen Top Layer

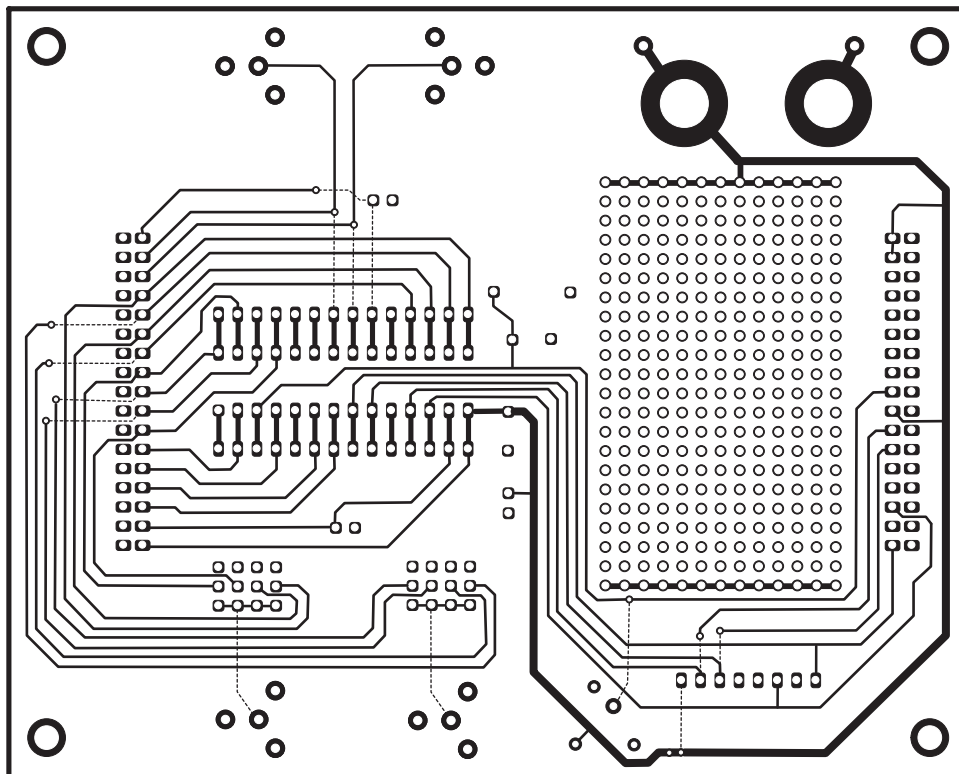
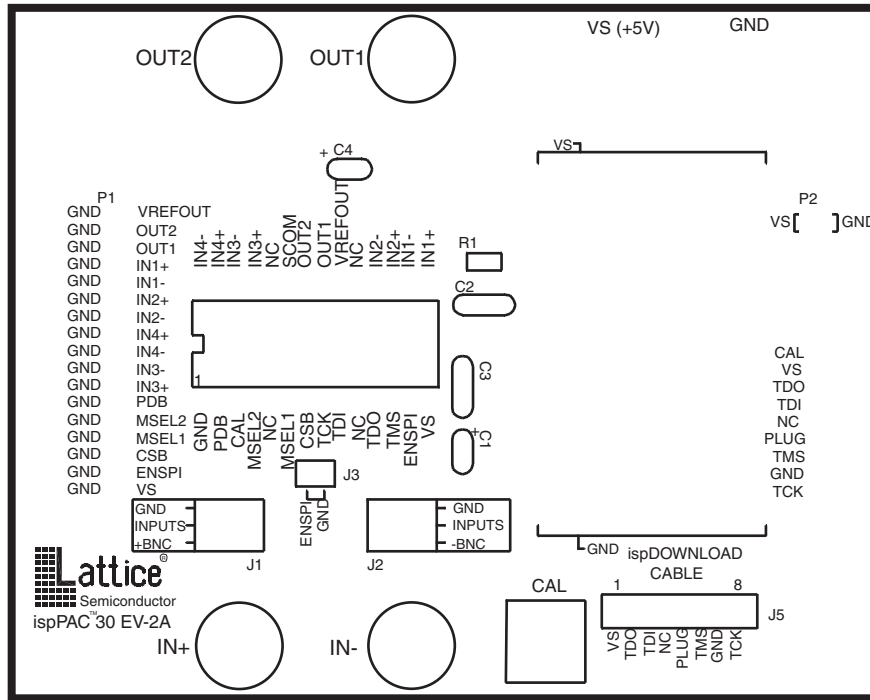
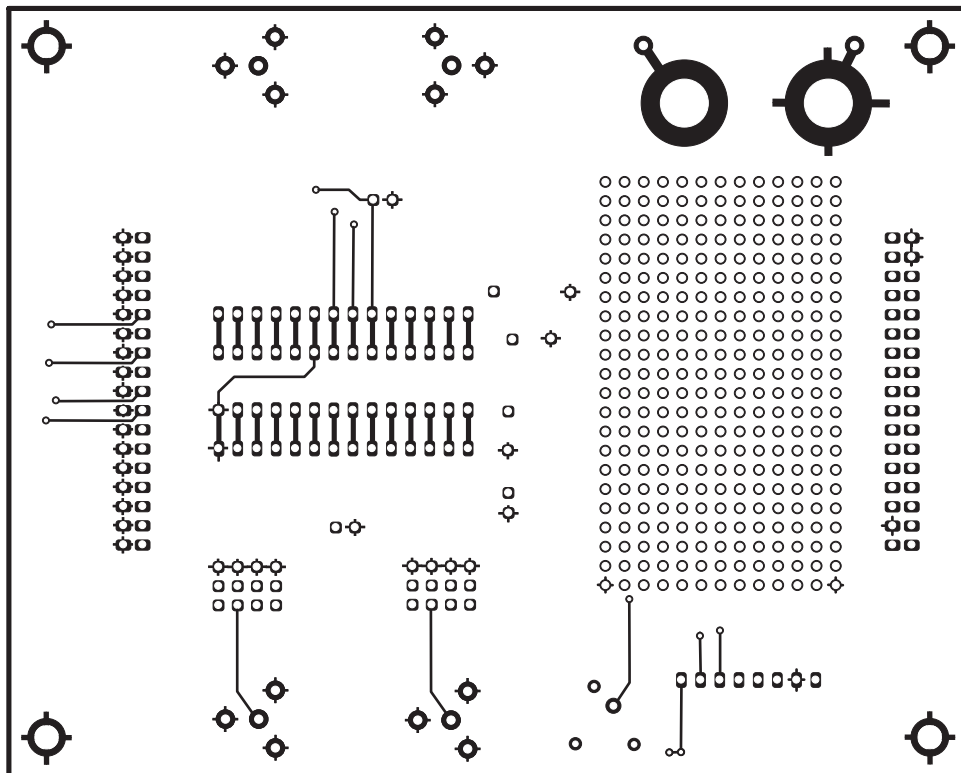


Figure 6. Bottom side PCB (ground-plane pour not shown)



Component List

- (1) PCB, (4.0"x 5.0") .063 FR4 with Solder Mask/Silk Screen.
- (4) BNC Connectors.
- (2) 3x4 Position Jumper Headers for Inputs. J1,J2
- (1) 8-pin Header for JTAG Programming Interface (J5).
- (1) Push-button Switch (momentary, normally open).
- (2) Banana Jacks for Vs and Gnd.
- (1) .01uF capacitor (C2)
- (1) 1uF capacitor (C4)
- (1) 4.7uF capacitor (C1)
- (1) .1 uF capacitor (C3)
- (1) 10K Ohm resistor (R1)
- (1) 28-pin DIP socket.
- (2) ispPAC30 28-pin DIP Samples.
- (4) Rubber bumper feet.
- (3) Shorting jumpers

Technical Support Assistance

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