

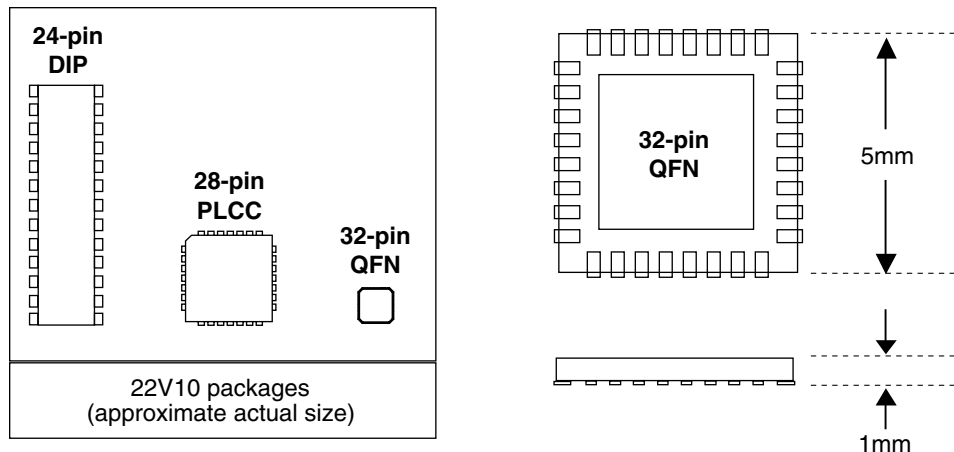
Introduction

Lattice's ispGAL[®]22V10A device in the QFN package provides several added capabilities to the standard 22V10 architecture. The QFN (Quad Flat pack, No lead) package, also known as the MLF (Micro Lead Frame) package, is a near chip scale plastic encapsulated package that provides a small PCB footprint as well as better thermal, better speed and more robust handling characteristics. This application note describes how to handle the QFN package, including information on selecting attributes such as slew rate control, open-drain and input threshold through Lattice's ispLEVER[™] design tool.

QFN Package

Due to the high speed and small die size of the ispGAL22V10A, Lattice supplies this device in the 32-pin QFN package. This package has four more pins than the standard 22V10 in the 28-lead PLCC package. Even with the additional four pins, the QFN package is dramatically smaller than the PLCC package as shown in Figure 1. Refer to the *Package Diagrams* document on the Lattice web site at www.latticesemi.com for a detailed description of the package.

Figure 1. ispGAL22V10 Relative Package Sizes and 32-pin QFN Dimensions



The four additional pins on the QFN package are utilized as two VCCO and two GNDO pins to provide a separate power and ground for the output pins from the core logic. The separate VCCO pin is used to supply a different output voltage reference from the core VCC. The VCCO options on the QFN package are 1.8V, 2.5V and 3.3V for LVCMOS output standards.

The QFN also features a paddle on the bottom of the package that forms a low thermal resistance path from the die. Although not necessary with the low-power ispGAL22V10A device, this paddle can be soldered to the thermal pad of a printed circuit board for improved heat dissipation.

The References section at the end of this document lists QFN socket manufacturers and an application note on QFN assembly recommendations from Amkor Technology.

ispLEVER Software Attributes for the ispGAL22V10A QFN Device

ispLEVER version 3.0 or later supports the ispGAL22V10A QFN device option with the following attributes.

Pullup/Buskeeper

- This attribute is set globally
- Attribute options are:
 - Down for Pulldown
 - Up for Pullup
 - Hold for Bus Hold Latch
 - Off for turning off the bus maintenance option
- This attribute can be set only using ABEL.

Syntax for setting the Pullup/Buskeeper attribute using ABEL:

```
LATTICE property 'PULL down';
LATTICE property 'PULL up';
LATTICE property 'PULL hold';
LATTICE property 'PULL off';
```

Input Threshold

- This attribute is set for individual Input or I/O pin.
- Attribute options are 2.5/3.3V LVCMOS and 1.8V LVCMOS.
- This attribute can be set using VHDL, Verilog and ABEL.

Syntax for setting the Input Threshold attribute using ABEL:

```
LAT_IOTYPES (PinName, LVCMOS33);"2.5/3.3V LVCMOS
LAT_IOTYPES (PinName, LVCMOS25);"2.5/3.3V LVCMOS
LAT_IOTYPES (PinName, LVCMOS18);"1.8V LVCMOS
```

Syntax for setting the Input Threshold attribute using VHDL:

```
ATTRIBUTE IO_TYPES OF PinName:    SIGNAL IS "LVCMOS33 ,-";
ATTRIBUTE IO_TYPES OF PinName:    SIGNAL IS "LVCMOS25 ,-";
ATTRIBUTE IO_TYPES OF PinName:    SIGNAL IS "LVCMOS18 ,-";
```

Syntax for setting the Input Threshold attribute using Verilog:

Exemplar:

```
//exemplar attribute PinName IO_TYPES LVCMOS33,-;
//exemplar attribute PinName IO_TYPES LVCMOS25,-;
//exemplar attribute PinName IO_TYPES LVCMOS18,-;
```

Synplicity:

```
output PinName /* synthesis IO_TYPES="LVCMOS33,-"*/;
output PinName /* synthesis IO_TYPES="LVCMOS25,-"*/;
output PinName /* synthesis IO_TYPES="LVCMOS18,-"*/;
```

SlewRate

- This attribute is set for individual I/O pin.
- Attribute options are Slow and Fast.
- This attribute can be set using VHDL, Verilog and ABEL.

Syntax for setting the SlewRate attribute using ABEL:

```
LAT_SLEW (SLOW, PinName);"Slow Slew
LAT_SLEW (FAST, PinName);"Fast Slew
```

Syntax for setting the SlewRate attribute using VHDL:

```
ATTRIBUTE SLEW OF PinName: SIGNAL IS "SLOW";
ATTRIBUTE SLEW OF PinName: SIGNAL IS "FAST";
```

Syntax for setting the SlewRate attribute using Verilog:

Exemplar:

```
output PinName; //exemplar attribute PinName SLEW SLOW
output PinName; //exemplar attribute PinName SLEW FAST
```

Synplicity:

```
output PinName /* synthesis SLEW="SLOW" */;
output PinName /* synthesis SLEW="FAST" */;
```

Open Drain

- This attribute is set for individual I/O pin.
- Attribute options are Open Drain. If this attribute is not specified the default standard LVCMOS output.
- This attribute can be set using VHDL, Verilog and ABEL.

Syntax for setting the Open Drain attribute using ABEL:

```
LAT_IOTYPES (PinName, LVCMOS33_OD);"2.5/3.3V LVCMOS Opendrain
LAT_IOTYPES (PinName, LVCMOS25_OD);"2.5/3.3V LVCMOS Opendrain
LAT_IOTYPES (PinName, LVCMOS18_OD);"1.8V LVCMOS Opendrain
```

Syntax for setting the Open Drain attribute using VHDL:

```
ATTRIBUTE IO_TYPES OF PinName: SIGNAL IS "LVCMOS33_OD ,-";
ATTRIBUTE IO_TYPES OF PinName: SIGNAL IS "LVCMOS25_OD ,-";
ATTRIBUTE IO_TYPES OF PinName: SIGNAL IS "LVCMOS18_OD ,-";
```

Syntax for setting the Input Threshold attribute using Verilog:

Exemplar:

```
//exemplar attribute PinName IO_TYPES LVCMOS33_OD,-;
//exemplar attribute PinName IO_TYPES LVCMOS25_OD,-;
//exemplar attribute PinName IO_TYPES LVCMOS18_OD,-;
```

Synplicity:

```
output PinName /* synthesis IO_TYPES="LVCMOS33_OD,-"*/;
output PinName /* synthesis IO_TYPES="LVCMOS25_OD,-"*/;
output PinName /* synthesis IO_TYPES="LVCMOS18_OD,-"*/;
```

References

QFN Socket Manufacturers

- Adapters.com: www.adapters.com
- Aries Electronics, Inc.: www.arieselec.com
- Emulation Technology Inc.: www.1800adapter.com
- Gryphics Inc.: www.gryphics.com
- Loranger International Corporation: www.loranger.com
- Plastronics: www.locknest.com

Application Note

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages, available from Amkor Technology at www.amkor.com.

Technical Support Assistance

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