

ispLeverCORE

Re-Usable, Fully-Tested IP Modules

Lattice's new ispLeverCORE™ IP modules are large, modular design blocks that can be reused and easily placed within a programmable logic design. ispLeverCORE modules implement popular industry-standard functions, commonly used in communications, bus interface, memory control, and DSP applications.

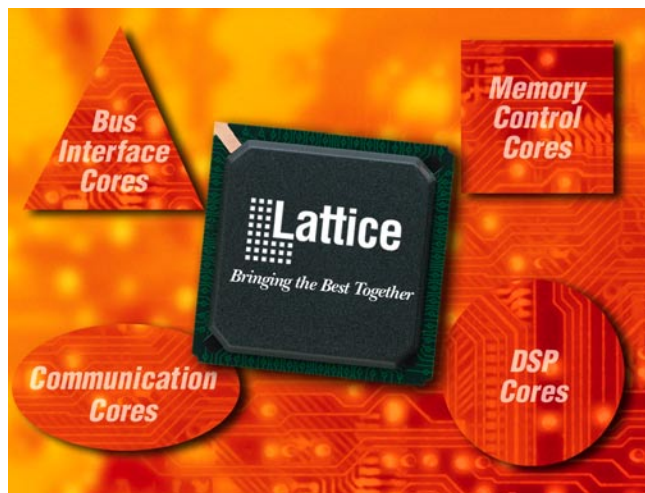
ispLeverCORE IP modules are designed using the highest coding standards and are fully tested to meet functional and performance requirements. These cores are ready-to-use, well documented, and are fully supported by Lattice field and factory engineers. Most ispLeverCORE modules are designed to be parameterizable. That is, the core can quickly be reconfigured to meet specific system needs.

By leveraging Lattice's combined work in hardware, software, and IP, users enjoy enormous savings in time and effort, and achieve faster time-to-market.



ispLeverCORE IP Modules

The ispLeverCORE Modules listed below are just a sample of the IP cores available from Lattice. ispLeverCORE modules are designed to support ispXPGA™, ispXPLD™, ORCA® Series 4, and FPSC devices.



Key Features and Benefits

- **A Foundation of Ready Designs**
 - Parameterizable
 - Free “no-risk” evaluations
 - Easily integrated into VHDL or Verilog projects
 - Standardized license agreement
- **High Coding Standards**
 - Reuse Methodology Manual
 - Coded for compactness
 - Coded for high performance
 - Lattice device-specific coding
 - Automated design rule checking
- **Fully Tested**
 - Code coverage analyzed
 - Tested for routability and consistent performance
 - Tested for compatibility on supported software including 3rd-party simulators and synthesis tools

ispLeverCORE IP Modules (go to www.latticesemi.com for a complete listing and availability)

Communication Cores

UTOPIA Level 3 ATM Transmit Interface
 UTOPIA Level 3 ATM Receive Interface
 UTOPIA Level 3 PHY Transmit Interface
 UTOPIA Level 3 PHY Receive Interface
 10/100 Mbps Ethernet MAC
 Gigabit Ethernet MAC
 10GbE PCS
 Quad Gigabit Ethernet over SONET
 POS-PHY Level 3 Physical Layer Interface
 POS-PHY Level 3 Link Layer Interface

Bus Interface Cores

PCI Master/Target: 32-bit
 PCI Master/Target: 64-bit
 PCI Target: 32-bit
 PCI Target: 64-bit

Memory Control Cores

Multi-Channel DMA Controller
 DDR SDRAM Controller: Generic Interface
 DDR SDRAM Controller: PowerPC® Interface
 DDR SDRAM Controller: AHB Interface
 DDR SDRAM Controller: PCI Interface

Digital Signal Processing Cores

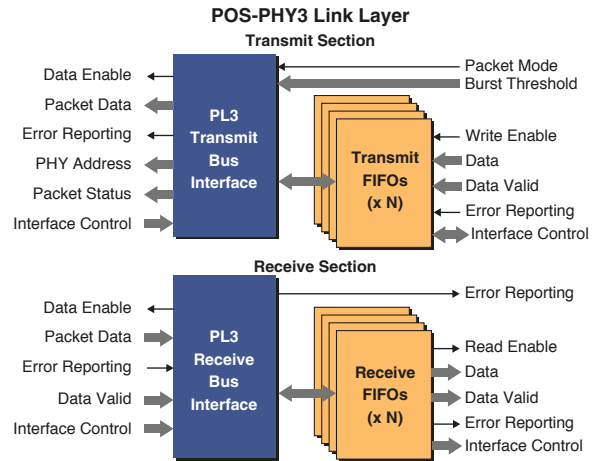
Reed Solomon Decoder
 Reed Solomon Encoder
 Turbo Decoder
 Turbo Encoder
 FIR Filter: Serial
 FIR Filter: Parallel
 Convolutional Encoder
 Viterbi Decoder

Example ispLeverCO

Communication Cores

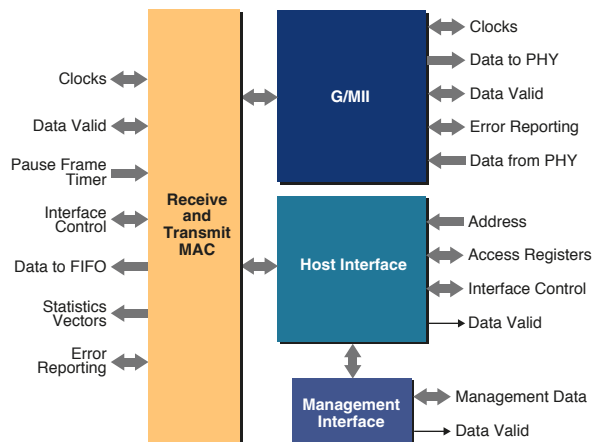
POS-PHY 3 Link & PHY Layer Interfaces

- Conforms to POS-PHY Level 3 (PL3) Specification
- 104MHz FIFO Clock Rate
- Multiple-port Configuration
- 8- or 32-bit Configuration
- Supports Variable-size Packets
- Programmable PL3 Bus Burst Length
- Fully Synchronous Design
- Seamless PL3 Interface with other Lattice PL3 Cores
- Transmit and Receive FIFOs for Full-duplex Operation
- Generic Asynchronous FIFO Interface
- Configurable FIFO Parameters for
 - Depth
 - Threshold Level for Packet Available Signal Generation
 - Almost Full and Almost Empty Threshold Levels



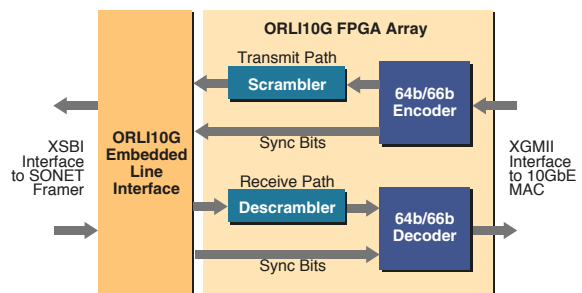
Ethernet MACs

- 10/100 Mbps and Gigabit Versions
- Compliant to IEEE 802.3z Standard
- Generic Host Interface with Configurable 8-bit or 16-bit Data Bus
- 16-bit Wide Internal Data Path
- Full-duplex Operation in Gigabit Mode
- Full and Half Duplex in 10/100 Mode
- Transmit and Receive Statistics Vector
- Programmable Inter Packet Gap (IPG)
- Multicast Address Filtering
- Supports
 - Full-duplex Control Using PAUSE Frames
 - VLAN Tagged Frames
 - Automatic Re-transmission on Collision
 - Automatic Padding of Short Frames



10Gb Ethernet PCS Solution

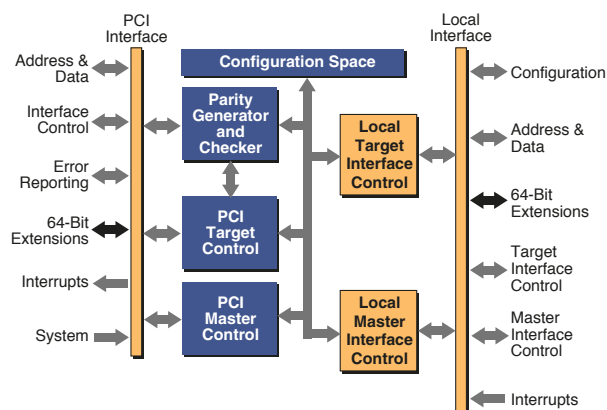
- Complete Physical Coding Sublayer (PCS) Solution Enabling Flexible 10GbE LAN/WAN Applications
- IP Implemented in the FPGA Section of the ORCA 10 Gbits/s Line Interface (ORLI10G) FPSC. The XSBI (OIF standard 99.102.5) is Embedded in the ORLI10G.
- Conforms to IEEE Standard 802.3ae, including:
 - XGMII for Interfacing with 10GbE MACs
 - Elastic Store Buffers for Clock Domain Transfer to/from the XGMII
 - X58 + X39 + 1 Polynomial 10GbE Scrambler/Descrambler
 - 64b/66b Encoder/Decoder, Separate Transmit & Receive Gearboxes, 66-bit Receive Word Aligner
- ORCA Bitstream Format for Turnkey Functionality



Bus Interface Cores

PCI Master/Target

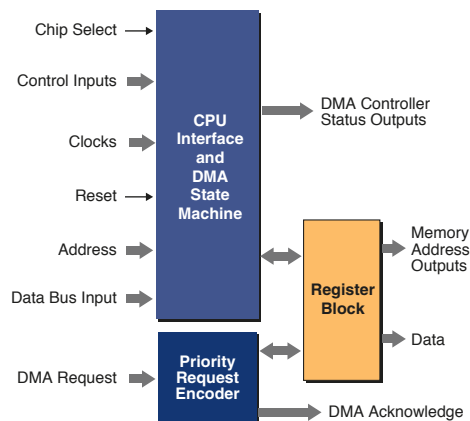
- Available as 32/64-Bit PCI Bus and 32/64-Bit Local Bus
- PCI SIG Local Bus Specification, Revision 2.2 Compliant
- 64-Bit Addressing Support
- Capabilities List Pointer Support
- Parity Error Detection
- Up to Six Base Address Registers (BARs)
- Expansion ROM BAR Support
- Fast Back-to-Back Transaction Support
- Supports Zero Wait State Transactions
- Special Cycle Transaction Support
- Customizable Configuration Space
- Up to 66MHz PCI
- Fully Synchronous Design



Memory Controller Cores

Multi-Channel DMA Controller

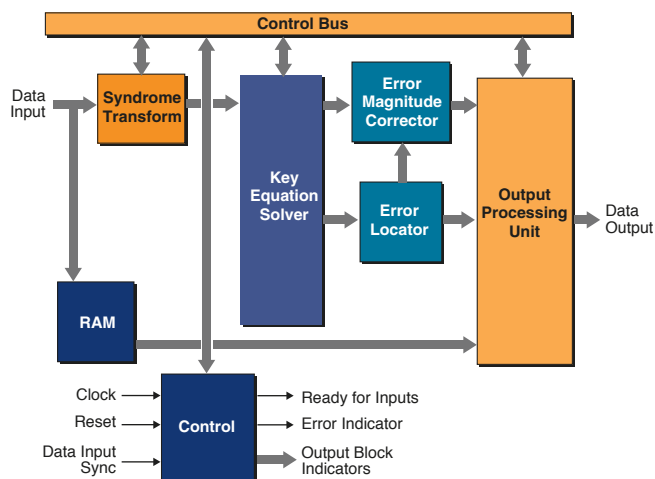
- Selectable 8237 Mode
- Configurable up to 16 Independent DMA Channels for Non-8237 Mode
- Configurable Data Width of 8, 16, 32 or 64 Bits for Non-8237 Mode
- Configurable Address Width of 16, 24 or 32 Bits for Non-8237 Mode
- Configurable Word Count Register Width for Non-8237 Mode
- Independent Auto-Initialization of All Channels
- Memory-to-Memory Transfers on Single, Block, and Demand Transfer Mode
- Memory Block Initialization
- Software DMA Requests



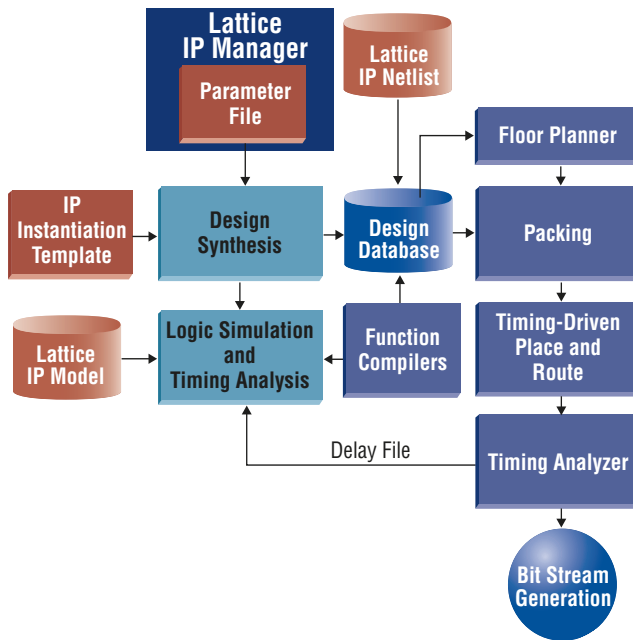
Digital Signal Processing Cores

Reed Solomon Decoder

- Forward Error Correction (FEC) for Communication and Common Applications
- Selectable Reed-Solomon Standards
 - CCSDS (255,223) – Consultative Committee for Space Data Systems
 - ATSC (207,187) – Advanced Television Systems Committee
 - DVB (204,188) – Digital Video Broadcasting
 - OC-192 (255,239) – Optical Carrier
- Shortened Codes Supported
- Errors/Erasures Supported
- Supports Symbol Widths From 3 to 12 Bits, Corresponding to GF(8) to GF(4096) Respectively
- User-Defined and Default Field and Generator Polynomials Supported
- Error Measurement Information



ispLeverCORE Flow in ispLEVER™ Software



Free Evaluation Packages

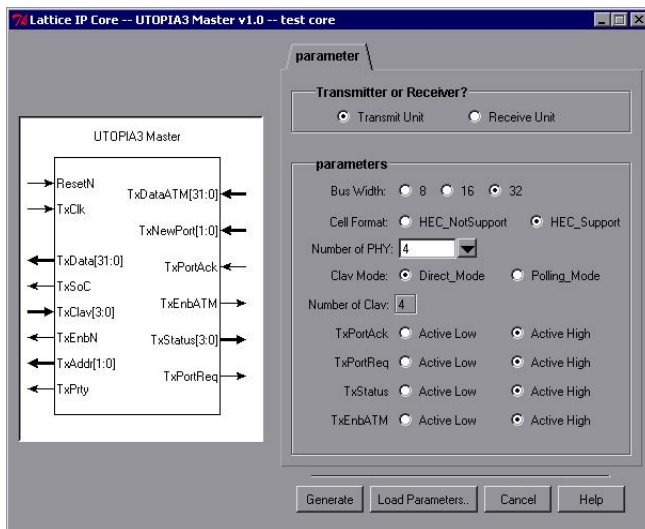
Lattice offers a free evaluation package for most ispLeverCORE products. Packages include:

- Data Sheet
- User's Guide
- Model for Functional Simulation
- System-Level Testbench
- Netlist(s)
- Parameter Configuration File(s)
- Constraints or Preferences File(s)

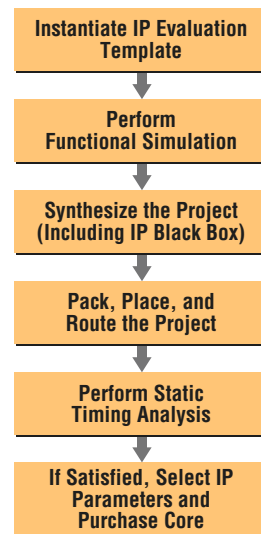


Lattice IP Manager Software Tool

- Easy-to-use GUI for Parameter Selection
- Makes Lattice ispLeverCORE Products Easy-to-Use
- No-Risk Free Trial Evaluations
- Complete On-line Help Documentation



ispLeverCORE Evaluation Flow



For the latest information on Lattice's ispLeverCORE IP modules go to www.latticesemi.com/ip

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