Lattice Semiconductor Corporation

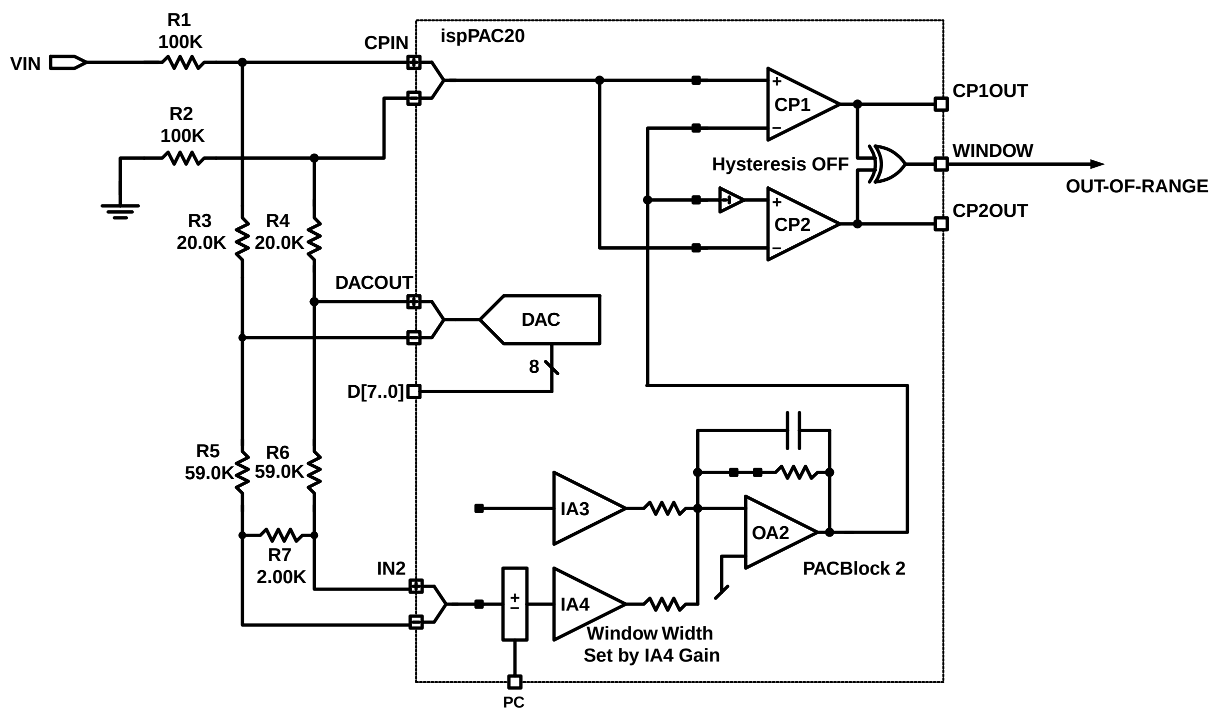
Voltage Monitor Circuit

February 2001 **Circuit Solution**

Determining if a voltage is within a given set of limits is important in a wide variety of electronic systems. For example, many modern microprocessors require power supply voltages to be held within tight tolerances to ensure correct operation and to avoid potential damage.

The circuit shown in Figure 1 can be used to monitor a single voltage of either positive or negative polarity using a single ispPAC®20 and seven external precision resistors. This circuit allows one to set the target voltage through the ispPAC20's DAC, and to independently set a plus or minus percentage 'voltage valid' window around the target voltage by setting the gain of IA4.

Figure 1. ispPAC20 Voltage Monitoring Circuit



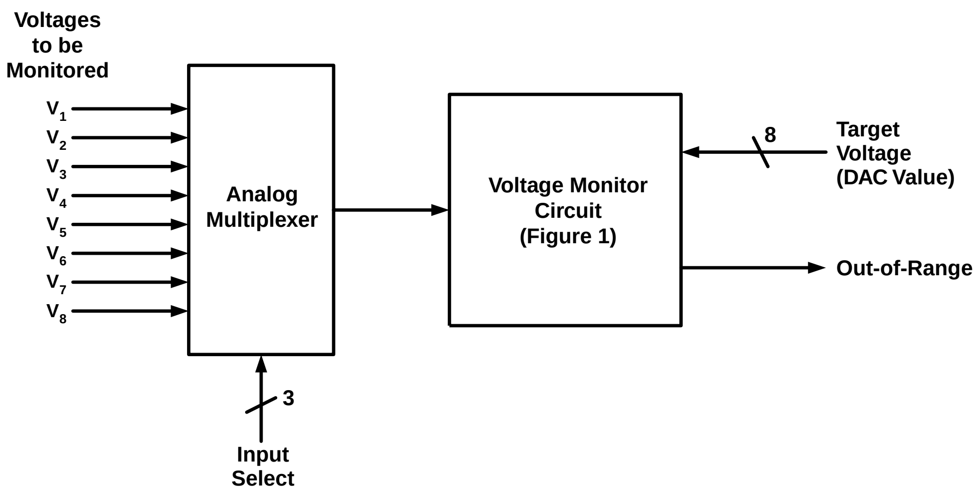
This circuit operates by balancing the input voltage against a reference voltage derived from the ispPAC20's on-board Digital-to-Analog converter (DAC). This is done by the resistive network formed by R1 through R4. The resistor values chosen provide a 5:1 ratio between the input voltage and the DAC voltage, so that a 5V input can be balanced by a 1V DAC voltage. When the input voltage is exactly 5X the DAC voltage, the differential voltage sensed at the input of CPIN is zero. To sense around a given target voltage, one should set the DAC voltage to 1/5th of the target.

The CPIN voltage is fed to CP1 and CP2, which are configured as a symmetric window comparator. The threshold limits for these comparators are obtained from the output of OA2. In this circuit, these threshold limits are also derived from the output of the DAC, suitably divided down (60:1) by resistors R5,R6, and R7. This causes the threshold levels to be proportional to the DAC voltage, resulting in plus and minus thresholds that are a constant percentage of the target voltage. These thresholds can be changed by setting the gain of IA4. The division ratio of 60:1 was chosen so that each gain step of IA4 would correspond to a +/-2% step in setting the out-of-range window. For example, to set a +/-10% limit around the target voltage, one would set the gain of IA4 to -5.

As an example of how to set up this circuit, consider monitoring a voltage of 12V +/-8%. To monitor this spec, one would set the DAC voltage to 2.4V (12 ÷ 5) and set the gain of IA4 to -4 (8% ÷ 2% / step).

Even though the ispPAC20 runs from a single +5V supply, this circuit can also be used to monitor negative voltages.. To set a negative target voltage requires that one set the DAC to a negative voltage. The input circuit (R1-R4) will still present a positive voltage to the CPIN terminals.

Figure 2. Using Voltage Monitor with multiple Input Voltages



Because the target voltage is controlled by the DAC, it can be changed 'on-the-fly' through either the ispPAC's parallel or serial interfaces. This can be useful in situations where a number of different voltages need to be monitored if they all share the same percentage tolerance bands. This can be done by adding an input multiplexor as shown in Figure 2 and by reloading the DAC with the appropriate target values as one switches the multiplexor among the various input voltages.

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-826-6002 (International)
e-mail: ispPACs@latticesemi.com