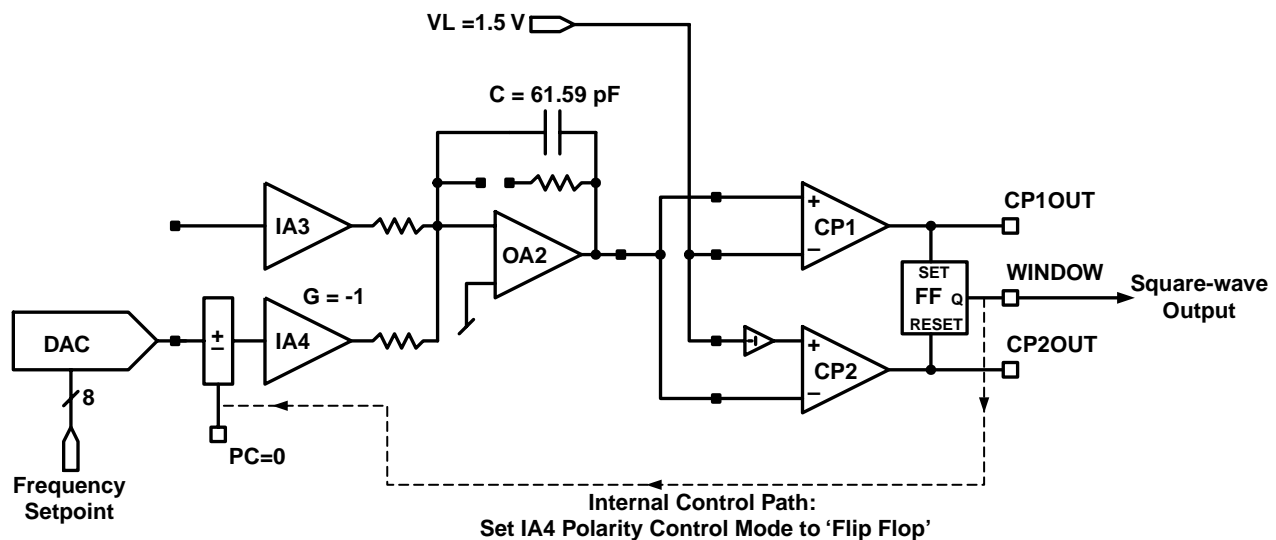


Digitally programmable oscillators can be useful in many applications where a more traditional analog device is often found. The ability to change frequency with a digital adjustment, as opposed to having to manually adjust potentiometers offers significant manufacturability advantages. Additionally, for frequency synthesis and phase-locked-loop applications, digitally controlled oscillators provide significant performance and system integration advantages over their analog counterparts.

The ispPAC20 can be used to implement digitally programmable oscillators which operate from a few hundred Hz to approximately 100kHz. Because the gains, time constants and reference voltages in the ispPAC20 are consistent both on a unit-to-unit basis and over temperature, it is straightforward to use the ispPAC20 as the basis for a stable programmable oscillator circuit. The digital frequency setting may be either written into E<sup>2</sup> memory so that the device powers-up set to a desired frequency or updated on-the-fly through the ispPAC20's parallel, JTAG or SPI ports. The schematic of Figure 1 shows how to use an ispPAC20 to implement this function.

**Figure 1. Digitally Programmable Oscillator Using ispPAC20**

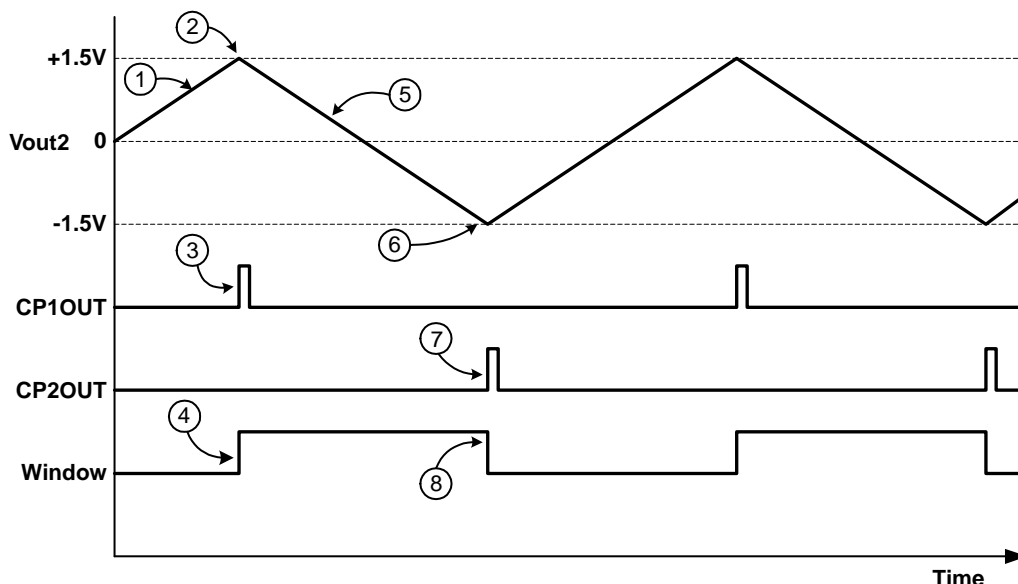


To successfully implement this circuit, there are several options on the ispPAC20 that must be set correctly. They are:

- 1) The feedback link on OA2 must be OPEN
- 2) The WINDOW output must be set to Flip-Flop mode instead of the XOR mode.
- 3) IA4's polarity control should be set to 'Flip-Flop' mode

The operation of this circuit can be understood by following the events that occur in it through a single cycle of oscillation. These events and the associated voltage waveforms are illustrated in Figure 2.

This circuit operates by integrating a constant voltage provided by the DAC. This results in a ramp whose slew rate is proportional to the DAC setting. Referring to Figure 2, Vout2 ramps in a positive direction (1) until it reaches a specified threshold (VL) of +1.5V (2). At this point, CP1 turns ON (3) and sets the output flip-flop, bringing the WINDOW output line high (4). Because the polarity control of the integrator (PC pin) is controlled by the WINDOW output, this changes the direction of integration, and Vout2 ramps in a negative direction (5). When Vout2 falls below

**Figure 2. Voltage Waveforms in Programmable Oscillator**

the negative threshold of -1.5V (6), comparator CP2 turns ON (7), and resets the output flip-flop (8). At this point Vout2 begins to ramp in a positive direction and the cycle repeats.

When using the gain, capacitor and threshold settings shown in Figure 1, this circuit can provide frequencies ranging from about 0.3kHz (DAC setting = 129) to 31kHz (DAC setting=255), selectable in roughly 300Hz increments. Note that for this circuit to operate correctly, the DAC needs to be set to a value that provides a positive output voltage (DAC setting is > 128). It is possible to halve this operating frequency range by increasing the threshold voltages from +/-1.5 to +/-3. It is also possible to increase the operating frequency range by reducing the capacitor value or increasing the gain value. Although this circuit can oscillate at up to 300kHz, at operating frequencies much beyond 50kHz the comparator delay becomes a significant fraction of the oscillator's cycle time and reduces the actual output frequency below that which one would expect.

## Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)  
1-408-826-6002 (International)  
e-mail: [ispPACs@latticesemi.com](mailto:ispPACs@latticesemi.com)