

A delta-sigma ($\Delta-\Sigma$) modulator provides a simple way to digitize an analog signal into a bit-serial digital signal, and can be used in several ways. By taking the digital output signal, and running it through an appropriate digital filter, one can make a first-order delta-sigma ($\Delta-\Sigma$) analog-to-digital converter. Another use for $\Delta-\Sigma$ modulators is in isolation circuits. In this application, an analog signal is delta-modulated, and the resulting digital bit-stream is then used to drive an opto-isolator or a fiber-optic transmitter. The digital signal is recovered at the receiver end of the isolator or optical fiber, at which point the original analog input signal can be reconstructed.

Figure 1. Block Diagram of Delta-modulation

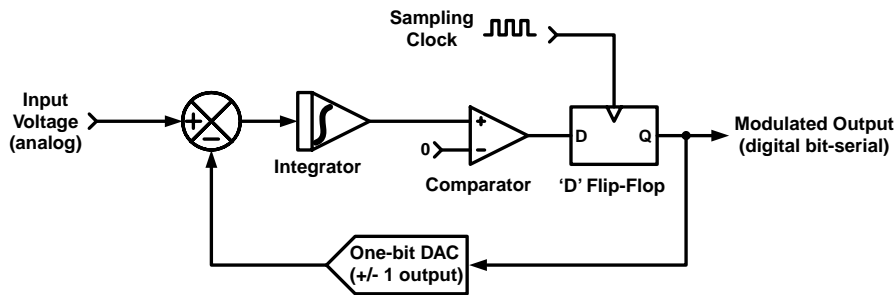
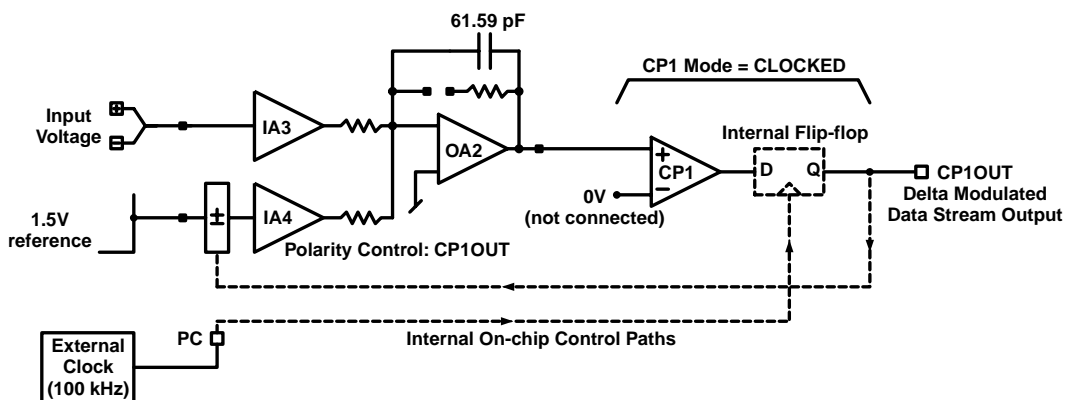


Figure 1 shows a block diagram of a $\Delta-\Sigma$ modulator. This system balances an input signal with an opposing feedback signal produced by a one-bit digital-to-analog converter (DAC). The resulting error signal is then integrated, compared to a threshold, and the resulting digital value is then sampled by a flip-flop. The output of the flip flop is then in turn used to control the DAC, and also provides the modulated equivalent of the input signal. Despite the nonlinear components comprising this feedback loop (comparator, flip-flop, DAC), this system is stable and will achieve a predictable 'steady-state' condition in response to a DC input. Because of the system's various non-linearities and data sampling, however, the 'steady-state' response to a DC input consists of an output pulse stream with specific average value and spectral characteristics.

The above system-level diagram can be implemented with a single ispPAC20 programmable analog IC, without the need for any additional external components. Figure 2 shows how this is done.

Figure 2. 100kHz Delta-modulator Implemented with a Single ispPAC20 Device



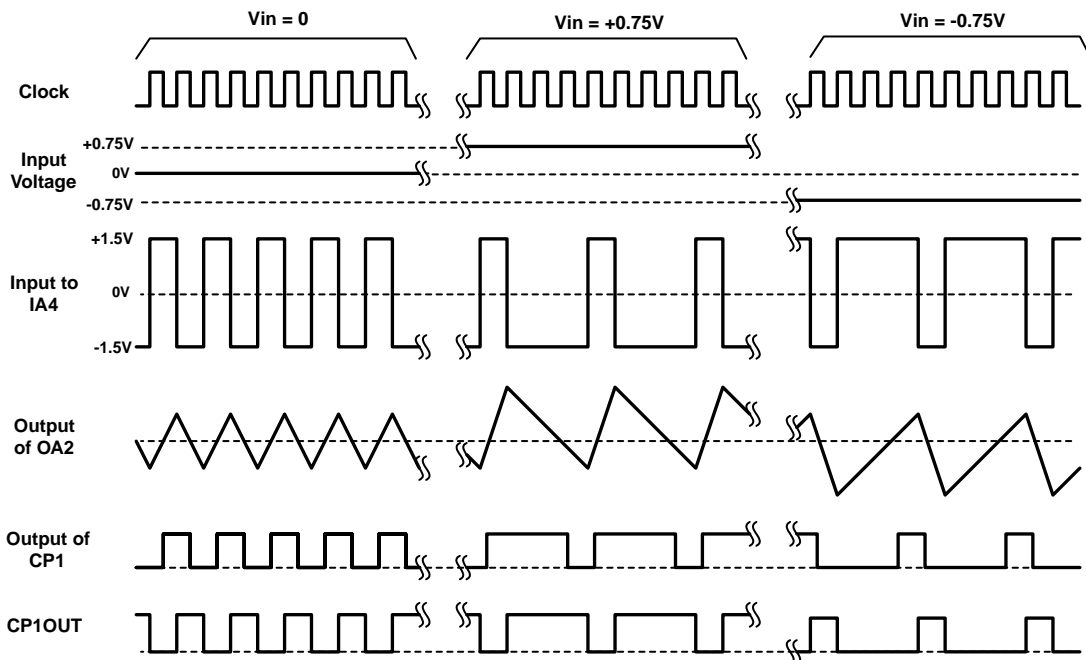
In this circuit, the integration function is performed by OA2. When the CP1 mode is set to 'CLOCKED,' the ispPAC20 inserts a 'D' flip-flop between the output of the CP1 comparator and CP1out, providing the sampling function. In this mode, the sampling clock is input on the PC pin.

The one-bit DAC is implemented by using IA4's polarity control with a fixed reference. In this case, this is the internal 1.5V reference, but the 3V reference, the ispPAC20 DAC, or an external reference brought in from the outside may also be used. In this way the polarity control behaves as a single-bit DAC, outputting either a +1.5V or -1.5V signal. The magnitude of the reference sets the 'full-scale' range for the Δ - Σ modulator.

By setting the polarity control mode on IA4 to 'CP1OUT,' the polarity control will be switched directly by the state of CP1. This saves having to provide an external connection from the CP1OUT pin to the PC pin. For the configuration presented above, some 'typical' steady state waveforms are provided in Figure 3 to help illustrate how this circuit works. Examples are provided for several input voltage conditions.

Because of the fast response times of the ispPAC20 polarity switch and comparators, delta-sigma modulators with sampling frequencies of 100kHz and even higher can be readily implemented with the ispPAC20.

Figure 3. Typical Steady-state Waveforms for Various Voltage Inputs to Delta-modulator



Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
 1-408-826-6002 (International)
 e-mail: ispPACs@latticesemi.com