

Features

■ Extensive Density and Package Options

- 1.5K to 41K LUT4s
- 65 to 576 I/Os
- Density migration supported

■ sysDSP™ Block (LatticeECP™ Versions)

- High performance multiply and accumulate
- 4 to 10 blocks
 - 4 to 10 36x36 multipliers or
 - 16 to 40 18x18 multipliers or
 - 32 to 80 9x9 multipliers

■ Embedded and Distributed Memory

- 18 Kbits to 645 Kbits sysMEM™ Embedded Block RAM (EBR)
- Up to 163 Kbits distributed RAM
- Flexible memory resources:
 - Distributed and block memory

■ Flexible I/O Buffer

- Programmable sysIO™ buffer supports wide range of interfaces:

- LVCMOS 3.3/2.5/1.8/1.5/1.2
- LVTTTL
- SSTL 3/2 Class I, II, SSTL18 Class I
- HSTL 18 Class I, II, III, HSTL15 Class I, III
- PCI
- LVDS, Bus-LVDS, LVPECL

■ Dedicated DDR Memory Support

- Implements interface up to DDR333 (166MHz)

■ sysCLOCK™ PLLs

- Up to 4 analog PLLs per device
- Clock multiply, divide and phase shifting

■ System Level Support

- IEEE Standard 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
- SPI boot flash interface
- 1.2V power supply

■ Low Cost FPGA

- Features optimized for mainstream applications
- Low cost TQFP and PQFP packaging

Table 1-1. LatticeECP/EC Family Selection Guide

Device	LFEC1	LFEC3	LFEC6/ LFCEP6	LFEC10/ LFCEP10	LFEC15/ LFCEP15	LFEC20/ LFCEP20	LFEC40/ LFCEP40
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	80
PFUs/PFFs	192	384	768	1280	1920	2464	5120
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	41.0
Distributed RAM (Kbits)	6	12	25	41	61	79	164
EBR SRAM (Kbits)	18	55	92	277	350	424	645
EBR SRAM Blocks	2	6	10	30	38	46	70
sysDSP Blocks ¹	—	—	4	5	6	7	10
18x18 Multipliers ¹	—	—	16	20	24	28	40
V _{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages and I/O Combinations:							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	
672-ball fpBGA (27 x 27 mm)						400	496
900-ball fpBGA (31 x 31 mm)							576

1. LatticeECP devices only.

Introduction

The LatticeECP/EC family of FPGA devices has been optimized to deliver mainstream FPGA features at low cost. For maximum performance and value, the LatticeECP (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general purpose features of LatticeECP devices without dedicated function blocks to achieve lower cost solutions.

The Lattice-ECP/EC FPGA fabric, which was designed from the outset with low cost in mind, contains all the critical FPGA elements: LUT-based logic, distributed and embedded memory, PLLs and support for mainstream I/Os. Dedicated DDR memory interface logic is also included to support this memory that is becoming increasingly prevalent in cost-sensitive applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeECP/EC family of FPGA devices. Synthesis library support for LatticeECP/EC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP/EC device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP/EC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.