

LatticeECP3 Family

Exceptional Performance – Uncommon Value

The LatticeECP3™ FPGA family is the newest addition to the value-based LatticeECP™ (Economy Plus) FPGA series. Utilizing an ultra low power, cost-optimized 65-nm process FPGA architecture, LatticeECP3 extends the functionality of prior generation families to new levels and provides designers with enhanced features and capabilities at a fraction of the power consumption and cost of competing devices.

LatticeECP3 offers up to 150K LUTs of logic capacity and up to 7Mbits of memory for system integration, cascadable high performance DSP blocks for processing intensive RF/IF and baseband designs, support for high-speed memory interfaces including DDR3 at 800Mbps and up to 1Gbps generic LVDS performance for ADC/DAC interfacing. LatticeECP3 devices enable you to further reduce cost with built-in high speed, low power transceivers for protocols including PCI Express, Ethernet (GbE, SGMII & XAUI), SDI (3G/HD/SD), Serial RapidIO, CPRI and OBSAI. LatticeECP3 devices also provide enhanced FPGA configuration options supporting encryption, multi-boot capability and fast configuration via parallel Flash.

With its low power characteristics, small die size, small form factor wirebond packaging, high performance DSP, I/O and multi-protocol SERDES, the LatticeECP3 family is ideally suited for wireless, wireline and video broadcast infrastructure applications.

FPGA Fabric Features and Capabilities

- **Low-Power, High-Value FPGA Fabric**
 - Low-power 65nm process with 4-input look-up table (LUT) fabric
 - Logic densities from 17K to 149K LUTs
 - Up to 7Mbits of Embedded Block RAM (EBR) and 303Kbits of distributed RAM
- **High-Speed Embedded SERDES**
 - Up to 16 channels with data rates from 250Mbps to 3.2Gbps
 - Less than 100mW power per channel at 3.2Gbps
 - Supports PCI Express, Ethernet (GbE, XAUI, SGMII), SMPTE, Serial RapidIO, CPRI, OBSAI
- **Flexible sysIO™ Buffers**
 - LVCMOS 33/25/18/15/12, PCI
 - SSTL3/2/18 & HSTL15 & HSTL18
 - LVDS, Bus-LVDS, MLVDS & LVPECL
 - 800Mbps DDR3
 - 1Gbps LVDS
- **Wide Range of Package & User I/O Options**
 - Up to 586 user I/O pins
 - Low-cost wirebond fpBGA packages
 - Density migration across all densities
 - Pb-free / RoHS-compliant
- **sysCLOCK™ PLL and DLL**
 - 2 DLLs per device, 2 to 10 PLLs per device



LatticeECP3 Features and Benefits

EMBEDDED SERDES

- 3.2Gbps operation with less than 100mW power per channel
- Built-in pre-emphasis and equalization
- Supports PCIe, Ethernet (GbE, XAUI, & SGMII), SMPTE, Serial RapidIO, CPRI and OBSAI
- Quad-based architecture with mix and match of different protocols within a quad
- Single-channel granularity for 3G/HD/SD SDI
- Support low latency variation CPRI links for multi-hop RRH applications

CASCADABLE DSP WITH ALU

- Fully cascadable slice for high performance filter and wide arithmetic functions
- Implement rounding and truncation functions with 54-bit cascadable arithmetic logic unit
- Multiply, accumulate, addition and subtraction
- Up to 320 18x18 multipliers

HIGH-SPEED I/O

- Pre-engineered DDR3 memory (800Mbps)
- 1Gbps LVDS
- On-chip termination

ADVANCED CONFIGURATION OPTIONS

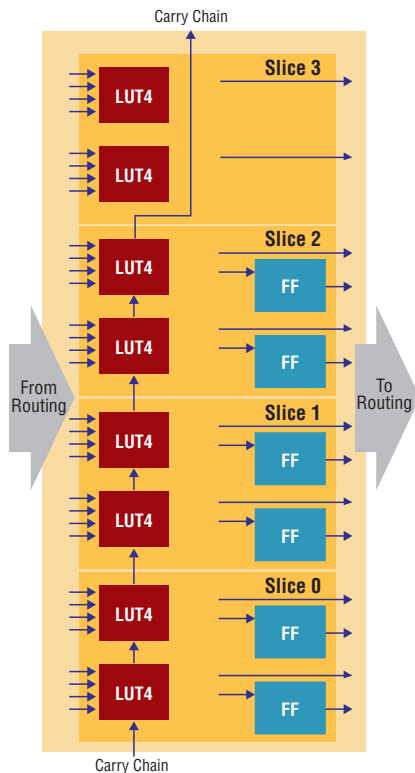
- Configure with SPI boot flash or parallel burst mode flash
- Protect your designs with 128-bit AES
- Multi-boot provides backup configuration copy
- TransFR™ I/O support updates while system operates

LatticeECP3 Architecture

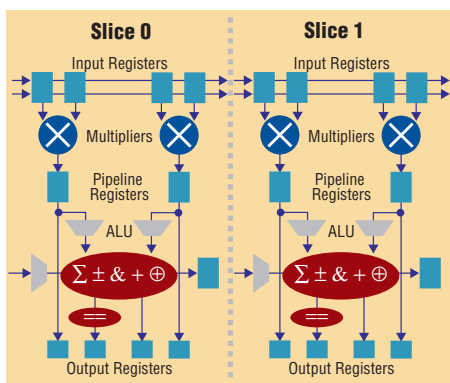
Architecture Overview

LatticeECP3 FPGAs utilize Lattice's third generation of cost optimized transceivers and a low-power 65-nm process FPGA architecture. Building on the successful LatticeECP2M™ FPGA family, LatticeECP3 devices deliver high-performance SERDES blocks, cascadable high-performance sysDSP, ultra-high logic and sysMEM™ embedded RAM, distributed memory, sysCLOCK PLLs, DDR3 memory interface, and sysIO buffers. LatticeECP3 provides a low-cost, low-power programmable solution for a wide variety of wireless and wireline applications.

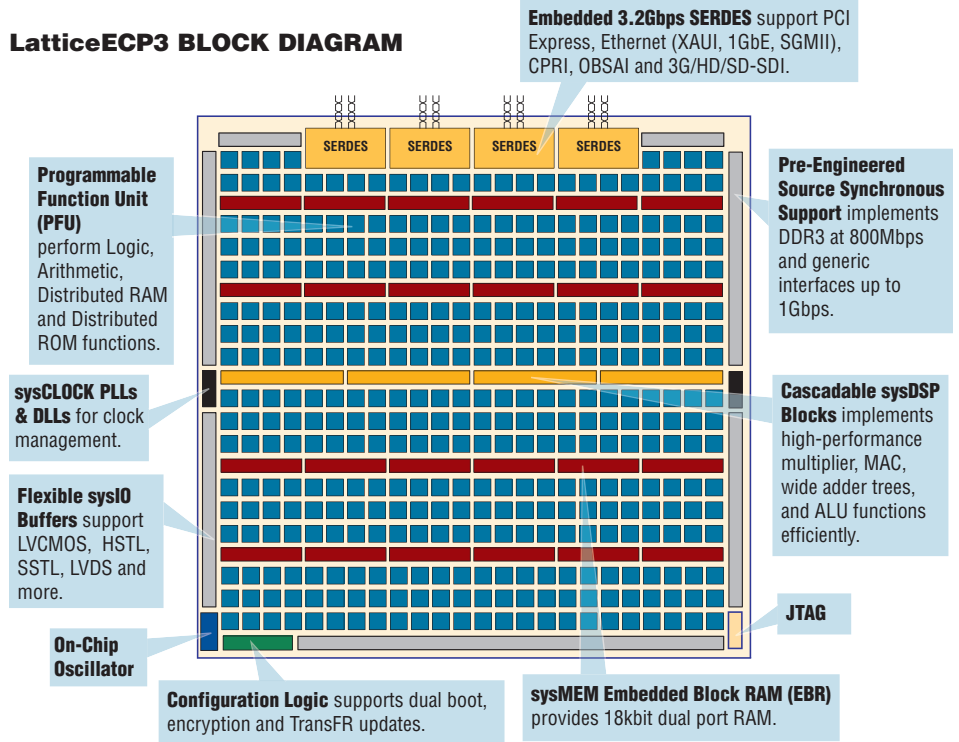
PROGRAMMABLE FUNCTION UNIT (PFU) BLOCK DIAGRAM



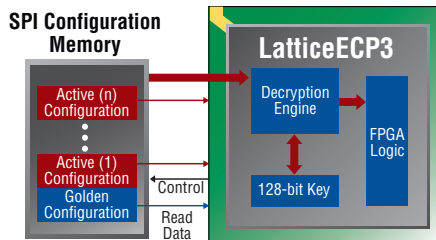
sysDSP BLOCK DIAGRAM



LatticeECP3 BLOCK DIAGRAM



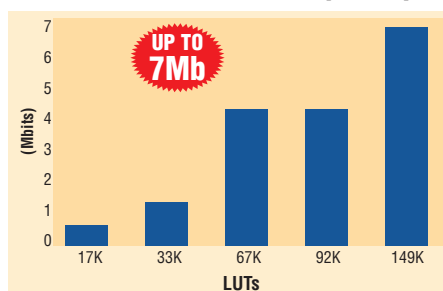
MULTI-BOOT AND 128-BIT AES ENCRYPTION



sysMEM CONFIG OPTIONS

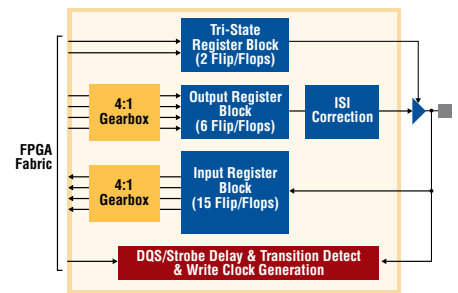
Single Port	Dual Port	Pseudo-Dual Port
16384 x 1	16384 x 1	16384 x 1
8192 x 2	8192 x 2	8192 x 2
4096 x 4	4096 x 4	4096 x 4
2048 x 9	2048 x 9	2048 x 9
1024 x 18	1024 x 18	1024 x 18
512 x 36	—	512 x 36

LatticeECP3 EBR SRAM (Mbits)

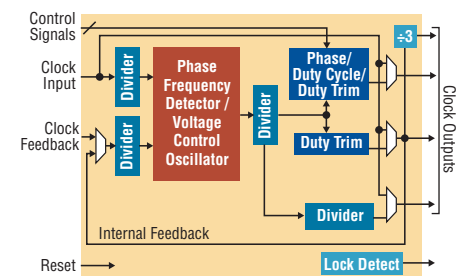


PRE-ENGINEERED SOURCE SYNCHRONOUS INTERFACES

- On-Chip Termination
- DDR3 (800 Mbps)
- 7:1 LVDS, ADC/DAC



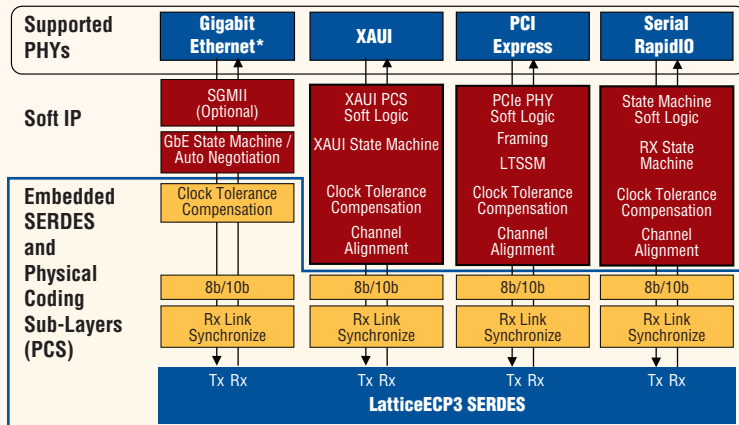
sysCLOCK PLL BLOCK DIAGRAM



High-Value, Low-Power Serial Protocol Solutions

LatticeECP3 MULTI-PROTOCOL STACK

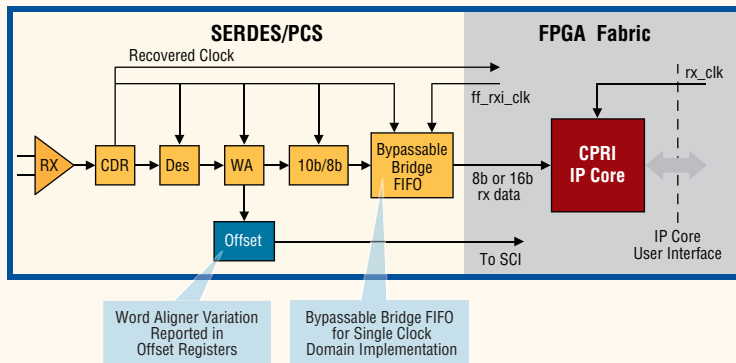
- Supports commonly used Ethernet protocols (1GbE, SGMII, and XAUI), Wireless protocols, such as CPRI and OBSAI, are supported by extension
- Supports PCI Express and Serial RapidIO



* CPRI/OBSAI Supported By Extension

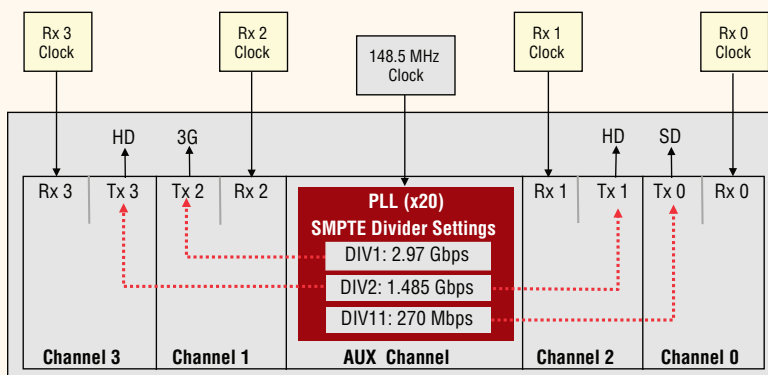
CPRI LOW LATENCY OPTION

- Supports data rates for up to 3.072 CPRI and OBSAI links
- Supports multi-hop RRH applications through innovative low-latency variation SERDES implementation
- Library of CPRI, OBSAI, SRIO, Ethernet and DSP cores and reference designs for single-chip RF and baseband implementations



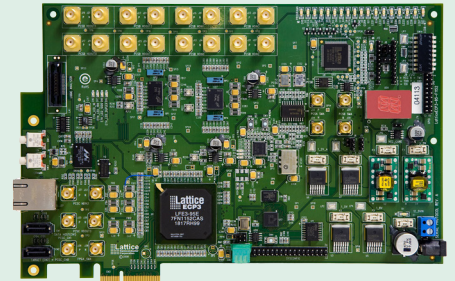
ENHANCED SMPTE SUPPORT

- Any rate, any channel, any direction for SD/HD and 3G
 - New x11 divider setting
 - Added independent Rx clocking per channel
- Truly independent Rx/Tx multi-rate support for SD/HD/3G!

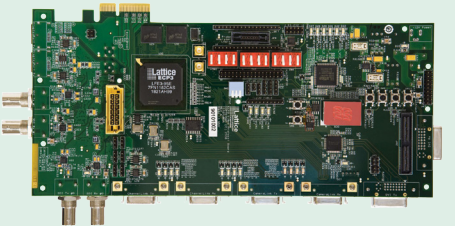


Evaluation & Development Boards

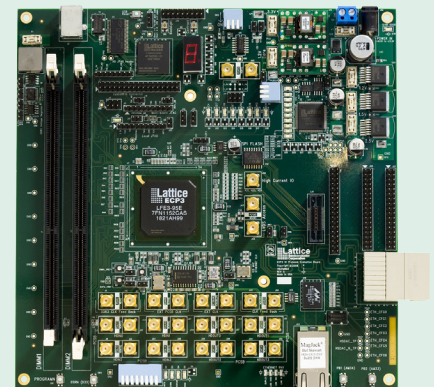
To accelerate your design development, Lattice offers several development boards to support LatticeECP3 designs. These boards enable you to evaluate the benefits and capabilities of LatticeECP3 devices in a lab setting.



The *LatticeECP3 Serial Protocol Board* provides a platform to evaluate the LatticeECP3 device's multi-protocol serial protocol functionality as well as DDR2 and DDR3 memory interfaces.



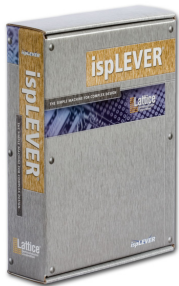
The *LatticeECP3 Video Protocol Board* provides a platform to evaluate the LatticeECP3 device's multi-rate 3G/HD/SDI and 7:1 LVDS capabilities. Breakout options for other display interfaces are also available.



The *LatticeECP3 I/O Protocol Board* provides a platform to evaluate DDR3 DIMMs and includes connectors for serial protocols as well as high-speed source synchronous LVDS I/O.

Design Made Simple with Advanced Design Software and IP

ispLEVER Software



Lattice's ispLEVER® software is a comprehensive design environment for the LatticeECP3 architectures. The ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floorplanning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Aldec® and Synplicity® are included with ispLEVER.



ispLeverCORE™ Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used functions, including:

- PCI Express x1/x4
 - 10Gb Ethernet MAC, Tri-speed Ethernet, XAUI, SGMII
 - Serial Rapid I/O, CPRI
 - ADC/DAC reference designs
 - DDR1, 2 & 3 memory controllers
 - FFT/IFFT compiler
 - FIR compiler
 - LatticeMico32™
 - SMPTE/SDI multi-rate PHY
 - DUC/DDC reference designs
- and more.....

For additional IP cores, go to www.latticesemi.com/ip. Lattice's ispLeverCORE Connections partners also offer a wide range of IP for the LatticeECP3 family.

LatticeECP3 (Economy Plus FPGAs with SERDES, sysDSP Blocks, & Source Synchronous I/O)

Parameter	ECP3-17	ECP3-35	ECP3-70	ECP3-95	ECP3-150
LUTs (K)	17	33	67	92	149
Number of EBR SRAM Blocks	30	72	240	240	372
EBR Block SRAM (K bits)	552	1327	4420	4420	6850
Distributed RAM (K bits)	36	68	145	188	303
18x18 Embedded Multipliers	24	64	128	128	320
3.2Gbps SERDES Channels	4	4	12	12	16
Maximum Available I/O	222	310	490	490	586
Number of PLLs/DLLs	2+2	4+2	10+2	10+2	10+2
Packages & SERDES / I/O Combinations					
256-ball ftBGA (17 x 17 mm)	4/133	4/133			
484-ball fpBGA (23 x 23 mm)	4/222	4/295	4/295	4/295	
672-ball fpBGA (27 x 27 mm)		4/310	8/380	8/380	8/380
1156-ball fpBGA (35 x 35 mm)			12/490	12/490	16/586

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