

# LatticeECP & EC Families

## Exceptional Performance with Uncommon Value

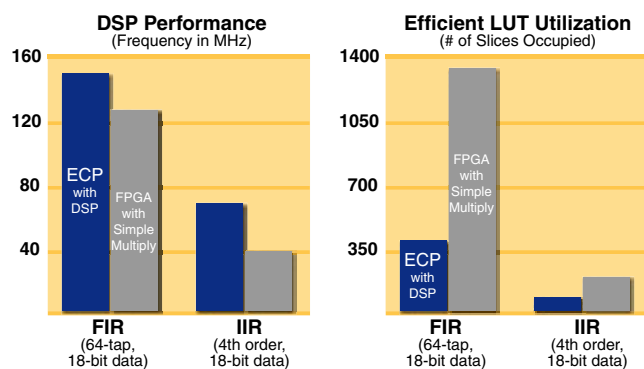
Since 1985, Lattice has led the programmable logic industry by bringing the best together to provide design engineers with the most innovative programmable products. Now, Lattice brings you a new generation of optimized low-cost FPGAs. For maximum performance and value, the LatticeECP™ (Economy Plus) FPGA concept combines an efficient FPGA fabric with high-speed dedicated functions. Lattice's first family to implement this approach is the LatticeECP-DSP (Economy Plus DSP) family, providing dedicated high-performance DSP blocks on-chip. The LatticeEC™ (Economy) family supports all the general-purpose features of LatticeECP devices without dedicated function blocks to achieve even lower cost solutions.

The LatticeECP and EC families both utilize a silicon-efficient FPGA fabric in which I/O capability, distributed memory, embedded memory, logic and routing have been optimized to provide the best features at value-conscious prices.

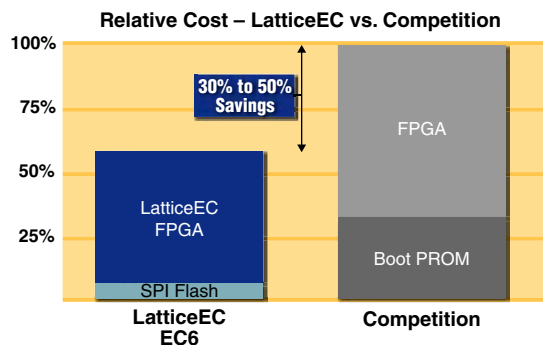
The LatticeECP-DSP devices are ideal for use in applications in which cost-effective DSP functionality is needed. Such applications include software defined radio, wireless communications, military applications and video processing equipment. LatticeEC devices are ideal for general non-DSP applications such as low-cost networking, blade servers, network access equipment, consumer electronics, industrial, medical and automotive applications.



## Superior DSP Performance and Utilization



## The Most Affordable FPGA Solution



Note: Based on competition's low volume, published pricing as of June 1, 2004.

## Key Features and Benefits

- **Low-Cost FPGAs**
  - Features optimized for mainstream applications
  - Balanced logic / memory / I/O resources
- **High Performance sysDSP™ Blocks (LatticeECP-DSP)**
  - Multiply, accumulate, addition and subtraction
  - Input, intermediate and output pipeline registers
  - 4 to 10 sysDSP blocks per device
    - Each block supports multiple 9x9, 18x18, 36x36 multipliers
- **Extensive Density and Package Options**
  - 1.5K to 41K LUT4s; 67 to 576 I/Os
  - Density migration supported
  - TQFP, PQFP and fpBGA packaging options
  - Pb-free / RoHS compliant options
- **Embedded and Distributed Memory**
  - 18 Kbits to 645 Kbits sysMEM™ Embedded Block RAM (EBR)
  - Up to 164 Kbits distributed RAM
- **Flexible I/O Buffer**
  - Hot Socketing
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8/1.5/1.2
    - LVTTTL
    - SSTL 3/2 Class I, II, SSTL18 Class I
    - HSTL 18 Class I, II, III, HSTL15 Class I, III
    - PCI
    - LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
  - Implements interface up to DDR333 (166MHz)
- **sysCLOCK™ PLLs**
  - Up to 4 analog PLLs per device
  - Clock multiply, divide and phase shifting
- **System Level Support**
  - Standard IEEE 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
  - Industry standard, third-party SPI boot flash interface
  - 1.2V power supply

# LatticeECP & EC Architecture

## Architecture Overview

The LatticeECP and EC families are designed to offer exceptional functionality, performance and value. Built with an extremely efficient architecture, these low-cost FPGAs deliver high performance DSP blocks, sysMEM embedded RAM blocks, distributed memory, sysCLOCK PLLs, DDR memory interface, sysIO buffers, and more.



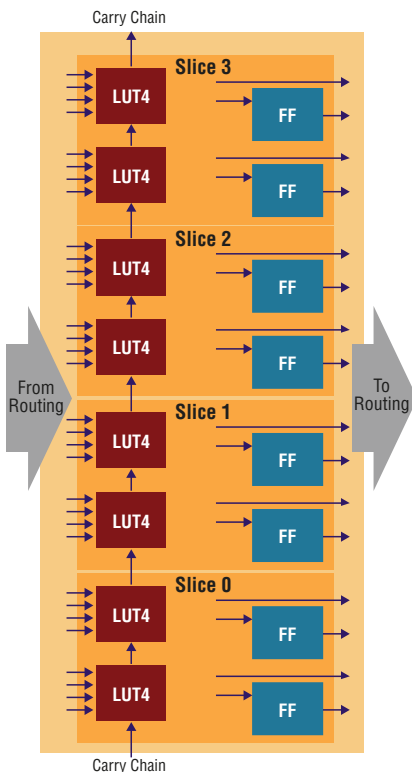
Low-cost LatticeECP devices bring the best together with high-performance dedicated functions, fast DDR interface, and embedded memory.

## Programmable Function Unit Blocks (PFU)

The core of LatticeECP and EC devices consists of Programmable Functional Units (PFU) and PFUs without RAM (PFF). The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions.

- Four Slices per PFU
- Each Slice Individually Programmable
- Slices can be Concatenated for Longer Functions
- PFUs can be Concatenated for Complex Functions

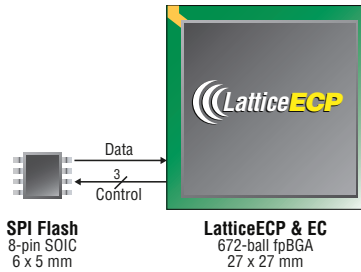
## PFU BLOCK DIAGRAM



## Low-cost SPI Flash Memory Configuration

LatticeECP and EC are the first FPGAs in the marketplace to support direct boot-up from industry standard, third-party, SPI Serial Flash memory. Low-cost SPI memories are ideal for high-volume applications. They offer fast configuration times, lowest costs, and a smaller PCB footprint.

- Optimized SPI Memory Provides up to 75% Lower Costs vs. Proprietary Boot PROM Solutions
- ~75% Smaller Package Size and PCB Footprint – Perfect for Tight Board Space Constraints



## High Speed sysDSP Blocks

LatticeECP-DSP devices include up to ten high performance sysDSP blocks per device. sysDSP blocks are optimized for processing intensive applications and allow designers to quickly implement DSP functions. Each sysDSP block supports:

- A Range of Multiplier Widths:
  - One 36x36
  - Four 18x18
  - Eight 9x9
- Programmable Addition, Subtraction, and Accumulate Modes
- Programmable Pipelining – Input, Intermediate and Output
- 250MHz Performance

One LatticeECP-DSP device can provide up to 10,000 Million Multiply Accumulates per second (MMACs)!

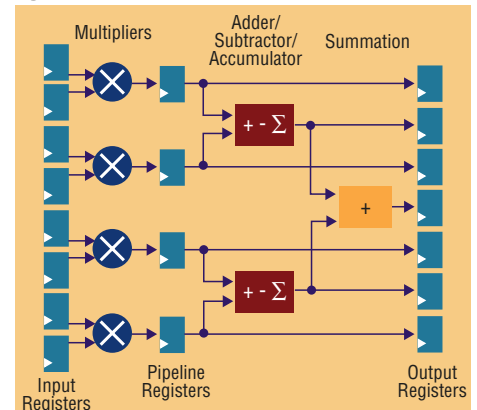
## LatticeECP & EC Block Diagram

**Programmable Function Unit (PFU)** blocks are optimized to perform logic + RAM (25% of blocks) and logic only (75% of blocks).

**sysCONFIG™ Port** supports SPI, serial and parallel configuration.

**Programmable I/O Cells (PIC)** include sysIO buffers that support over 20 interfaces at up to 700Mbps and 333Mbps DDR memory interfaces.

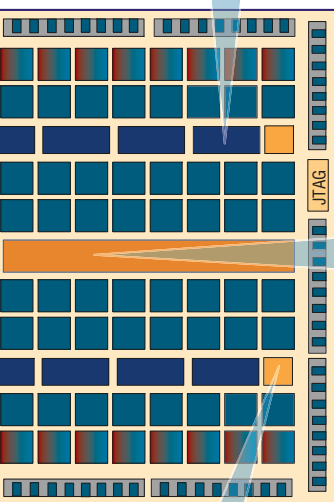
## sysDSP BLOCK DIAGRAM



# LatticeECP & EC Applications

- Routers • SAN • Blade Servers • Line Cards • Military • Wireless • Software Defined Radio • DSL Modems • Cable Modems • Satellite Modems • Medical Imaging • Home Video Editing • Video on Demand • DVD-RW • LCD and PDP Monitors • HDTV Monitors • Residential Gateways • GPS Navigation • Digital Camcorders • Bridging • DSP Co-processing • PCI and Parallel Interconnect • MPEG-4 Hardware Acceleration • Memory Interfaces – SRAM, SDRAM, DDR DRAM, and Flash • Peripherals – IrDA, UART, I2C, and SPI • and more

**sysMEM Embedded Block RAM (EBR)** provides 9kbit true dual port RAM at up to 275MHz.



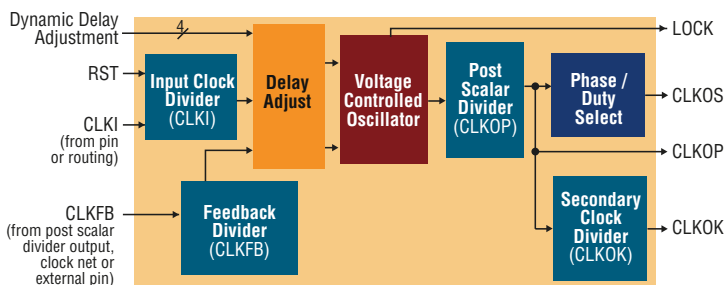
**sysDSP Blocks** implement multipliers, adders, subtractors, accumulators at up to 250MHz. (ECP-DSP only)

**sysCLOCK PLLs** for clock management.

## sysCLOCK PLLs for Timing Control

- Frequency Range 33 to 420MHz
- Low Output Period Jitter (+/-100ps)
- Programmable Phase/Duty Cycle (45 degree steps)
- Programmable Input, Scaling, Feedback and Secondary Counters
- Internal and External Feedback

## sysCLOCK PLL BLOCK DIAGRAM

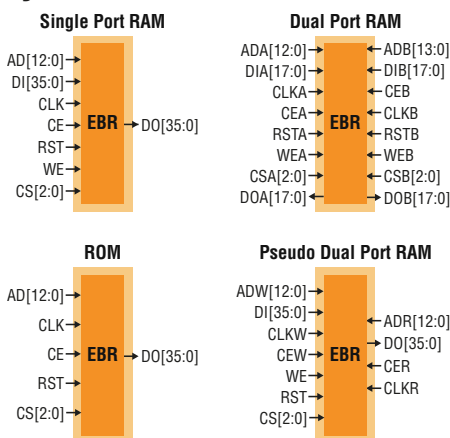


## sysMEM Embedded Block RAM (EBR)

LatticeECP and EC FPGAs include flexible sysMEM EBR blocks. sysMEM EBR blocks provide on-chip memory resources to support a broad range of features.

- 18K Bits to 645K Bits sysMEM Embedded Block RAM (EBR)
- 275MHz Operation
- Multiple Blocks per Device
- Configurable Width and Depth
- Single-Port, Dual-Port and Pseudo-Dual-Port
- Bus Size Matching
- RAM Initialization and ROM Operation
- Memory Cascading

## sysMEM EBR PRIMITIVES



## sysIO Buffer Supports High-Bandwidth I/O Standards

With Lattice's sysIO interfaces, LatticeECP and EC devices can easily communicate with a variety of devices, supporting many single-ended and differential I/O standards.

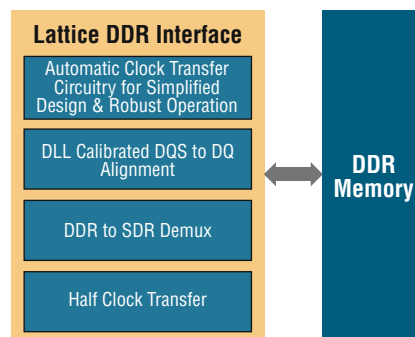
- sysIO Interfaces Support
  - LVCMOS / LVTTTL
    - Hotsocketing capable
    - Programmable slew rate
    - Programmable drive strength
    - Programmable pull-up, pull-down, bus friendly
    - Programmable open drain
  - PCI, LVDS, SSTL, HSTL, Differential HSTL, Differential SSTL, LVPECL, BLVDS, RSDS
  - 700Mbps+ I/O buffers
  - 333Mbps DDR memory interfaces
- Eight I/O Banks Per Device

## DDR Interface Support

LatticeECP and EC devices provide designers with dedicated DDR interfaces to easily connect LatticeECP and EC FPGAs to external DDR memory.

- Precision DQS Delay Control
- Dedicated DDR Registers (For Mux/Demuxing)
- Automatic DQS to System Clock Domain Transfer
- Half Clock Transfer
- High Performance (166MHz+)

## SUPERIOR DDR INTERFACE



## Design Made Simple with Advanced Design Software and IP

### ispLEVER Software

Lattice's ispLEVER® software is a comprehensive design environment for the LatticeECP and EC architectures. The ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floor-planning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Mentor Graphics and Synplicity are included with ispLEVER.



The ispLEVER design tools also include a comprehensive interface to The MathWorks MATLAB and Simulink tools for DSP design. Lattice's DSP solution features a seamless design flow that includes 30+ commonly used DSP blocks to auto-generate HDL and test benches from the Simulink Graphical Editor.

### ispLeverCORE™ Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used functions, including:

- Interface and Memory Control Functions
  - PCI Master/Target and Target 64-bit and 32-bit
  - DDR Memory Controllers
  - 10/100 Ethernet MAC
  - Gigabit Ethernet MAC
  - DMA Controller
- DSP Functions
  - FIR Filters
  - Reed-Solomon Encoder and Decoder
  - Turbo Encoder and Decoder
  - Viterbi Decoder
  - Convolutional Encoder
  - NCO
  - Interleaver/Deinterleaver
- Encryption Functions



For additional IP cores, go to [www.latticesemi.com/ip](http://www.latticesemi.com/ip). Lattice's ispLeverCORE Connections partners also offer a wide range of IP for the LatticeECP and EC families.

### Device Selection Guide

Parameter	EC1	EC3	ECP6 / EC6	ECP10 / EC10	ECP15 / EC15	ECP20 / EC20	ECP33 / EC33	ECP40 / EC40
PFU/PFF Rows	12	16	24	32	40	44	64	64
PFU/PFF Columns	16	24	32	40	48	56	64	80
Number of PFUs/PFFs	192	384	768	1280	1920	2464	4096	5120
sysDSP Blocks*	—	—	4	5	6	7	8	10
18x18 Embedded Multipliers*	—	—	16	20	24	28	32	40
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8	41
Distributed RAM (K bits)	6	12	25	41	61	79	131	164
EBR Block SRAM (K bits)	18	55	92	277	350	424	535	645
Number of EBR SRAM Blocks	2	6	10	30	38	46	58	70
V <sub>CC</sub> Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4	4
<b>Packages &amp; I/O Combinations</b>								
100-pin TQFP (14 x 14 mm)	67	67						
144-pin TQFP (20 x 20 mm)	97	97	97					
208-pin PQFP (28 x 28 mm)	112	145	147	147				
256-ball fpBGA (17 x 17 mm)		160	195	195	195			
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360	
672-ball fpBGA (27 x 27 mm)						400	496	496
900-ball fpBGA (31 x 31 mm)								576

\* ECP-DSP devices only

### Applications Support

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