

Features

- **Complete 10Gb Ethernet Physical Coding Sublayer (PCS) Solution Based on the ORCA 10 Gbits/s Line Interface (ORLI10G) FPSC, Enabling Flexible 10GbE LAN/WAN Application Solutions.**
- **IP Targeted to the ORLI10G Programmable Array Section Implements Functionality Conforming to IEEE Standard 802.3ae, Including:**
 - 10 GbE Media Independent Interface (XGMII) for Interfacing with 10Gb Ethernet MACs.
 - Elastic Store Buffers for Clock Domain Transfer to/from the XGMII Interface.
 - $X^{58} + X^{39} + 1$ Polynomial 10GbE Scrambler/Descrambler Blocks.
 - Receive Direction 64b-to-66b Gearbox, 66-bit Word Aligner and 64b/66b Decoder.
 - Transmit Direction 64b/66b Encoder and 66b-to-64b Gearbox.
 - Interface with the High-speed Line Interface Block Embedded in the ORLI10G which Implements an OIF Standard (OIF 99.102.5) 10Gb 16-bit Interface (XSBI).

- **ORCA Bitstream Format Allows Direct Downloading and Turnkey Functionality.**

General Description

The 10 Gigabit Ethernet (10 GbE) Physical Coding Sublayer (PCS) solution from Lattice Semiconductor enables creation of system solutions for applications using 10 Gigabit Ethernet as defined by IEEE 802.3ae. This IP solution includes soft IP that is targeted to the programmable array section of the ORCA[®] ORLI10G FPSC. The ORLI10G contains a 10 Gbits/s Transmit and Receive Line Interface, and when combined with this PCS core, enables flexible 10GbE LAN/WAN application solutions.

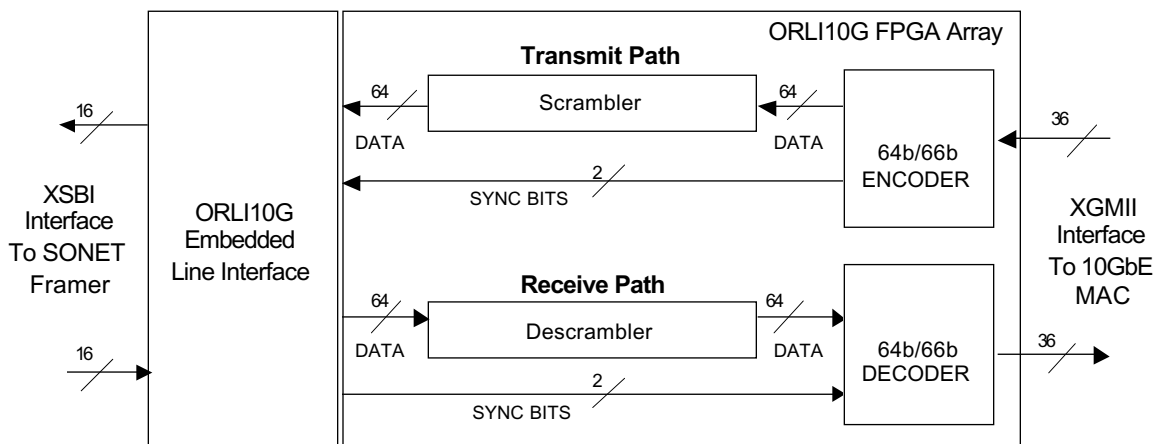
The 10 GbE PCS IP solution includes a 10GbE scrambler/descrambler, 10 GbE Media Independent Interface (XGMII) and 64b/66b encoder/decoder functions. These functions are implemented in software to provide flexibility while the specifications for these interface functions are being finalized. This IP interfaces with the high-speed line interface block embedded in the ORLI10G which implements an OIF standard (OIF 99.102.5) 10Gb 16-bit Interface (XSBI).

The PCS IP is provided in ORCA bitstream format to allow direct downloading and turnkey functionality. The PCS solution comes with the following documentation and files:

- Data sheet
- User's guide
- Solution bitstream
- Interface loopback bitstreams to support initial hardware debugging

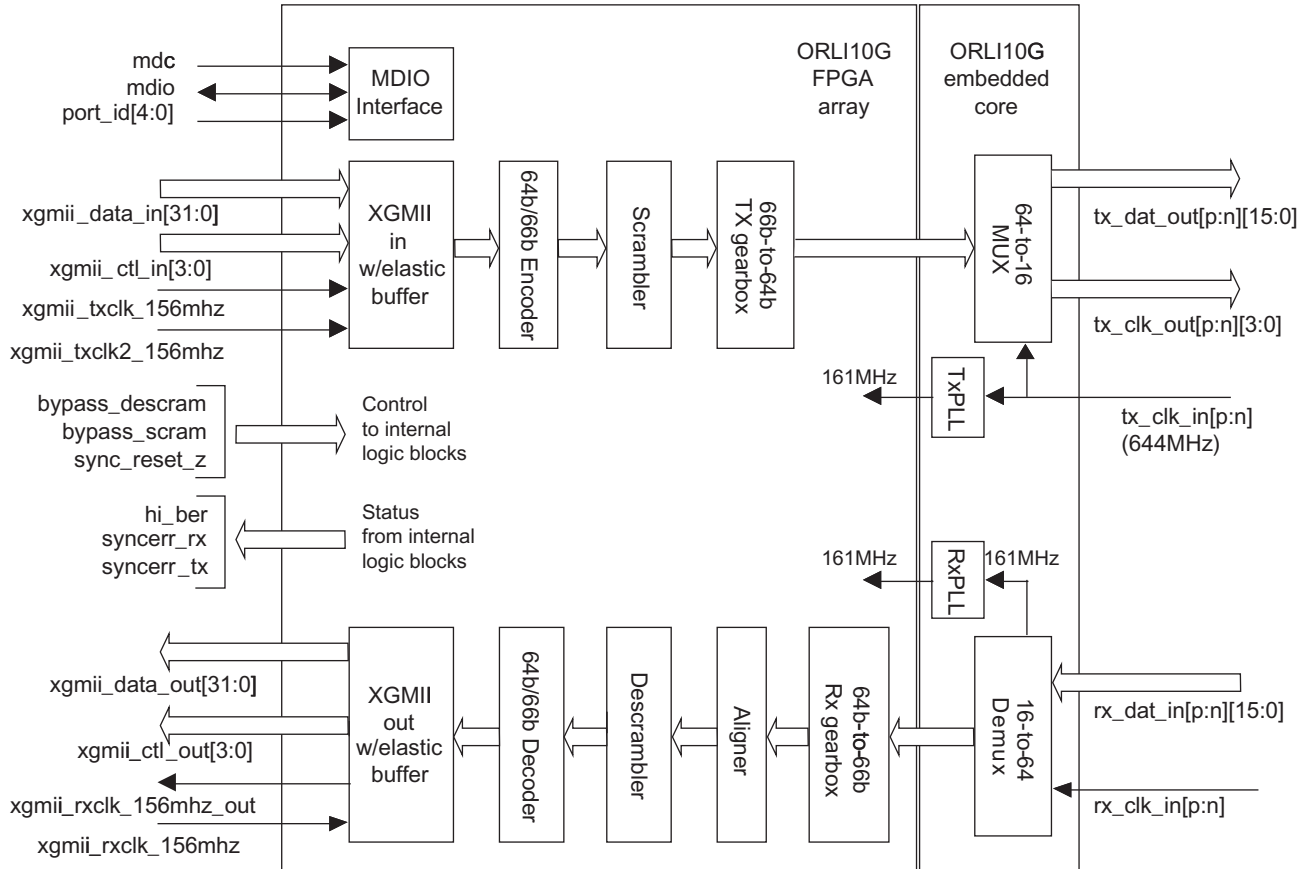
Block Diagram

Figure 1. 10 Gigabit Ethernet Dataflow



A block diagram of the PCS solution is shown in Figure 2. The PCS IP solution implements functionality conforming to Clause 49 of IEEE 802.3ae/D3.0, PCS for 64b/66b type 10GBASE-R. The primary function of this solution is to support the encoding and decoding of data from the eight octet XGMII structure to 66-bit blocks based on 64b/66b encoding/decoding, and then to transfer the data to/from the XSBI interface in 16-bit blocks.

Figure 2. PCS Solution Block Diagram



XGMII and Elastic Buffers

The 10Gigabit Media Independent Interface (XGMII) supported by the PCS solution conforms to Clause 46 of IEEE 802.3ae. The XGMII is composed of independent transmit and receive paths. Each direction uses 32 data signals, four control signals and a clock. The 32 data signals in each direction are organized into four lanes of eight signals each. Each lane is associated with a control signal. The control signal for each lane is de-asserted when a data octet is being sent on the corresponding lane, and asserted when a control character is being sent.

The XGMII supports Double Data Rate (DDR) transmission, i.e. the data and control input signals are sampled on both the rising and falling edges of the corresponding clock. The PCS XGMII input data is sampled based on an input clock typically sourced from the MAC running at 156.25MHz, one-sixty-fourth of the 10Gb data rate. The PCS XGMII output data is referenced to a forwarded clock that is phase locked to a 156.25MHz (typical) input reference.

The XGMII blocks incorporate elastic buffers that accommodate small differences between MAC and line interface timing by inserting or deleting idle characters. No idle is inserted during data transmission.

XSBI and Mux/Demux

The 10Gigabit Sixteen Bit Interface (XSBI) capability supported by the PCS solution and implemented in the ORL10G embedded core conforms to Clause 51 of IEEE 802.3ae. The XSBI consists of a 16-bit LVDS receive data bus and a 16-bit LVDS transmit bus operating at 644.53 Mbits/s per input/output pair for 10 Gigabit Ethernet

applications. In the receive direction, all 16 input data signals are timed from a single high-speed LVDS input clock signal operating at 644.53 MHz. In the transmit direction, each 4-bit group of transmit data signals has a separate clock output reference. The transmit output clocks are phase locked to a 644.53 MHz input reference.

16b-to-64b demultiplexing and 64b-to-16b multiplexing blocks are implemented in the ORLI10G embedded core to convert between the 644.53 MHz XSBI data rate and the 161.13 MHz internal clock rate of the PCS processing logic implemented in the ORLI10G FPGA array.

64b/66b Encoding/Decoding

The PCS maps XGMII signals to/from the 66-bit blocks using the 64b/66b transmission coding scheme specified in Clause 49 of IEEE 802.3ae. The first two bits of a block are the synchronization header used to delineate the 66-bit block boundaries and to designate block type. Blocks may be either data blocks or control blocks. Data blocks contain eight 8-bit data characters. Control blocks begin with: an 8-bit block type field which indicates the format of the remainder of the block; and eight characters which may be 7-bit control codes, 4-bit O codes, or 8-bit data characters.

PCS Transmit Process

The 64b/66b encoder implements the PCS transmit process that generates blocks based on the data and control signals received from the XGMII. The transmit process state machine provides packet boundary protection, verifying the proper sequence of start of packet (S), end of packet (T), and that control blocks (C) and data blocks (D) are transmitted. Error (E) blocks are generated if improper sequences are detected.

Scrambler

The payload of each block is scrambled with a self-synchronizing scrambler based on the polynomial $G(X) = 1 + X^{39} + X^{58}$. There is no requirement on the initial value of the scrambler. The sync header bits bypass the scrambler.

Transmit Gearbox

The transmit gearbox transforms a 66-bit word from the scrambler at 156.25 MHz to a 64-bit word at 161.13 MHz. The 156.25 MHz clock is created by a digital 32/33 divider from the 161.13 MHz clock.

PCS Receive Process

The receive gearbox, aligner and 64b/66b decoder implement the PCS receive process that decodes blocks to produce the data and control signals for transmission to the XGMII. The receive process state machine provides packet boundary protection, verifying the proper sequence of start of packet (S), end of packet (T), and that control blocks (C) and data blocks (D) are received. Error (E) blocks are generated if improper sequences are detected.

Receive Gearbox and Aligner

The receive gearbox transforms a 64-bit word from the embedded core at 161MHz to a 66-bit word at 156.25MHz. The 156.25 MHz clock is created by a digital 32/33 divider from the 161.13 MHz clock. The aligner locks onto the 66-bit blocks in the receive bitstream by locking onto the position of the sync header.

Bit Error Rate Monitor

The aligner implements the bit error rate monitor state machine. This state machine counts the number of sync header errors detected in a 125 μ s window. A high bit error rate (hi_ber) condition is indicated if more than 16 sync header errors are detected in 125 μ s.

Management Data Input/Output (MDIO) Interface

The MDIO interface provides access to the internal PCS registers. The register access mechanism corresponds to Clause 45 of the IEEE 802.3ae standard. The PCS core provides access to PCS registers 0x0000-0x0003 as specified in 802.3ae. A few registers in the vendor-specific address space have been allocated for implementation-specific control/status functions.

PCS Registers

The registers supported in the PCS core are shown in Tables 1 and 2. These registers are accessed via the MDIO interface as described in Sec. 2.2.10. The notation a.b.c in Table 2 is used to define the registers where a indicates the device, b the register address, and c the register bit for that address. Events are latched to a '1' and the corresponding r/w register bit is set. The register bits are cleared on a read.

In accordance with IEEE 802.3ae, the PCS core returns a value of zero for access of all undefined and unsupported registers and bits. Writes to undefined and read-only registers and bits have no effect.

Table 1. Register Map for PCS IP (Device Address = 3)

Register Address (Hex.)	Register Name
0	PCS Control
1	PCS Status
2,3	PCS Identifier: PCS_ID0=0x0000 and PCS_ID1=0x0003
0x8000-0x8003	PCS IP Vendor Specific

Table 2. PCS Registers

Bit(s)	Name	Description	R/W
Control Register			
3.0.15	Reset	1 = PCS reset	R/W
3.0.[14:0]	Reserved	Read = 0, Write = no effect	RO
Status Register			
3.1.[15:14]	Device Present	[15:14] = 10	ROC
3.1.[13:10]	Reserved	Read = 0, Write = no effect	RO
3.1.9	PCS High BER	1 = high BER, 0 = low BER	ROC
3.1.8	PCS Sync Done	1 = PCS synchronized to received frames 0 = PCS not synchronized to received frames	ROC
3.1.[7:0]	Reserved	Read = 0, Write = no effect	RO
PCS Identifier Registers			
3.2.[15:0]	PCS_ID0	[15:0] = 0x0000	RO
3.3.[15:0]	PCS_ID1	[15:0] = 0x0003	RO
Vendor Specific Registers			
3.8000.[15:0]	Reserved	Read = 0, Write = no effect	RO
3.8001.[15:0]	64b/66b sync loss counter	Increments each time sync is lost	RO
3.8002.[15:0]	64b/66b sync time counter	Counts time (clock cycles) to resync	RO
3.8003.[15:4]	Reserved	Read = 0, Write = no effect	RO
3.8003.3	Descrambler bypass	1 = bypass descrambler 0 = enable descrambler	RO
3.8003.2	Scrambler bypass	1 = bypass scrambler 0 = enable scrambler	RO
3.8003.1	Reserved	Read = 0, Write = no effect	RO
3.8003.0	Reserved	Read = 0, Write = no effect	RO

RO = read-only

ROC = read-only, clear on read

R/W = read/write

Signal Descriptions

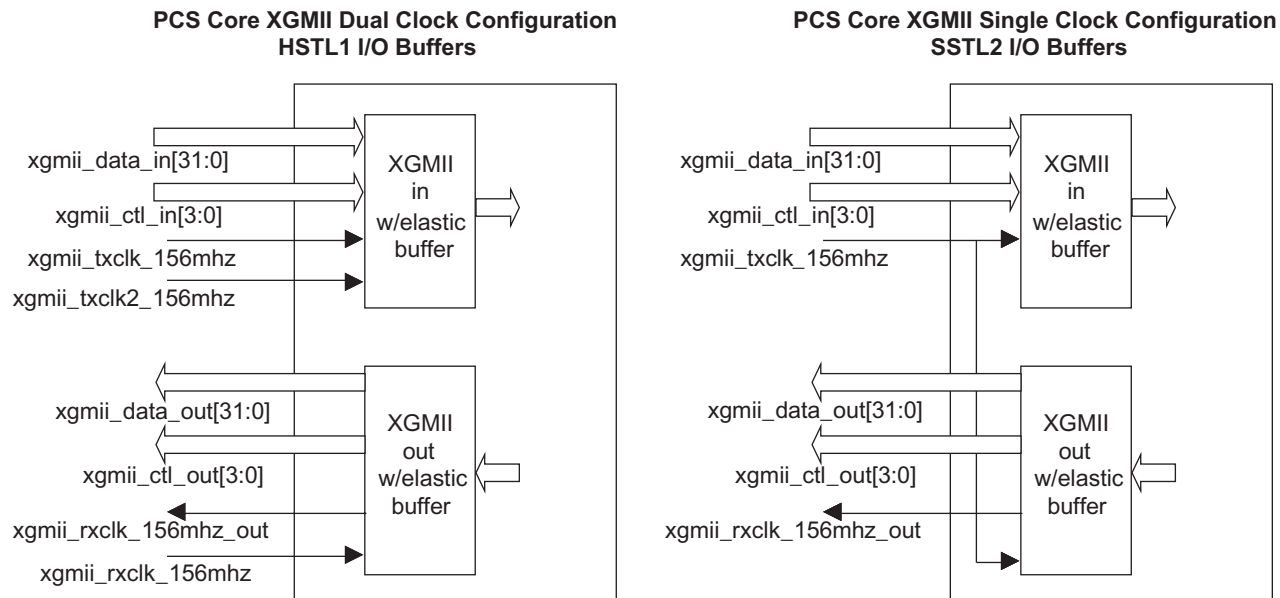
Table 3 defines all I/O interface ports available in this core.

Table 3. PCS Solution I/O

Signal Name	Direction	Description
XGMII Signals		
xgmii_data_in[31:0]	input	64-bit wide DDR XGMII input data.
xgmii_ctl_in[3:0]	input	Per-byte DDR XGMII control inputs.
xgmii_txclk_156mhz	input	156MHz XGMII transmit (PCS input) clock.
xgmii_txclk2_156mhz	input	156MHz XGMII transmit (PCS input) clock 2 (provided to meet timing requirements across all XGMII data and control inputs).
xgmii_data_out[31:0]	output	64-bit wide DDR XGMII output data.
xgmii_ctl_out[3:0]	output	Per-byte DDR XGMII control outputs.
xgmii_rxclk_156mhz	input	XGMII receive (PCS output) reference clock.
xgmii_rxclk2_156mhz_out	output	Forwarded XGMII receive (PCS output) clock.
XSBI Signals		
tx_clk_in[n:p]	input	644MHz LVDS transmit reference clock input.
tx_clk_out[n:p][3:0]	output	LVDS transmit direction clock outputs (one per four data bits).
tx_dat_out[n:p][15:0]	output	LVDS transmit direction data outputs.
rx_clk_in[n:p]	input	LVDS receive direction clock input.
rx_dat_in[n:p][15:0]	input	LVDS receive direction data inputs.
MDIO Interface Signals		
mdio	input/output	MDIO bi-directional data.
mdc	input	MDIO clock.
port_id[4:0]	input	5-bit port ID for PHY device.
PCS Soft IP Control and Status Signals		
sys_reset_z	input	System reset (active low).
bypass_descram	input	Scrambler disable (active high).
bypass_sscram	input	Descrambler disable (active high).
hi_ber	output	High bit error rate status signal from aligner (1 = high BER).
syncerr_rx	output	Receive sync error indication from rx gearbox (1 = error).
syncerr_tx	output	Transmit sync error indication from tx gearbox (1 = error).
ORLI10G Embedded Core Control and Global I/O		
pll_bypass	input	Enables bypass mode for both receive and both transmit PLLs.
pwrndn	input	Power down all LVDS links and both receive and both transmit PLLs.
reset_rx	input	Resets the receive PLLs and the demultiplexer block.
reset_tx	input	Resets the transmit PLLs and the multiplexer block.
ORLI10G FPGA Configuration I/O		
Please refer to the ORCA Series 4 FPGA Data Sheet and the ORLI10G Data Sheet for information on the various configuration options.		

Core Configurations

The core is provided in bitstream format, ready to use. There are no user configurable parameters. Two different PCS IP bitstreams are available which support different XGMII configurations as shown in Figure 3. One configuration supports HSTL1 I/O buffers and a dual clocking arrangement in which the transmit and receive sides of the XGMII interface are timed with different clock inputs. The second configuration supports SSTL2 I/O buffers and a single clock inputs used to time both the transmit and receive sides of the XGMII.

Figure 3. PCS XGMII Configurations Supported

Clause 46 of IEEE 802.3ae specifies HSTL1 I/O with a 1.5V output buffer supply voltage for all XGMII signals. The HSTL1 specifications comply with EIA/JEDEC Standard EIA/JESD8-6 using Class I output buffers with output impedance greater than 38Ω to ensure acceptable overshoot and undershoot performance in an un-terminated interconnection. The thresholds and parametric values for HSTL1 XGMII signals are specified in IEEE 802.3ae.

SSTL2 is a non-inverting bidirectional capability specified to comply with JEDEC Standard JESD8-9 operating at 2.5V supply voltages. This capability is intended to provide improved performance in situations where buses must be isolated from relatively large stubs. The operating specifications and termination scheme for this capability may be found in the ORCA ORLI10G FPSC Data Sheet.

Reference Information

The PCS solution is compliant with IEEE Draft P802.3ae/D3.0 except where specifically noted. A complete description of PCS functionality is given in the draft specification.

Additional information on implementing this solution is contained in the following documents:

- ORLI10G 10 Gbits/s Transmit and Receive Line Interface FPSC Data Sheet
- ORCA Series 4 FPGAs Data Sheet

These documents are available on the Lattice web site at www.latticesemi.com.