



# ***CLOCK NETWORK MANAGEMENT ISSUES***

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## ***The ispClock™5500 Family***

**In-System Programmable Clock Generator with Universal Fan-out Buffer**

**A Lattice Semiconductor White Paper**

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## ***Clock Network Management Issues***

The key to increasing the overall performance of a synchronous design is increasing the frequency of the clock network. However, factors such as timing margin, signal integrity, synchronizing related clock edges, etc., dramatically increase the complexity of clock network design. Traditionally, clock networks have been designed using simple components such as fan-out buffers, clock generators, delay lines, zero delay buffers and frequency synthesizers. Timing errors due to unequal PCB trace lengths have been addressed by using trace length matching through serpentine trace layouts. Trace impedance mismatch with the output driver impedance has frequently been mitigated by trial and error selection of series resistors. Multiple signaling standards further complicated synchronizing clock edges. Until now, these three challenges have been met with multiple and often less than ideal solutions. The following describes some of these challenges.

### ***Increased clock frequency results in reduced timing margin***

Increasing clock frequency reduces the time available for transferring data from one device to the other. With the increase in the frequency of operation (particularly >66 MHz), those designing clock nets are required to carefully consider timing parameters such as device set up and hold time, signal flight time across the circuit board trace, clock timing differences between devices on a common clock net, etc. If timing margin rules are violated, the circuit board will no longer function reliably as designed.

Methods used to address these timing issues include:

- ✎✎ Serpentine traces to match clock trace lengths
- ✎✎ Use Fan-out Buffers with minimum output-output skew
- ✎✎ Use Zero Delay Buffers to advance/ delay clock edges or to compensate for various delays, including those of the fan-out buffers

### ***Signal Integrity degradation due to impedance mismatch***

As the edge rates of the clock increase, the harmonic frequency content extends into the GHz range. This means that any trace length longer than two centimeters should be treated as a transmission line. Clock signals can become distorted due to signal reflections caused by an impedance mismatch between the fan-out driver and the clock trace, as well as the clock trace and the receiving device, resulting in increased receive data errors, increased EMI, crosstalk, etc. Device-to-device output impedance variation, as well as impedance variation due to output voltage (the output impedance at 2.5V is higher than the output impedance at 3.3V), further complicates impedance matching issues.

Methods used to improve the signal integrity of a clock signal include:

- ✎✎ Use resistors in series with the fan-out drivers to match the trace impedance
- ✎✎ Use termination resistors from inputs to ground or across inputs
- ✎✎ Use fan-out buffers to drive individual clock signals to each receiver device

### Multiple signaling standards force increased hierarchy levels

The signaling standard of the clock is determined by the receiver chip or by the clock domain. For example, DDR memory requires SSTL2-Differential standard clock signals, but a clock generator circuit supporting the LVCMOS standard might generate the required master clock frequency. Increasing the number of levels in a clock net hierarchy due to standard translators often complicates the process of meeting the required timing specifications.

Methods used to interface different logic standards (e.g., LVDS, LVCMOS, SSTL, HSTL, etc.) include:

- ✎✎ Use specialized translators to match the signaling interface between the clock generators and receiver IC
- ✎✎ Terminate unused outputs depending on the design
- ✎✎ Use specialized zero delay buffers to synchronize edges of clocks with dissimilar signaling interfaces

### Other clock net design issues

- ✎✎ Reduction of Electro Magnetic Interference (EMI), crosstalk, etc.
  - Reduce clock slew rate by using capacitors to load outputs
- ✎✎ Clock jitter further reduces the timing margin
  - Use devices with minimal jitter (cycle-to-cycle, period, phase, etc.,) characteristics depending on application needs
  - Limit the number of cascaded PLLs

*Lattice ispClock5500 family of In-System Programmable Clock Generator devices addresses all the above challenges in a unique and convenient manner while providing superior performance, reduced board space, ease of design, and flexibility across different clocking network architectures.*

### **The ispClock5500 Family**

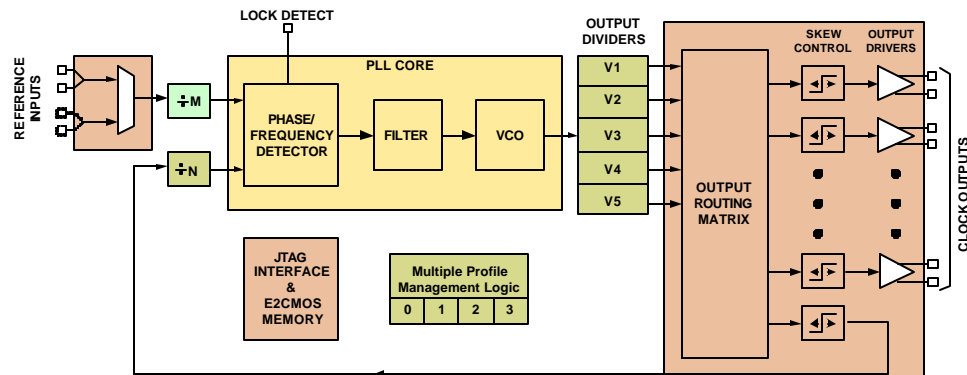
The first devices in the ispClock5500 family, the 10-output ispClock5510 and 20-output ispClock5520, combine a high-performance programmable clock generator together with a flexible, Universal Fan-out Buffer. The on-chip clock generator can provide up to 5 clock frequencies ranging from 10MHz to 320MHz using a high-performance PLL and clock multiply and divide facilities. The Universal Fan-out Buffer can drive up to 20 clock nets using either single-ended or differential signaling, with individual output control for improved signal and timing integrity. The new devices provide an unprecedented level of performance and flexibility in support of high-performance clock network designs on electronic circuit boards.

These devices greatly reduce clock net design effort by generating multiple clock frequencies and fanning out the resulting clocks across the circuit board, while also addressing signal integrity and timing issues on a per clock net basis.

## Architectural Details

The ispClock5500 Architecture can be divided into these sections:

- Programmable Clock I/O
- PLL Core
- Frequency Synthesis Counters
- JTAG Interface
- Profile Management



**Programmable Clock I/O** - The input section consists of two hardware selectable multiplexed clock inputs. The output section consists of up to 20 low-skew clock outputs. Both the reference clock input and the clock outputs can be individually programmed to interface to single ended logic (LVTTTL, LVCMOS, SSTL, HSTL) or differential logic (LVDS, LVPECL, Diff HSTL, Diff SSTL) types. Input and output termination resistance can be programmed between 40 to 70 ohms in 5-ohm steps. The output skew of each clock output can be individually set to one of 16 steps with resolution to 195ps. The skew step size is derived from the PLL frequency and so is very precise. The frequency synthesis unit is able to generate up to 5 clock frequencies. The non-blocking output switch matrix can switch any frequency to any output. The Input frequency range is from 10MHz to 320MHz and output frequency range is from 5MHz to 320 MHz.

**PLL Core** - The heart of the device is the high-performance PLL core consisting of a Phase Frequency Detector (PFD), Programmable on-chip filter, and VCO. The PLL core is able to lock to inputs ranging from 10 MHz to 320 MHz, while the output frequency range is between 320 to 640 MHz. Output jitter is <100ps.

**Frequency Synthesis Counters** - The device has seven 5-bit counters: M, N, and five V Counters. The M, N, and one V counter provide 5-bit resolution to set the operating frequency of the PLL. The output of the PLL then drives the remaining V-dividers, resulting in the synthesis of five independent frequencies related only by the PLL operating frequency.

**JTAG Programming and Boundary Scan Interface** - While the device can be fully programmed using the JTAG interface, it can also be used for testing circuit board interconnection using standard in-circuit testers.

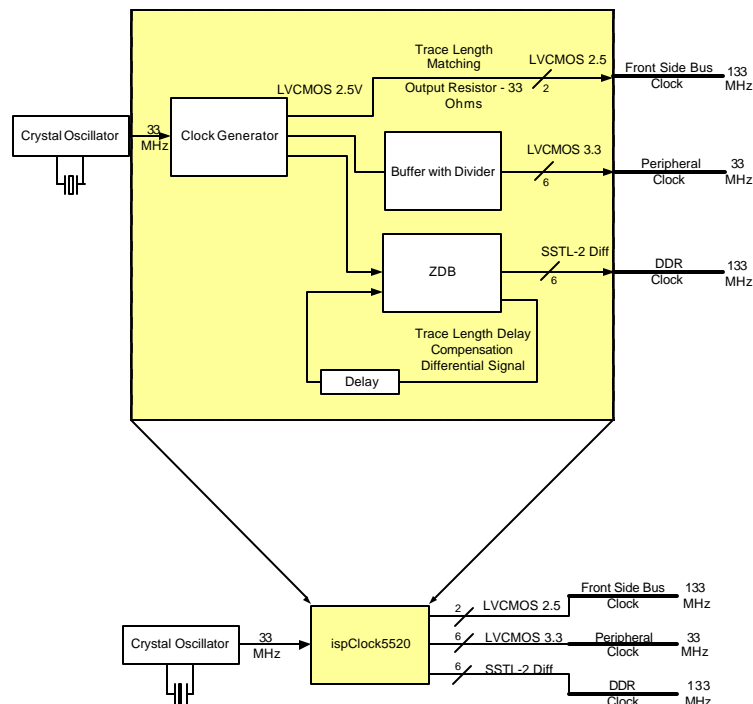
**Profile Management** -The device can store up to four independent configurations – (M, N, and V counters, Skew) -- enabling the selection of one of four independent clock frequencies or skew, etc. Profile management provides an ideal mechanism for implementing functions such as frequency switching for power management, or configuring the board operating frequency depending on the speed of the processor, etc.

ispClock5500 family:

Features	ispClock5510	ispClock5520
Input and Output Frequency Range	10-320 MHz	10-320 MHz
Programmable Input and Output Interface Types	LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL	LVTTL, LVCMOS, SSTL, HSTL, LVDS, LVPECL
Number of Outputs	10	20
Output-Output Skew (Max)	50ps	50ps
Maximum cycle-Cycle Jitter	70ps (Peak-Peak)	70ps (Peak-Peak)
Number of Frequencies Generated	5	5
Programmable Skew	195ps to 12 ns	195ps to 12 ns
Programmable Termination	40 ohm to 70 ohm	40 ohm to 70 ohm
Package	48-pin TQFP	100-pin TQFP
Ordering Part Number	ispPAC-CLK5510V-01T48C	ispPAC-CLK5520V-01T100C

## Application

In the following figure the top section illustrates a clock net hierarchy implementation using a traditional method. The bottom section is the same implementation using the ispClock5500.



ispClock5520 Replaces Traditional Discrete Devices

### Description of discrete clock net circuit (top section of the figure)

Starting from the left, a 33 MHz oscillator circuit is used as a source for the entire clock net. The clock generator chip multiplies the input clock by 4 and distributes the 133MHz clock using LVCMOS2.5V integrated fan-out buffer. The four outputs of 133 MHz are used as follows:

- 2 outputs are used for clocking processor front-side bus interface
- 1 output is used for generating 33 MHz using a 1:6 fan-out buffer with divider for clocking peripheral devices using LVCMOS3.3 interface
- 1 output is used for deriving six 133MHz SSTL-2D (Differential Clocks) for clocking DDR devices and the memory controller. This section required a Zero Delay Buffer to translate the input signal, and compensate for flight time.

The design also required termination resistors for signal integrity, and snaking clock patterns for matching trace lengths.

### ispClock5520-based circuit (bottom section of the figure)

Starting from the left, this circuit used the same 33MHz crystal oscillator. The PLL core and the V-dividers internally generate both 133 MHz and 33 MHz. The output switch matrix is configured to route these clock signals to the corresponding fan-out buffer. The Universal Fan-out buffer was configured as follows:

- 2 single ended outputs to drive the Processor Front-Side Bus with 133MHz using the LVCMOS2.5 interface and matched trace impedance using the programmable output impedance feature
- 6 single ended outputs to drive the peripheral bus with the 33MHz clock using the LVCMOS3.3 interface and matched trace impedance using the programmable impedance feature
- 6 differential outputs to drive the DDR memory and controllers with 133MHz using the SSTL-2D interface and set the output impedance to 50 ohm using the programmable output impedance feature

The programmable skew feature of the ispClock5520 greatly simplified the task of clock trace length matching by using 32 steps of 235ps for each skew setting. The trace impedance matching was resolved by using the programmable output impedance feature of the ispClock5520.

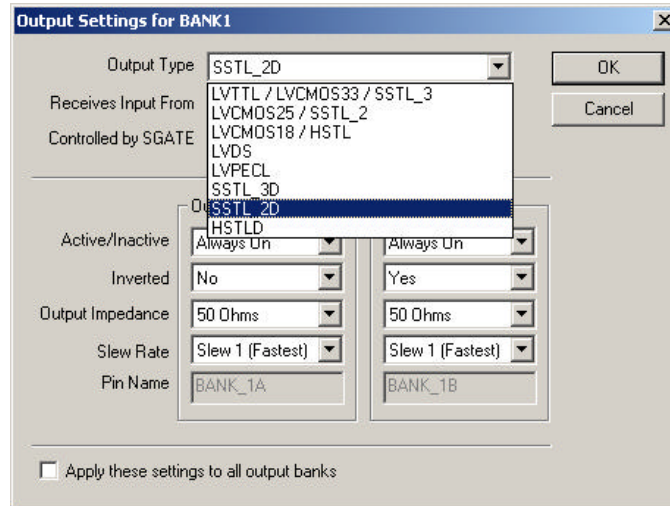
## **Software Support**

Implementing the design shown in the circuit diagram above in an ispClock5520 device using the PAC-Designer Version 3.0 software tool is completed in minutes using the steps described below.

### Clock I/O Interface Specification

The schematic interface of the PAC-Designer software enables the user to specify the I/O characteristics, M, N, and V dividers, Skew setting etc, through simple pull down menus.

The output interface characteristics can be defined using the pull down menu as shown. The designer should use the following menu to set the output type, output impedance, slew rate, and V-Divider to source the required frequency. Additionally, this menu can be used to select the output enable control and synchronous gating functions.

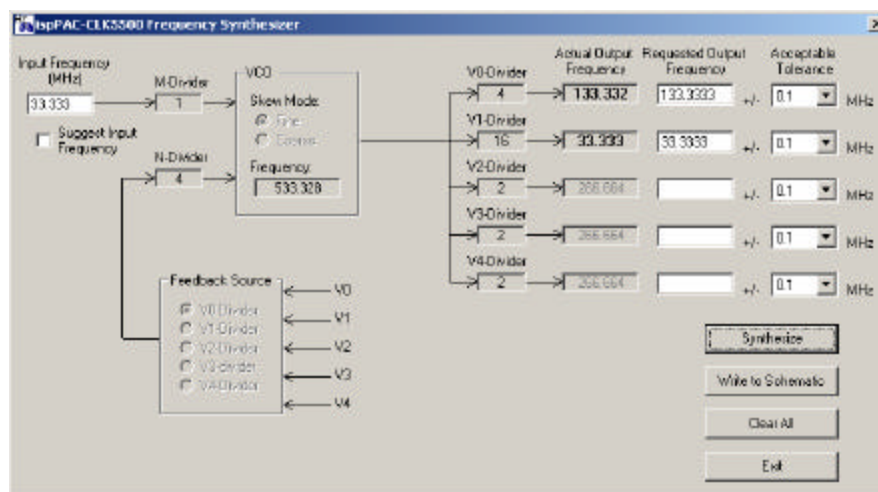


In this design, the outputs are configured as follows:

- Bank 0 to Bank 5 – 6 outputs, SSTL-2 differential, 133 MHz, 50 Ohm, Fast Slew rate
- Bank 6 – 2 outputs, LVCMOS2.5, 133 MHz, 50 Ohm, Fast Slew Rate
- Bank 7 to Bank 10 – 6 outputs, LVCMOS3.3, 33 MHz, 50 Ohm, Fast Slew Rate

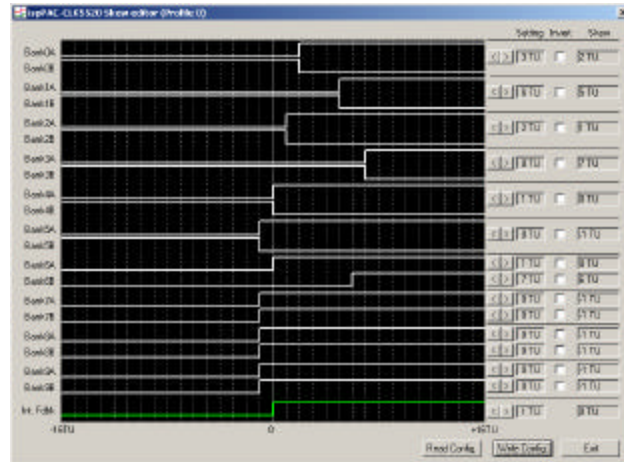
Calculating the M, N and V divider values from the input and output clock frequencies

PAC-Designer supports a number of design utilities that enable the designer to select the configuration from the system specifications. In this case, the frequency synthesizer design utility is used to calculate the M, N and V divider configuration using the input and output frequencies.



As can be seen in generating 133MHz and 33MHz from the input 33MHz, the M divider should be set to 1, the N divider to 4, V-Divider generating 133 MHz to 4 and the V-Divider generating 33 MHz to 16. The PLL VCO is configured to operate at 533MHz. This results in minimum skew step size of  $(1/8 * 533 * 10E06) = 235ps$ .

Setting the Output Skew to compensate for Differences in Trace Length



The Skew Editor screen above is used to select the output clock skew. The skew step size, shown in this screen as TU (Time Unit), is 235 ps. To modify the skew of a clock signal, just click and drag the waveform.

Verify the design using the summary report

Output	Pin Name	Output Type	Receives From	Controlled by STATE	Active/Inactive	Inverted	Impedance	Skew Rate	Skew
BANK0_A	BANK0_A	SSTL_2D	Div 0	No	Always On	No	45	Slew 1	3TU
BANK0_B	BANK0_B					Yes	45	Slew 1	3TU
BANK1_A	BANK1_A	SSTL_2D	Div 0	No	Always On	No	50	Slew 1	6TU
BANK1_B	BANK1_B					Yes	50	Slew 1	6TU
BANK2_A	BANK2_A	SSTL_2D	Div 0	No	Always On	No	50	Slew 1	2TU
BANK2_B	BANK2_B					Yes	50	Slew 1	2TU
BANK3_A	BANK3_A	SSTL_2D	Div 0	No	Always On	No	50	Slew 1	8TU
BANK3_B	BANK3_B					Yes	50	Slew 1	8TU
BANK4_A	BANK4_A	SSTL_2D	Div 0	No	Always On	No	50	Slew 1	1TU
BANK4_B	BANK4_B					Yes	50	Slew 1	1TU
BANK5_A	BANK5_A	SSTL_2D	Div 0	No	Always On	No	50	Slew 1	0
BANK5_B	BANK5_B					Yes	50	Slew 1	0
BANK6_A	BANK6_A	LVCMOS25 / SSTL_2	Div 0	No	Always On	No	50	Slew 1	1TU
BANK6_B	BANK6_B					No	50	Slew 1	7TU
BANK7_A	BANK7_A	LVTTL / LVCMOS33 / SSTL_3	Div 1	No	Always On	No	50	Slew 1	0
BANK7_B	BANK7_B					No	50	Slew 1	0
BANK8_A	BANK8_A	LVTTL / LVCMOS33 / SSTL_3	Div 1	No	Always On	No	50	Slew 1	0
BANK8_B	BANK8_B					No	50	Slew 1	0
BANK9_A	BANK9_A	LVTTL / LVCMOS33 / SSTL_3	Div 1	No	Always On	No	50	Slew 1	0
BANK9_B	BANK9_B					No	50	Slew 1	0

The output summary utility can be used to document all configurations on a single page for documentation and verification purposes.

## ***The ispClock5500 Redefines Clock Net Management***

The ispClock5500 devices provide unprecedented convenience in clock network design by integrating a high performance PLL core with a universal fan-out buffer.

### ***Easily compensate for circuit board trace length differences and device delays***

The programmable skew feature simplifies circuit board layout by reducing the need for snaking traces, and also helps in increasing timing margins, reducing design time.

### ***Improve the signal integrity by matching the circuit board trace impedance***

The ability to match the trace impedance through a programmable output impedance feature, coupled with increased output Vcc and Ground pins, improves clock signal integrity. Additionally, since the output impedance is trimmed on a per device basis, the device to device variation of output impedance is minimized, resulting in increased manufacturing yield.

### ***Reduce number of levels in clock net hierarchy – flattening the hierarchy***

The universal fan-out buffer can be programmed to drive multiple signaling standards, reducing the need for separate (sometimes partially used) signal translators and so reducing the number of levels in the clock net hierarchy and reducing the effort in meeting the overall circuit board timing requirements.

### ***Improved performance***

Low jitter, well-matched output-output skew provide additional timing margin.

### ***Reduced board space***

The ispClock5500 integration provides complete clock network implementation on one chip, saving circuit board area. The programmable skew management feature reduces the circuit board area used for compensating for differential trace lengths through serpentine trace layout. The on-chip programmable output impedance compensates for the increased circuit board area for the use of output impedance matching resistors.

### ***Reduces manufacturing cost***

The ispClock5500 devices support JTAG-based programming and boundary scan test on all I/O pins, reducing manufacturing costs due to programming and in-circuit testing.

### ***Other advantages***

Clock profile management supports easy implementation of power management through frequency scaling, as well as quality control through clock margining.

Because all the key features of this device are programmable, designers can standardize on the ispClock5500 for all their system clocking needs, resulting in reduced cost of ownership.

	<b>Design Approach With</b>		
<b>Clock Net Application</b>	<b>Lattice ispClock5500</b>	<b>Traditional Clock Devices</b>	<b>Other Programmable Skew Devices</b>
<i>Clock Edge Alignment:</i> Compensate for differential trace length or other chip delays	Programmable Individual Output Skew Control with <b>Fine</b> Skew Adjustment	Serpentine Trace Pattern, Delay Lines	Programmable Individual Output Skew Control with <b>Coarse</b> Skew Adjustment
<i>Signal Integrity:</i> Matching Trace Impedance with Output Impedance	Individual Programmable Output Impedance	Manually Select External Resistors	Manually Select External Resistors
<i>Application Specific Clock Signaling Interface</i>	Program the Universal Fan-out Buffer to Interface to LVCMOS, LVTTTL, SSTL, HSTL, LVDS, LVPECL	Translator ICs for Specific Interface/ Use Zero-delay Buffers to Compensate for Additional Time Delay	Translator ICs for Specific Interface/ Use Zero-delay Buffers to Compensate for Additional Time Delay
<i>Generate Multiple Clock Frequencies</i>	Up to 5 Programmable Output Frequencies	Multiple Clock Generators or Synthesizer Devices	Limited Frequency Options
<i>Reduce EMI and Crosstalk</i>	Program Individual Output Slew Rate	Use External Capacitors to Slow Clock Edges	Use External Capacitors to Slow Clock Edges
<i>Power Management:</i> Switching Clock Frequencies	Use Profile to Switch Between Independent Sets of Frequencies	Use Multiple Generators & Synthesizers and Switch the Clocks with Separate Fan-out Buffers	Use Multiple Generators & Synthesizers and Switch the Clocks with Separate Fan-out Buffers