

Introduction

Lattice Semiconductor's Programmable Logic Devices (PLDs) are manufactured using high-performance E²CMOS[®] processes. CMOS processing provides maximum AC performance with minimal power consumption. A potentially destructive phenomenon common to all CMOS technologies is known as latch-up.

This application note defines latch-up, how it manifests itself, and techniques that can be used to control it.

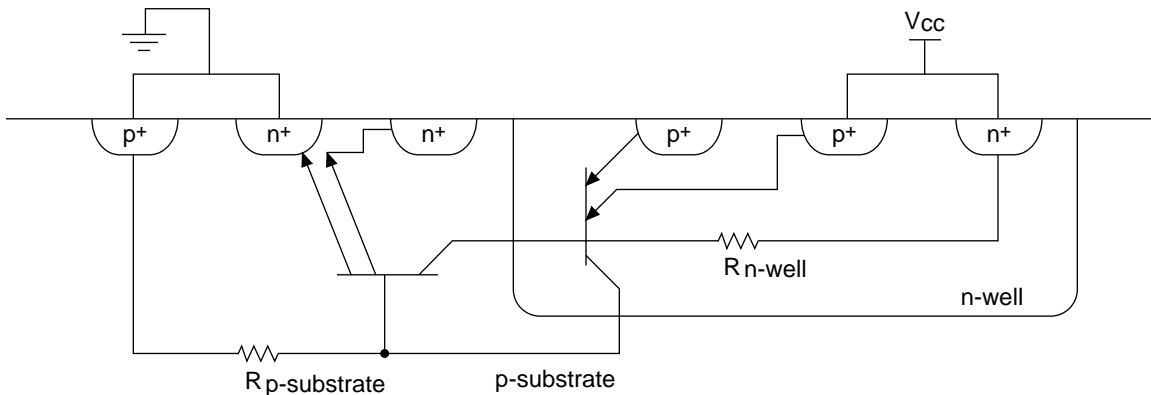
Background

Latch-up occurs as a result of parasitic bipolar transistors between the n-channel and p-channel devices. These transistors form a parasitic SCR (Silicon Controlled Rectifier), which turns ON when triggered, conducting large amounts of current. Once started, the current flow is usually impossible to interrupt without removing all power from the device. The amount of current drawn can be so high that it can either overload a power supply or, if the power supply can supply large amounts of current, destroy the device.

Latch-up is normally triggered when an input/output pin or supply voltage delta (referenced to ground) is significantly above the maximum pin or supply voltage specifications for a device, with enough current drawn to cause the parasitic SCR devices to turn on. This condition may be caused by power supply overshoot and undershoot, board noise and other behavior commonly found in a hot-socketing environment (i.e., plugging a part into a powered board or inserting a board into a powered system).

For true CMOS outputs, the SCR is an intrinsic part of the CMOS structure and cannot be eliminated. The SCR must be made as difficult as possible to turn ON.

Figure 1. Cross Section of Parasitic Devices



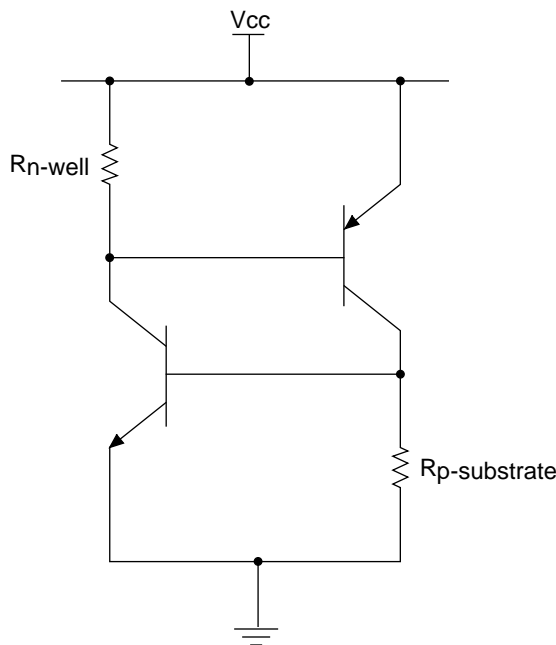
Manufacturing Steps for Reducing Latch-up

Through the use of advanced software simulations and testing procedures, Lattice is able to apply techniques that have been proven to reduce a device's susceptibility to latch-up while providing a cost-effective solution for customers. Also, through the use of advanced layout techniques, Lattice further lowers the risk of latch-up.

Customer Steps for Reducing Latch-up

Although the potential for latch-up is inherent in all CMOS devices, there are several steps a board/system designer can take to reduce the level of latch-up susceptibility in a system. Below are suggested areas that should be considered to reduce a board's exposure to latch-up

Figure 2. Equivalent Schematic for Device Parasites



Power Supply Noise Control

Bulk capacitors can be used near a board power supply to reduce potentially damaging voltage spikes. Also, several 0.01 μ F - 1.0 μ F capacitors should be placed next to each semiconductor device to provide power supply decoupling. Large CPLD devices with multiple V_{CC} and GND connections should have at least one capacitor on each quadrant of the device. In addition, all V_{CC} and GND connections should be connected.

Power Supply Control Output Control

The behavior of a power supply can greatly affect a board's overall latch-up susceptibility. One should take care to analyze the power-up and transient response as it relates to the operation of a system. For example, in a hot insertion environment, the insertions of a board into a backplane make cause a power supply to swing beyond the normal output voltage or current ratings inducing latch-up on a board. In this case, the supply transient response was not adequate to maintain the supply ratings under the load of the board upon insertion.

Another consideration when selecting a power supply is the power-up behavior of a supply in the entire system environment. A supply may require a "settling period" during which the outputs may not be guaranteed to remain in the specified operating range. For this, a rise time controlled supply would prove a better choice.

Power Sequencing

In hot insertion environments, it is common to find that an entire board does not become active at the same time. Commonly, a device's inputs will be driven before the device is fully powered. In some cases, powering the inputs of a device before the device is fully powered can cause it to power-up in a latch-up state.

There is one very easy solution that can be used to reduce power sequencing issues due to hot insertion. As mentioned, latch-up may occur when inputs of a device are driven to active levels before a device is powered. By extending the power supply pins of a board header, the board supply is able to power-up the devices before the backplane signals are able to drive the inputs of the board devices. This can prove to be a very cost-effective and proactive solution to a potentially costly board repair or replacement.

Board Layout Considerations

In addition to the power supply issues mentioned above, it is important to consider how power from the system power supply is distributed over the entire board. In an ideal environment, all devices would have “perfect” power applied at all times in the operation of a system where “perfect” power is the exact voltage and current needed for the device to operate at peak performance.

Unfortunately, “perfect” power distribution does not generally exist. Boards traces introduce undesired resistance, capacitance and inductance which can cause system power to become noisy or unclear. To reduce these characteristics, proper ground and power planes should be used in conjunction with the individual device decoupling techniques mentioned above. Although not a guarantee, proper board layout techniques can lower a systems susceptibility to latch-up.

Using Transient Suppression

Even with the steps mentioned in this application note, it may become impossible to adequately reduce a board's exposure to voltage and current spikes. In this case, it is possible to momentarily clamp the spikes to the power supply protecting the devices on the board. For this, Transient Voltage Suppressors (TVS) can be used. These devices are similar to zener diodes, but offer a much faster turn-on time. There are several types of transient suppressor diodes available. Many of these have been designed for datacom/telecom type of applications where hot insertion is prevalent. This wide device selection allows a board designer to select a device that will turn on at a specific voltage, clamping a voltage spike to the supply. The device turn-on voltage should be above the board (or design) V_{CC} , but below the level of potentially damaging noise.

Summary

In summary, although all CMOS devices are capable of latch-up, devices today include advanced processing and design techniques that can control the occurrences of latch-up. Most importantly, there are board design and layout techniques that customers can use to further lower a system's susceptibility to latch-up and its damaging affects. It often proves cost-effective to design a board from the beginning that can handle possible latch-up causing events.