

Features

■ High Performance

- f_{MAX} = 260MHz maximum operating frequency
- t_{PD} = 4.4ns propagation delay
- Up to four global clock pins with programmable clock polarity control
- Up to 80 PTs per output

■ Ease of Design

- Flexible CPLD macrocells with individual clock, reset, preset and clock enable controls
- Up to four global OE controls
- Individual local OE control per I/O pin
- Excellent First-Time-Fit™ and refit
- Wide input gating (36 input logic blocks) for fast counters, state machines and address decoders

■ Ultra Low Power

- Standby current as low as 10µA typical
- 1.8V core; low dynamic power
- Operational down to 1.6V V_{CC}
- Superior solution for power sensitive consumer applications
- **Per pin pull-up, pull-down or bus keeper control***
- **Power Guard with multiple enable signals***

■ Broad Device Offering

- 32 to 256 macrocells
- Multiple temperature range support
 - Commercial: 0 to 90°C junction (T_j)
 - Industrial: -40 to 105°C junction (T_j)
- Space-saving packages

■ Easy System Integration

- Operation with 3.3V, 2.5V, 1.8V or 1.5V LVCMOS I/O
- 5V tolerant I/O for LVCMOS 3.3, LVTTTL, and PCI interfaces
- Hot-socketing support
- Open-drain output option
- Programmable output slew rate
- 3.3V PCI compatible
- I/O pins with fast setup path
- **Input hysteresis***
- 1.8V core power supply
- IEEE 1149.1 boundary scan testable
- IEEE 1532 ISC compliant
- 1.8V In-System Programmable (ISP™) using Boundary Scan Test Access Port (TAP)
- Pb-free package options (only)
- **On-chip user oscillator and timer***

*New enhanced features over original ispMACH 4000Z

Table 1. ispMACH 400ZE Family Selection Guide

| | ispMACH 4032ZE | ispMACH 4064ZE | ispMACH 4128ZE | ispMACH 4256ZE |
|--|----------------|----------------|----------------|----------------|
| Macrocells | 32 | 64 | 128 | 256 |
| t_{PD} (ns) | 4.4 | 4.7 | 5.8 | 5.8 |
| t_S (ns) | 2.2 | 2.5 | 2.9 | 2.9 |
| t_{CO} (ns) | 3.0 | 3.2 | 3.8 | 3.8 |
| f_{MAX} (MHz) | 260 | 241 | 200 | 200 |
| Supply Voltages (V) | 1.8V | 1.8V | 1.8V | 1.8V |
| Packages¹ (I/O + Dedicated Inputs) | | | | |
| 48-Pin TQFP (7 x 7mm) | 32+4 | 32+4 | | |
| 64-Ball csBGA (5 x 5mm) | 32+4 | 48+4 | | |
| 100-Pin TQFP (14 x 14mm) | | 64+10 | 64+10 | 64+10 |
| 144-Pin TQFP (20 x 20mm) | | | 96+4 | 96+14 |
| 144-Ball csBGA (7 x 7mm) | | 64+10 | 96+4 | 108+4 |

1. Pb-free only.

Introduction

The high performance ispMACH 4000ZE family from Lattice offers an ultra low power CPLD solution. The new family is based on Lattice’s industry-leading ispMACH 4000 architecture. Retaining the best of the previous generation, the ispMACH 4000ZE architecture focuses on significant innovations to combine high performance with low power in a flexible CPLD family. For example, the family’s new Power Guard feature minimizes dynamic power consumption by preventing internal logic toggling due to unnecessary I/O pin activity.

The ispMACH 4000ZE combines high speed and low power with the flexibility needed for ease of design. With its robust Global Routing Pool and Output Routing Pool, this family delivers excellent First-Time-Fit, timing predictability, routing, pin-out retention and density migration.

The ispMACH 4000ZE family offers densities ranging from 32 to 256 macrocells. There are multiple density-I/O combinations in Thin Quad Flat Pack (TQFP) and Chip Scale BGA (csBGA) packages ranging from 32 to 176 pins/balls. Table 1 shows the macrocell, package and I/O options, along with other key parameters.

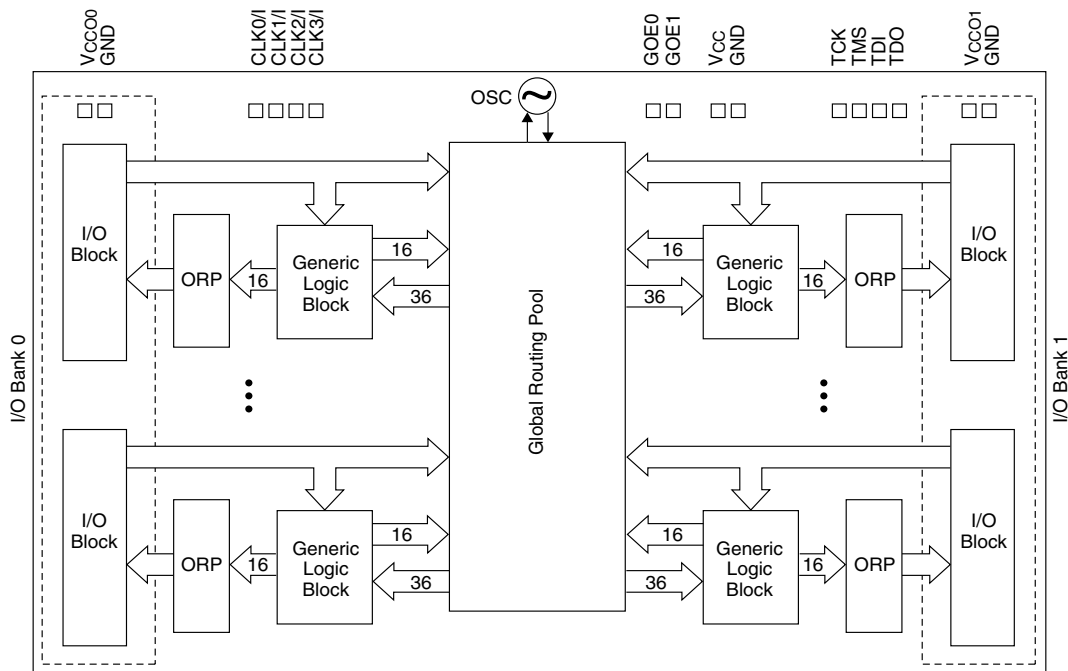
A user programmable internal oscillator and a timer are included in the device for tasks like LED control, keyboard scanner and similar housekeeping type state machines. This feature can be optionally disabled to save power.

The ispMACH 4000ZE family has enhanced system integration capabilities. It supports a 1.8V supply voltage and 3.3V, 2.5V, 1.8V and 1.5V interface voltages. Additionally, inputs can be safely driven up to 5.5V when an I/O bank is configured for 3.3V operation, making this family 5V tolerant. The ispMACH 4000ZE also offers enhanced I/O features such as slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs and hot socketing. Pull-up, pull-down and bus-keeper features are controllable on a “per-pin” basis. The ispMACH 4000ZE family members are 1.8V in-system programmable through the IEEE Standard 1532 interface. IEEE Standard 1149.1 boundary scan testing capability also allows product testing on automated test equipment. The 1532 interface signals TCK, TMS, TDI and TDO are referenced to V_{CC} (logic core).

Overview

The ispMACH 4000ZE devices consist of multiple 36-input, 16-macrocell Generic Logic Blocks (GLBs) interconnected by a Global Routing Pool (GRP). Output Routing Pools (ORPs) connect the GLBs to the I/O Blocks (IOBs), which contain multiple I/O cells. This architecture is shown in Figure 1.

Figure 1. Functional Block Diagram



The I/Os in the ispMACH 4000ZE are split into two banks. Each bank has a separate I/O power supply. Inputs can support a variety of standards independent of the chip or bank power supply. Outputs support the standards compatible with the power supply provided to the bank. Support for a variety of standards helps designers implement designs in mixed voltage environments. In addition, 5V tolerant inputs are specified within an I/O bank that is connected to a V_{CCO} of 3.0V to 3.6V for LVCMOS 3.3, LVTTTL and PCI interfaces.

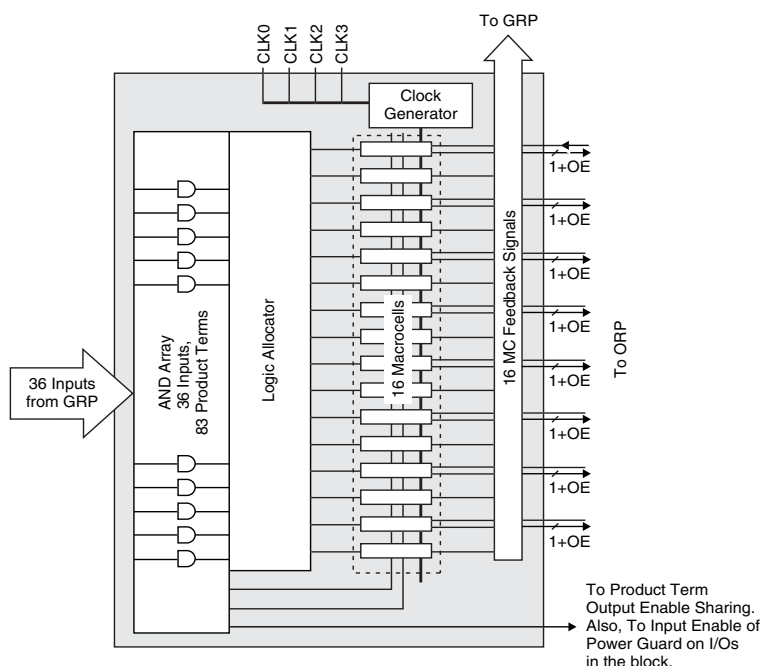
Architecture

There are a total of two GLBs in the ispMACH 4032ZE, increasing to 16 GLBs in the ispMACH 4256ZE. Each GLB has 36 inputs. All GLB inputs come from the GRP and all outputs from the GLB are brought back into the GRP to be connected to the inputs of any other GLB on the device. Even if feedback signals return to the same GLB, they still must go through the GRP. This mechanism ensures that GLBs communicate with each other with consistent and predictable delays. The outputs from the GLB are also sent to the ORP. The ORP then sends them to the associated I/O cells in the I/O block.

Generic Logic Block

The ispMACH 4000ZE GLB consists of a programmable AND array, logic allocator, 16 macrocells and a GLB clock generator. Macrocells are decoupled from the product terms through the logic allocator and the I/O pins are decoupled from macrocells through the ORP. Figure 2 illustrates the GLB.

Figure 2. Generic Logic Block

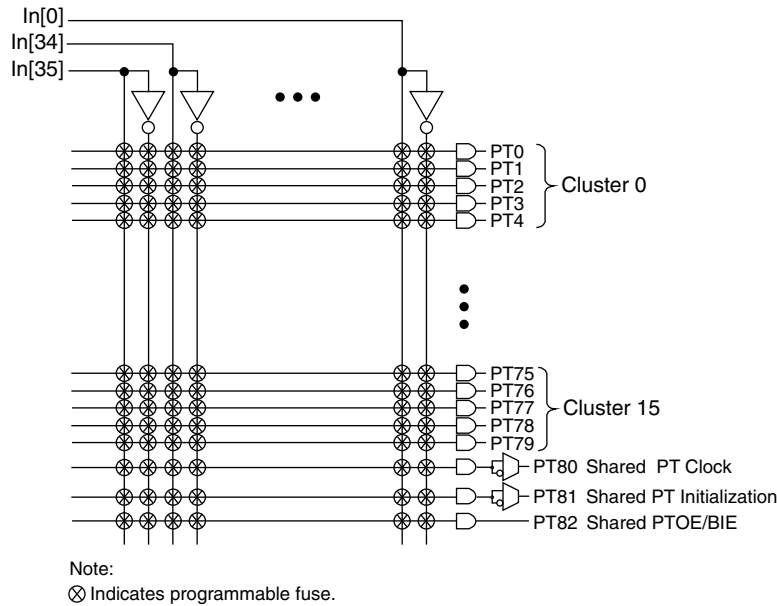


AND Array

The programmable AND Array consists of 36 inputs and 83 output product terms. The 36 inputs from the GRP are used to form 72 lines in the AND Array (true and complement of the inputs). Each line in the array can be connected to any of the 83 output product terms via a wired-AND. Each of the 80 logic product terms feed the logic allocator with the remaining three control product terms feeding the Shared PT Clock, Shared PT Initialization and Shared PT OE. The Shared PT Clock and Shared PT Initialization signals can optionally be inverted before being fed to the macrocells.

Every set of five product terms from the 80 logic product terms forms a product term cluster starting with PT0. There is one product term cluster for every macrocell in the GLB. Figure 3 is a graphical representation of the AND Array.

Figure 3. AND Array



Enhanced Logic Allocator

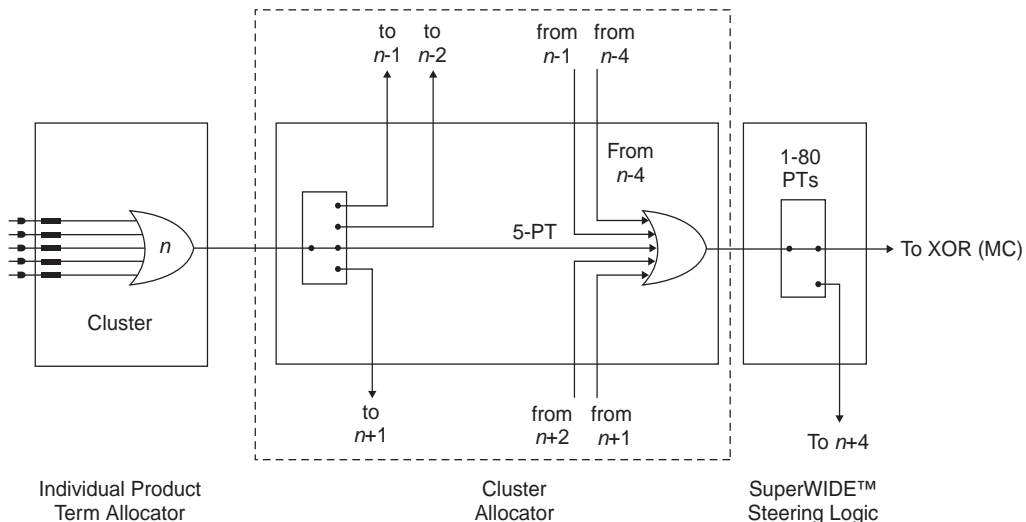
Within the logic allocator, product terms are allocated to macrocells in product term clusters. Each product term cluster is associated with a macrocell. The cluster size for the ispMACH 4000ZE family is 4+1 (total 5) product terms. The software automatically considers the availability and distribution of product term clusters as it fits the functions within a GLB. The logic allocator is designed to provide two speed paths: 20-PT Speed Locking path and an up to 80-PT path. The availability of these two paths lets designers trade timing variability for increased performance.

The enhanced Logic Allocator of the ispMACH 4000ZE family consists of the following blocks:

- Product Term Allocator
- Cluster Allocator
- Wide Steering Logic

Figure 4 shows a macrocell slice of the Logic Allocator. There are 16 such slices in the GLB.

Figure 4. Macrocell Slice



Product Term Allocator

The product term allocator assigns product terms from a cluster to either logic or control applications as required by the design being implemented. Product terms that are used as logic are steered into a 5-input OR gate associated with the cluster. Product terms that used for control are steered either to the macrocell or I/O cell associated with the cluster. Table 2 shows the available functions for each of the five product terms in the cluster.

Table 2. Individual PT Steering

| Product Term | Logic | Control |
|--------------|----------|---|
| PT n | Logic PT | Single PT for XOR/OR |
| PT $n+1$ | Logic PT | Individual Clock (PT Clock) |
| PT $n+2$ | Logic PT | Individual Initialization or Individual Clock Enable (PT Initialization/CE) |
| PT $n+3$ | Logic PT | Individual Initialization (PT Initialization) |
| PT $n+4$ | Logic PT | Individual OE (PTOE) |

Cluster Allocator

The cluster allocator allows clusters to be steered to neighboring macrocells, thus allowing the creation of functions with more product terms. Table 3 shows which clusters can be steered to which macrocells. Used in this manner, the cluster allocator can be used to form functions of up to 20 product terms. Additionally, the cluster allocator accepts inputs from the wide steering logic. Using these inputs, functions up to 80 product terms can be created.

Table 3. Available Clusters for Each Macrocell

| Macrocell | Available Clusters | | | |
|-----------|--------------------|-----|-----|-----|
| M0 | — | C0 | C1 | C2 |
| M1 | C0 | C1 | C2 | C3 |
| M2 | C1 | C2 | C3 | C4 |
| M3 | C2 | C3 | C4 | C5 |
| M4 | C3 | C4 | C5 | C6 |
| M5 | C4 | C5 | C6 | C7 |
| M6 | C5 | C6 | C7 | C8 |
| M7 | C6 | C7 | C8 | C9 |
| M8 | C7 | C8 | C9 | C10 |
| M9 | C8 | C9 | C10 | C11 |
| M10 | C9 | C10 | C11 | C12 |
| M11 | C10 | C11 | C12 | C13 |
| M12 | C11 | C12 | C13 | C14 |
| M13 | C12 | C13 | C14 | C15 |
| M14 | C13 | C14 | C15 | — |
| M15 | C14 | C15 | — | — |

Wide Steering Logic

The wide steering logic allows the output of the cluster allocator n to be connected to the input of the cluster allocator $n+4$. Thus, cluster chains can be formed with up to 80 product terms, supporting wide product term functions and allowing performance to be increased through a single GLB implementation. Table 4 shows the product term chains.

Table 4. Product Term Expansion Capability

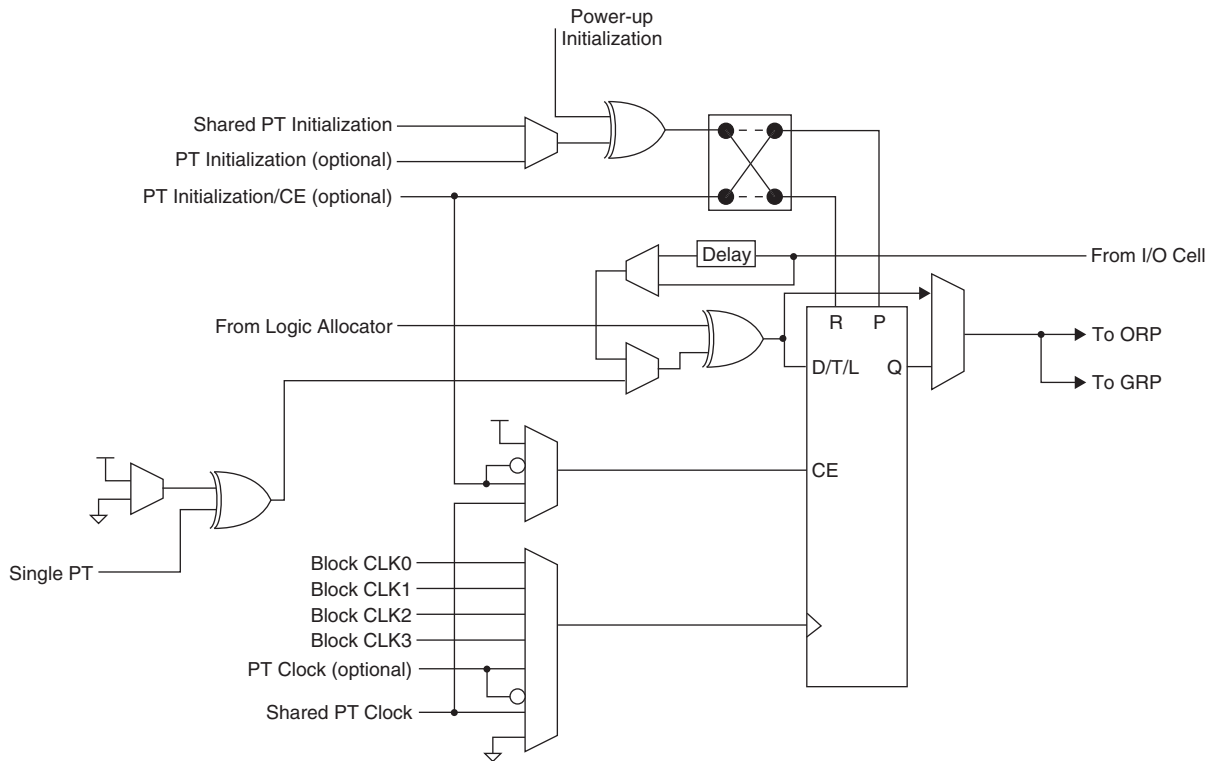
| Expansion Chains | Macrocells Associated with Expansion Chain (with Wrap Around) | Max PT/Macrocell |
|------------------|---|------------------|
| Chain-0 | M0 → M4 → M8 → M12 → M0 | 75 |
| Chain-1 | M1 → M5 → M9 → M13 → M1 | 80 |
| Chain-2 | M2 → M6 → M10 → M14 → M2 | 75 |
| Chain-3 | M3 → M7 → M11 → M15 → M3 | 70 |

Every time the super cluster allocator is used, there is an incremental delay of t_{EXP} . When the super cluster allocator is used, all destinations other than the one being steered to, are given the value of ground (i.e., if the super cluster is steered to M (n+4), then M (n) is ground).

Macrocell

The 16 macrocells in the GLB are driven by the 16 outputs from the logic allocator. Each macrocell contains a programmable XOR gate, a programmable register/latch, along with routing for the logic and control functions. Figure 5 shows a graphical representation of the macrocell. The macrocells feed the ORP and GRP. A direct input from the I/O cell allows designers to use the macrocell to construct high-speed input registers. A programmable delay in this path allows designers to choose between the fastest possible set-up time and zero hold time.

Figure 5. Macrocell



Enhanced Clock Multiplexer

The clock input to the flip-flop can select any of the four block clocks along with the shared PT clock, and true and complement forms of the optional individual term clock. An 8:1 multiplexer structure is used to select the clock. The eight sources for the clock multiplexer are as follows:

- Block CLK0
- Block CLK1

- Block CLK2
- Block CLK3
- PT Clock
- PT Clock Inverted
- Shared PT Clock
- Ground

Clock Enable Multiplexer

Each macrocell has a 4:1 clock enable multiplexer. This allows the clock enable signal to be selected from the following four sources:

- PT Initialization/CE
- PT Initialization/CE Inverted
- Shared PT Clock
- Logic High

Initialization Control

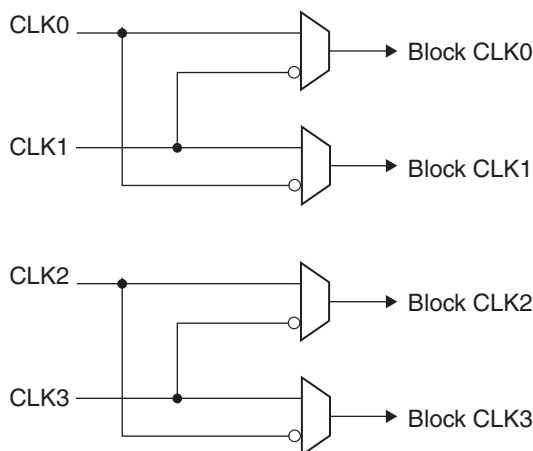
The ispMACH 4000ZE family architecture accommodates both block-level and macrocell-level set and reset capability. There is one block-level initialization term that is distributed to all macrocell registers in a GLB. At the macrocell level, two product terms can be “stolen” from the cluster associated with a macrocell to be used for set/reset functionality. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility.

Note that the reset/preset swapping selection feature affects power-up reset as well. All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the block-level initialization, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the block-level initialization or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

GLB Clock Generator

Each ispMACH 4000ZE device has up to four clock pins that are also routed to the GRP to be used as inputs. These pins drive a clock generator in each GLB, as shown in Figure 6. The clock generator provides four clock signals that can be used anywhere in the GLB. These four GLB clock signals can consist of a number of combinations of the true and complement edges of the global clock signals.

Figure 6. GLB Clock Generator



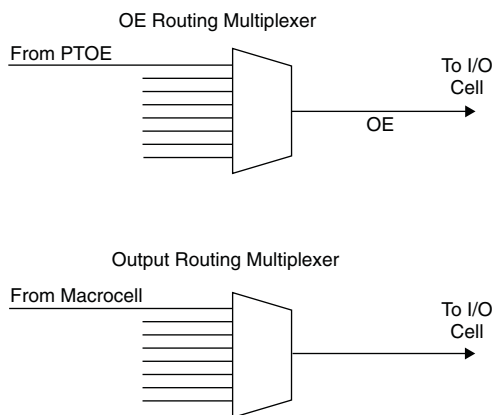
Output Routing Pool (ORP)

The Output Routing Pool allows macrocell outputs to be connected to any of several I/O cells within an I/O block. This provides greater flexibility in determining the pinout and allows design changes to occur without affecting the pinout. The output routing pool also provides a parallel capability for routing macrocell-level OE product terms. This allows the OE product term to follow the macrocell output as it is switched between I/O cells. The enhanced ORP of the ispMACH 400ZE family consists of the following elements:

- Output Routing Multiplexers
- OE Routing Multiplexers

Figure 7 shows the structure of the ORP from the I/O cell perspective. This is referred to as an ORP slice. Each ORP has as many ORP slices as there are I/O cells in the corresponding I/O block.

Figure 7. ORP Slice



Output Routing Multiplexers

The details of connections between the macrocells and the I/O cells vary across devices and within a device dependent on the maximum number of I/Os available. Tables 5-7 provide the connection details.

Table 5. GLB/MC/ORP Combinations for ispMACH 4256ZE

| GLB/MC | ORP Mux Input Macrocells |
|--------------|--------------------------------------|
| [GLB] [MC 0] | M0, M1, M2, M3, M4, M5, M6, M7 |
| [GLB] [MC 1] | M2, M3, M4, M5, M6, M7, M8, M9 |
| [GLB] [MC 2] | M4, M5, M6, M7, M8, M9, M10, M11 |
| [GLB] [MC 3] | M6, M7, M8, M9, M10, M11, M12, M13 |
| [GLB] [MC 4] | M8, M9, M10, M11, M12, M13, M14, M15 |
| [GLB] [MC 5] | M10, M11, M12, M13, M14, M15, M0, M1 |
| [GLB] [MC 6] | M12, M13, M14, M15, M0, M1, M2, M3 |
| [GLB] [MC 7] | M14, M15, M0, M1, M2, M3, M4, M5 |

Table 6. GLB/MC/ORP Combinations for ispMACH 4128ZE

| GLB/MC | ORP Mux Input Macrocells |
|---------------|--------------------------------------|
| [GLB] [MC 0] | M0, M1, M2, M3, M4, M5, M6, M7 |
| [GLB] [MC 1] | M1, M2, M3, M4, M5, M6, M7, M8 |
| [GLB] [MC 2] | M2, M3, M4, M5, M6, M7, M8, M9 |
| [GLB] [MC 3] | M4, M5, M6, M7, M8, M9, M10, M11 |
| [GLB] [MC 4] | M5, M6, M7, M8, M9, M10, M11, M12 |
| [GLB] [MC 5] | M6, M7, M8, M9, M10, M11, M12, M13 |
| [GLB] [MC 6] | M8, M9, M10, M11, M12, M13, M14, M15 |
| [GLB] [MC 7] | M9, M10, M11, M12, M13, M14, M15, M0 |
| [GLB] [MC 8] | M10, M11, M12, M13, M14, M15, M0, M1 |
| [GLB] [MC 9] | M12, M13, M14, M15, M0, M1, M2, M3 |
| [GLB] [MC 10] | M13, M14, M15, M0, M1, M2, M3, M4 |
| [GLB] [MC 11] | M14, M15, M0, M1, M2, M3, M4, M5 |

Table 7. GLB/MC/ORP Combinations for ispMACH 4032ZE and 4064ZE

| GLB/MC | ORP Mux Input Macrocells |
|---------------|--------------------------------------|
| [GLB] [MC 0] | M0, M1, M2, M3, M4, M5, M6, M7 |
| [GLB] [MC 1] | M1, M2, M3, M4, M5, M6, M7, M8 |
| [GLB] [MC 2] | M2, M3, M4, M5, M6, M7, M8, M9 |
| [GLB] [MC 3] | M3, M4, M5, M6, M7, M8, M9, M10 |
| [GLB] [MC 4] | M4, M5, M6, M7, M8, M9, M10, M11 |
| [GLB] [MC 5] | M5, M6, M7, M8, M9, M10, M11, M12 |
| [GLB] [MC 6] | M6, M7, M8, M9, M10, M11, M12, M13 |
| [GLB] [MC 7] | M7, M8, M9, M10, M11, M12, M13, M14 |
| [GLB] [MC 8] | M8, M9, M10, M11, M12, M13, M14, M15 |
| [GLB] [MC 9] | M9, M10, M11, M12, M13, M14, M15, M0 |
| [GLB] [MC 10] | M10, M11, M12, M13, M14, M15, M0, M1 |
| [GLB] [MC 11] | M11, M12, M13, M14, M15, M0, M1, M2 |
| [GLB] [MC 12] | M12, M13, M14, M15, M0, M1, M2, M3 |
| [GLB] [MC 13] | M13, M14, M15, M0, M1, M2, M3, M4 |
| [GLB] [MC 14] | M14, M15, M0, M1, M2, M3, M4, M5 |
| [GLB] [MC 15] | M15, M0, M1, M2, M3, M4, M5, M6 |

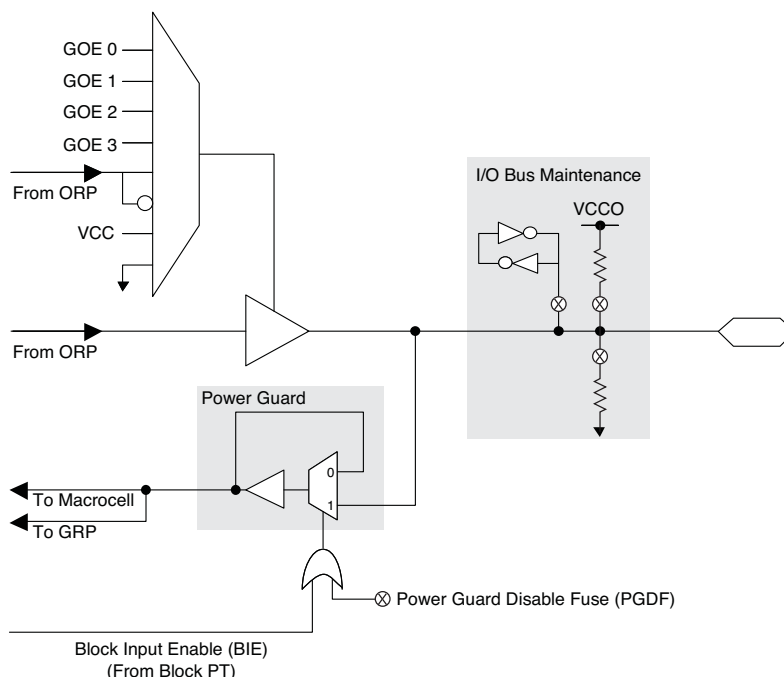
Output Enable Routing Multiplexers

The OE Routing Pool provides the corresponding local output enable (OE) product term to the I/O cell.

I/O Cell

The I/O cell contains the following programmable elements: output buffer, input buffer, OE multiplexer, Power Guard and bus maintenance circuitry. Figure 8 details the I/O cell.

Figure 8. I/O Cell



Each output supports a variety of output standards dependent on the V_{CCO} supplied to its I/O bank. Outputs can also be configured for open drain operation. Each input can be programmed to support a variety of standards, independent of the V_{CCO} supplied to its I/O bank. The I/O standards supported are:

- LVTTTL
- LVCMOS 3.3
- LVCMOS 2.5
- LVCMOS 1.8
- LVCMOS 1.5
- 3.3V PCI Compatible

All of the I/Os and dedicated inputs have the capability to provide a bus-keeper latch, pull-up resistor or pull-down resistor selectable on a “per-pin” basis. A fourth option is to provide none of these. The default in both hardware and software is such that when the device is erased or if the user does not specify, the input structure is configured to be a Pull-down Resistor.

Each ispMACH 4000ZE device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for fast slew or slow slew. The typical edge rate difference between fast and slow slew setting is 20%. For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed.

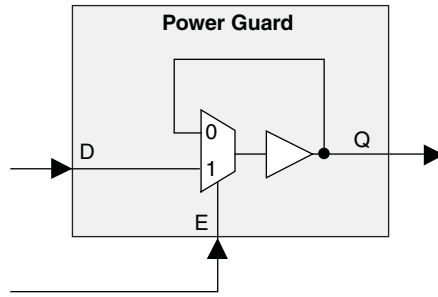
The ispMACH 4000ZE family has an always on, 200mV typical hysteresis for each input operational at 3.3V and 2.5V. This provides improved noise immunity for slow transitioning signals.

Power Guard

Power Guard allows easier achievement of standby current in the system. As shown in Figure 9, this feature consists of an enabling multiplexer between an I/O pin and input buffer, and its associated circuitry inside the device.

If the enable signal (E) is held low, all inputs (D) can be optionally isolated (guarded), such that, if any of these were toggled, it would not cause any toggle on internal pins (Q), thus, a toggling I/O pin will not cause any internal dynamic power consumption.

Figure 9. Power Guard

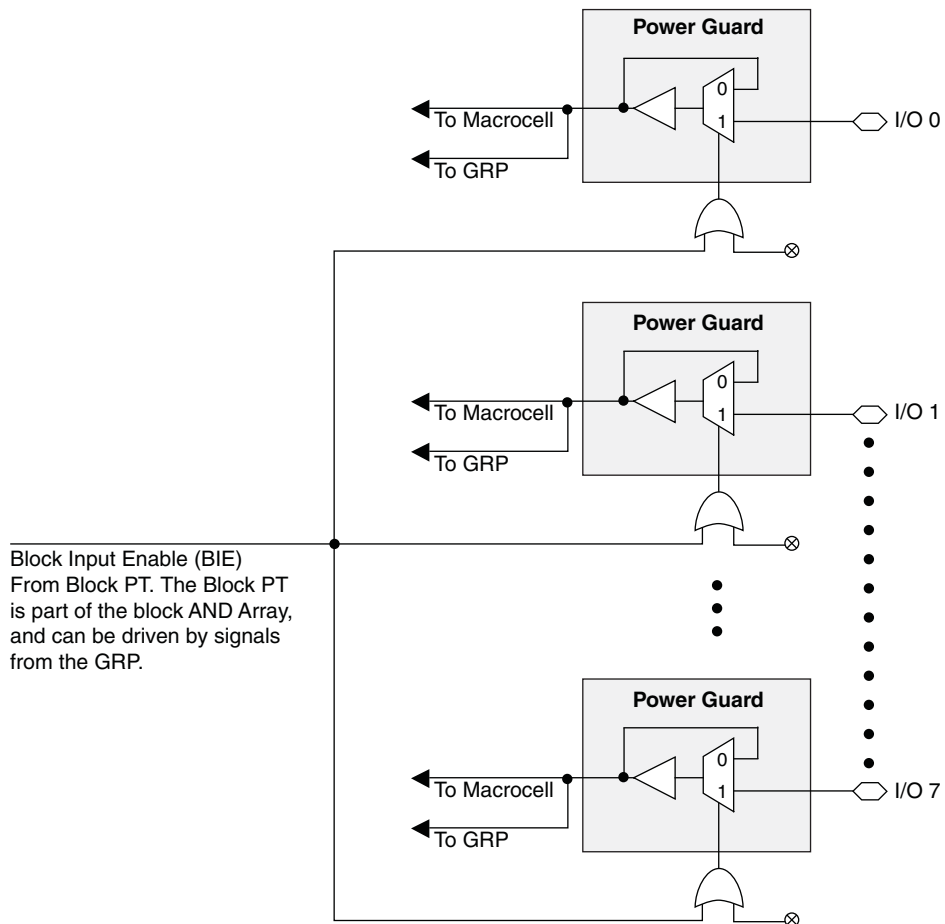


All the I/O pins in a block share a common Power Guard Enable signal. For a block of I/Os, this signal is called a Block Input Enable (BIE) signal. BIE can be internally generated using MC logic, or could come from external sources using one of the user I/O or input pins.

Any I/O pin in the block can be programmed to ignore the BIE signal. Thus, the feature can be enabled or disabled on a pin-by-pin basis.

Figure 10 shows Power Guard and BIE across multiple I/Os in a block that has eight I/Os.

Figure 10. Power Guard and BIE in a Block with 8 I/Os



The number of BIE inputs, thus the number of Power Guard “Blocks” that can exist in a device, depends on the device size. Table 8 shows the number of BIE signals available in the ispMACH 4000ZE family. The number of I/Os available in each block is shown in the Ordering Information section of this data sheet.

Table 8. Number of BIE Signals Available in ispMACH 4000ZE Devices

| Device | Number of Logic Blocks, Power Guard Blocks and BIE Signals |
|----------------|--|
| ispMACH 4032ZE | Two (Blocks: A and B) |
| ispMACH 4064ZE | Four (Blocks: A, B, C and D) |
| ispMACH 4128ZE | Eight (Blocks: A, B, C, ..., H) |
| ispMACH 4256ZE | Sixteen (Blocks: A, B, C, ..., P) |

Power Guard for Dedicated Inputs

Power Guard can optionally be applied to the dedicated inputs. The dedicated inputs and clocks are controlled by the BIE of the logic blocks shown in Tables 9 and 10.

Table 9. Dedicated Clock Inputs to BIE Association

| CLK/I | 32 MC Block | 64MC Block | 128MC Block | 256MC Block |
|----------|-------------|------------|-------------|-------------|
| CLK0 / I | A | A | A | A |
| CLK1 / I | A | B | D | H |
| CLK2 / I | B | C | E | I |
| CLK3 / I | B | D | H | P |

Table 10. Dedicated Inputs to BIE Association

| Dedicated Input | 4064ZE Block | 4128ZE Block | 4256ZE Block |
|-----------------|--------------|--------------|--------------|
| 0 | A | B | D |
| 1 | B | C | E |
| 2 | B | D | G |
| 3 | C | F | G |
| 4 | D | G | J |
| 5 | D | H | L |
| 6 | — | — | M |
| 7 | — | — | O |
| 8 | — | — | O |
| 9 | — | — | B |

For more information on the Power Guard function refer to TN1174, *Advanced Features of the ispMACH 4000ZE*.

Global OE (GOE) and Block Input Enable (BIE) Generation

Most ispMACH 4000ZE family devices have a 4-bit wide Global OE (GOE) Bus (Figure 11), except the ispMACH 4032 device that has a 2-bit wide Global OE Bus (Figure 12). This bus is derived from a 4-bit internal global OE (GOE) PT bus and two dual purpose I/O or GOE pins. Each signal that drives the bus can optionally be inverted.

Each GLB has a block-level OE PT that connects to all bits of the Global OE PT bus with four fuses. Hence, for a 256-macrocell device (with 16 blocks), each line of the bus is driven from 16 OE product terms. Figures 9 and 10 show a graphical representation of the global OE generation.

The block-level OE PT of each GLB is also tied to Block Input Enable (BIE) of that block. Hence, for a 256-macrocell device (with 16 blocks), each block’s BIE signal is driven by block-level OE PT from each block.

Figure 11. Global OE Generation for All Devices Except ispMACH 4032ZE

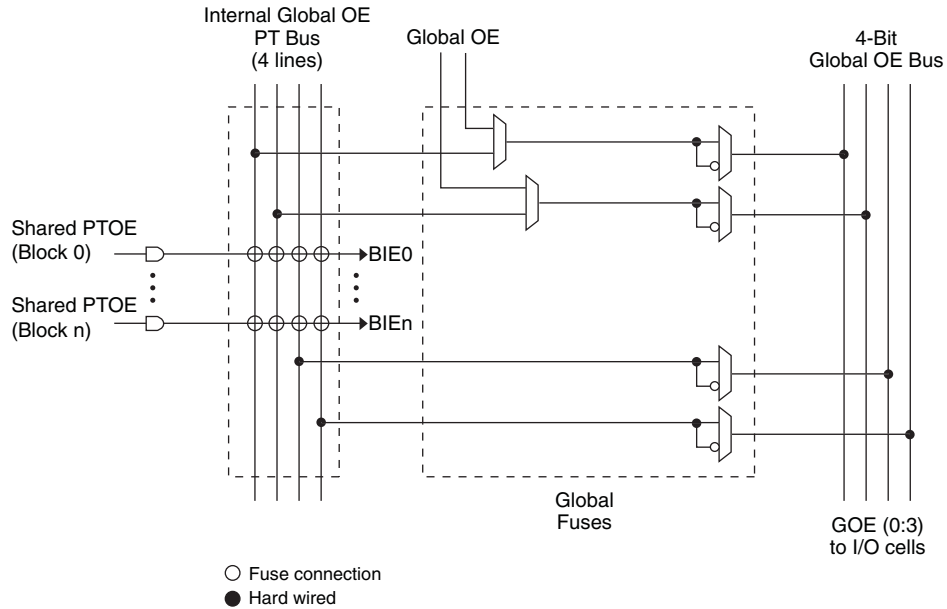
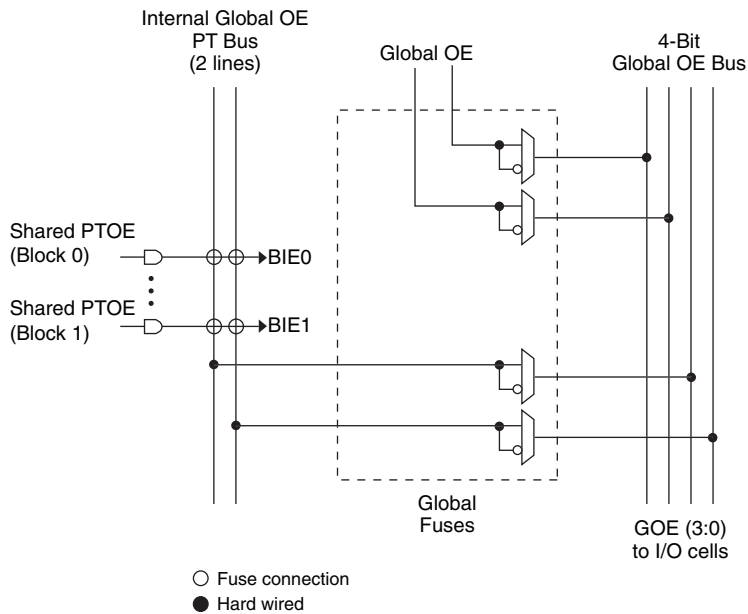


Figure 12. Global OE Generation for ispMACH 4032ZE



On-Chip Oscillator and Timer

An internal oscillator is provided for use in miscellaneous housekeeping functions such as watchdog heartbeats, digital de-glitch circuits and control state machines. The oscillator is disabled by default to save power. Figure 13 shows the block diagram of the oscillator and timer block.

Figure 13. On-Chip Oscillator and Timer



Table 11. On-Chip Oscillator and Timer Signal Names

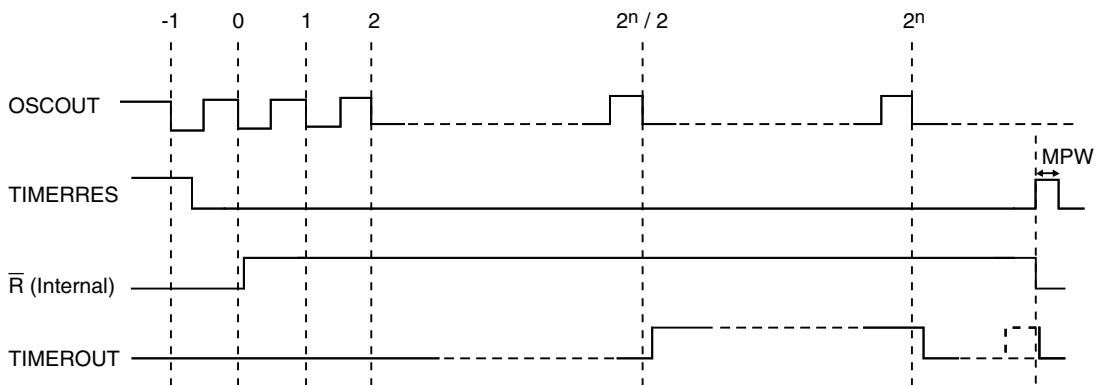
| Signal Name | Input or Output | Optional / Required | Description |
|-------------|-----------------|---------------------|--|
| OSCOUT | Output | Optional | Oscillator Output (Nominal Frequency: 5MHz) |
| TIMEROUT | Output | Optional | Oscillator Frequency Divided by an integer TIMER_DIV (Default 128) |
| TIMERRES | Input | Optional | Reset the Timer |
| DYNOSCDIS | Input | Optional | Disables the Oscillator, resets the Timer and saves the power. |

OSCTIMER has two outputs, OSCOUT and TIMEROUT. The outputs feed into the Global Routing Pool (GRP). From GRP, these signals can drive any macrocell input, as well as any output pin (with macrocell bypass). The output OSCOUT is the direct oscillator output with a typical frequency of 5MHz, whereas, the output TIMEROUT is the oscillator output divided by an attribute TIMER_DIV.

The attribute TIMER_DIV can be: 128 (7 bits), 1024 (10 bits) or 1,048,576 (20 bits). The divided output is provided for those user situations, where a very slow clock is desired. If even a slower toggling clock is desired, then the programmable macrocell resources can be used to further divide down the TIMEROUT output.

Figure 14 shows the simplified relationship among OSCOUT, TIMERRES and TIMEROUT. In the diagram, the signal “R̄” is an internal reset signal that is used to synchronize TIMERRES to OSCOUT. This adds one extra clock cycle delay for the first timer transition after TIMERRES.

Figure 14. Relationship Among OSCOUT, TIMERRES and TIMEROUT



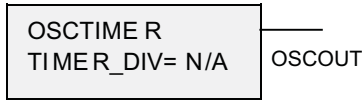
Note: n = Number of bits in the divider (7, 10 or 20)

Metastability: If the signal TIMERRES is not synchronous to OSCOUT, it could make a difference of one or two clock cycles to the TIMEROUT going high the first time.

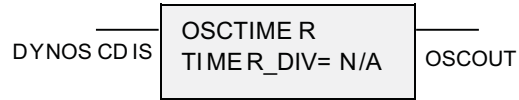
Some Simple Use Scenarios

The following diagrams show a few simple examples that omit optional signals for the OSCTIMER block:

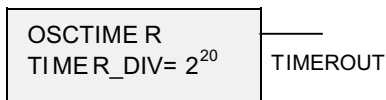
- A. An oscillator giving 5MHz nominal clock
- B. An oscillator that can be disabled with an external signal (5MHz nominal clock)
- C. An oscillator giving approximately 5 Hz nominal clock (TIMER_DIV = 2²⁰ (1,048,576))
- D. An oscillator giving two output clocks: ~5MHz and ~5KHz (TIMER_DIV= 2¹⁰ (1,024))



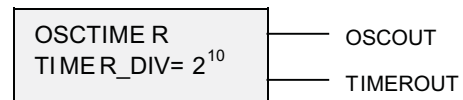
(A) A simple 5MHz oscillator.



(B) An oscillator with dynamic disable.



(C) A simple 5Hz oscillator.



(D) Oscillator with two outputs (5MHz and 5KHz).

OSCTIMER Integration With CPLD Fabric

The OSCTIMER is integrated into the CPLD fabric using the Global Routing Pool (GRP). The macrocell (MC) feedback path for two macrocells is augmented with a programmable multiplexer, as shown in Figure 15. The OSCTIMER outputs (OSCOUT and TIMEROUT) can optionally drive the GRP lines, whereas the macrocell outputs can drive the optional OSCTIMER inputs TIMERRES and DYNOSCDIS.

Figure 15. OSCTIMER Integration With CPLD Fabric

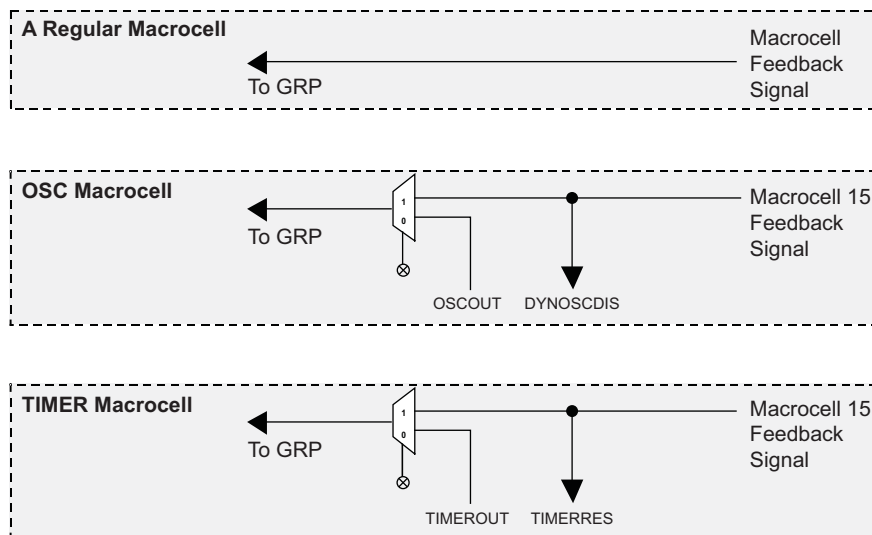


Table 12 shows how these two MCs are designated in each of the ispMACH4000ZE device.

Table 12. OSC and TIMER MC Designation

| Device | Macrocell | Block Number | MC Number |
|----------------|-----------|--------------|-----------|
| ispMACH 4032ZE | OSC MC | A | 15 |
| | TIMER MC | B | 15 |
| ispMACH 4064ZE | OSC MC | A | 15 |
| | TIMER MC | D | 15 |
| ispMACH 4128ZE | OSC MC | A | 15 |
| | TIMER MC | G | 15 |
| ispMACH 4256ZE | OSC MC | C | 15 |
| | TIMER MC | F | 15 |

Zero Power/Low Power and Power Management

The ispMACH 4000ZE family is designed with high speed low power design techniques to offer both high speed and low power. With an advanced E² low power cell and non sense-amplifier design approach (full CMOS logic approach), the ispMACH 4000ZE family offers fast pin-to-pin speeds, while simultaneously delivering low standby power without needing any “turbo bits” or other power management schemes associated with a traditional sense-amplifier approach.

The zero power ispMACH 4000ZE is based on the 1.8V ispMACH 4000Z family. With innovative circuit design changes, the ispMACH 4000ZE family is able to achieve the industry’s lowest static power.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispMACH 4000ZE devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more board-level testing. The test access port operates with an LVCMOS interface that corresponds to the power supply voltage.

I/O Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running any continuity tests. As these tests are fast, by nature, the overhead and time that is required for configuration of the I/Os’ physical nature should be minimal so that board test time is minimized. The ispMACH 4000ZE family of devices allows this by offering the user the ability to quickly configure the physical nature of the I/O cells. This quick configuration takes milliseconds to complete, whereas it takes seconds for the entire device to be programmed. Lattice’s ispVM™ System programming software can either perform the quick configuration through the PC parallel port, or can generate the ATE or test vectors necessary for a third-party test system.

IEEE 1532-Compliant In-System Programming

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispMACH 4000ZE devices provide In-System Programming (ISP™) capability through the Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains complaint to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, users get the benefit of a standard, well-defined interface. All ispMACH 4000ZE devices are also compliant with the IEEE 1532 standard.

The ispMACH 4000ZE devices can be programmed across the commercial temperature and voltage range. The PC-based Lattice software facilitates in-system programming of ispMACH 4000ZE devices. The software takes the JEDEC file output produced by the design implementation software, along with information about the scan chain, and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a scan chain via the parallel port of a PC. Alternatively, the software can output files in formats understood by common auto-

mated test equipment. This equipment can then be used to program ispMACH 4000ZE devices during the testing of a circuit board.

User Electronic Signature

The User Electronic Signature (UES) allows the designer to include identification bits or serial numbers inside the device, stored in E²CMOS memory. The ispMACH 4000ZE device contains 32 UES bits that can be configured by the user to store unique data such as ID codes, revision numbers or inventory control codes.

Security Bit

A programmable security bit is provided on the ispMACH 4000ZE devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

The ispMACH 4000ZE devices are well-suited for applications that require hot socketing capability. Hot socketing a device requires that the device, during power-up and down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of I/O pin loading be minimal on active signals. The ispMACH 4000ZE devices provide this capability for input voltages in the range 0V to 3.0V.

Density Migration

The ispMACH 4000ZE family has been designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization design targeted for a high density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

Absolute Maximum Ratings^{1, 2, 3}

- Supply Voltage (V_{CC}) -0.5 to 2.5V
- Output Supply Voltage (V_{CCO}) -0.5 to 4.5V
- Input or I/O Tristate Voltage Applied^{4,5} -0.5 to 5.5V
- Storage Temperature -65 to 150°C
- Junction Temperature (T_j) with Power Applied . . . -55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Undershoot of -2V and overshoot of ($V_{IH} (MAX) + 2V$), up to a total pin voltage of 6V is permitted for a duration of <20ns.
5. Maximum of 64 I/Os per device with $V_{IN} > 3.6V$ is allowed.

Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units | |
|----------|-----------------------------------|----------------------------|------------------|-------|---|
| V_{CC} | Supply Voltage | Standard Voltage Operation | 1.7 | 1.9 | V |
| | | Extended Voltage Operation | 1.6 ¹ | 1.9 | V |
| T_j | Junction Temperature (Commercial) | 0 | 90 | °C | |
| | Junction Temperature (Industrial) | -40 | 105 | °C | |

1. Devices operating at 1.6V can expect performance degradation up to 35%.

Erase Reprogram Specifications

| Parameter | Min. | Max. | Units |
|-----------------------|-------|------|--------|
| Erase/Reprogram Cycle | 1,000 | — | Cycles |

Note: Valid over commercial temperature range.

Hot Socketing Characteristics^{1,2,3}

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|------------------------------|--|------|------|------|-------|
| I_{DK} | Input or I/O Leakage Current | $0 \leq V_{IN} \leq 3.0V, T_j = 105^\circ C$ | — | ±30 | ±150 | µA |
| | | $0 \leq V_{IN} \leq 3.0V, T_j = 130^\circ C$ | — | ±30 | ±200 | µA |

1. Insensitive to sequence of V_{CC} or V_{CCO} . However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO} , provided $(V_{IN} - V_{CCO}) \leq 3.6V$.
2. $0 < V_{CC} < V_{CC} (MAX), 0 < V_{CCO} < V_{CCO} (MAX)$.
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH} . Device defaults to pull-up until fuse circuitry is active.

I/O Recommended Operating Conditions

| Standard | V_{CCO} (V) ¹ | |
|----------------------|----------------------------|------|
| | Min. | Max. |
| LVTTTL | 3.0 | 3.6 |
| LVC MOS 3.3 | 3.0 | 3.6 |
| Extended LVC MOS 3.3 | 2.7 | 3.6 |
| LVC MOS 2.5 | 2.3 | 2.7 |
| LVC MOS 1.8 | 1.65 | 1.95 |
| LVC MOS 1.5 | 1.4 | 1.6 |
| PCI 3.3 | 3.0 | 3.6 |

1. Typical values for V_{CCO} are the average of the min. and max. values.

DC Electrical Characteristics

Over Recommended Operating Conditions

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|------------------------|---------------------------------------|---|------------------|------|------------------|---------|
| $I_{IL}, I_{IH}^{1,2}$ | Input Leakage Current | $0 \leq V_{IN} < V_{CCO}$ | — | 0.5 | 1 | μA |
| I_{IH}^1 | Input High Leakage Current | $V_{CCO} < V_{IN} \leq 5.5V$ | — | — | 10 | μA |
| I_{PU} | I/O Weak Pull-up Resistor Current | $0 \leq V_{IN} \leq 0.7V_{CCO}$ | -20 | — | -150 | μA |
| I_{PD} | I/O Weak Pull-down Resistor Current | $V_{IL} (MAX) \leq V_{IN} \leq V_{IH} (MIN)$ | 30 | — | 150 | μA |
| I_{BHLS} | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL} (MAX)$ | 30 | — | — | μA |
| I_{BHHS} | Bus Hold High Sustaining Current | $V_{IN} = 0.7 V_{CCO}$ | -20 | — | — | μA |
| I_{BHLO} | Bus Hold Low Overdrive Current | $0V \leq V_{IN} \leq V_{BHT}$ | — | — | 150 | μA |
| I_{BHHO} | Bus Hold High Overdrive Current | $V_{BHT} \leq V_{IN} \leq V_{CCO}$ | — | — | -150 | μA |
| V_{BHT} | Bus Hold Trip Points | — | $V_{CCO} * 0.35$ | — | $V_{CCO} * 0.65$ | V |
| C_1 | I/O Capacitance ³ | $V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V$ | — | 8 | — | pf |
| | | $V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$ | — | | — | |
| C_2 | Clock Capacitance ³ | $V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V$ | — | 6 | — | pf |
| | | $V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$ | — | | — | |
| C_3 | Global Input Capacitance ³ | $V_{CCO} = 3.3V, 2.5V, 1.8V, 1.5V$ | — | 6 | — | pf |
| | | $V_{CC} = 1.8V, V_{IO} = 0$ to $V_{IH} (MAX)$ | — | | — | |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. I_{IH} excursions of up to 1.5 μA maximum per pin above the spec limit may be observed for certain voltage conditions on no more than 10% of the device's I/O pins.
3. Measured $T_A = 25^\circ C$, $f = 1.0MHz$.

Supply Current

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|------------------------------|--------------------------------|--|------|------|------|-------|
| ispMACH 4032ZE | | | | | | |
| ICC ^{1, 2, 3, 5, 6} | Operating Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 50 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 58 | — | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 60 | — | μA |
| ICC ^{4, 5, 6} | Standby Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 10 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 13 | 25 | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 15 | 40 | μA |
| ispMACH 4064ZE | | | | | | |
| ICC ^{1, 2, 3, 5, 6} | Operating Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 80 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 89 | — | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 92 | — | μA |
| ICC ^{4, 5, 6} | Standby Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 11 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 15 | 30 | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 18 | 50 | μA |
| ispMACH 4128ZE | | | | | | |
| ICC ^{1, 2, 3, 5, 6} | Operating Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 168 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 190 | — | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 195 | — | μA |
| ICC ^{4, 5, 6} | Standby Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 12 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 16 | 40 | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 19 | 60 | μA |
| ispMACH 4256ZE | | | | | | |
| ICC ^{1, 2, 3, 5, 6} | Operating Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 341 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 361 | — | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 372 | — | μA |
| ICC ^{4, 5, 6} | Standby Power Supply Current | V _{CC} = 1.8V, T _A = 25°C | — | 13 | — | μA |
| | | V _{CC} = 1.9V, T _A = 0 to 70°C | — | 32 | 65 | μA |
| | | V _{CC} = 1.9V, T _A = -40 to 85°C | — | 43 | 100 | μA |

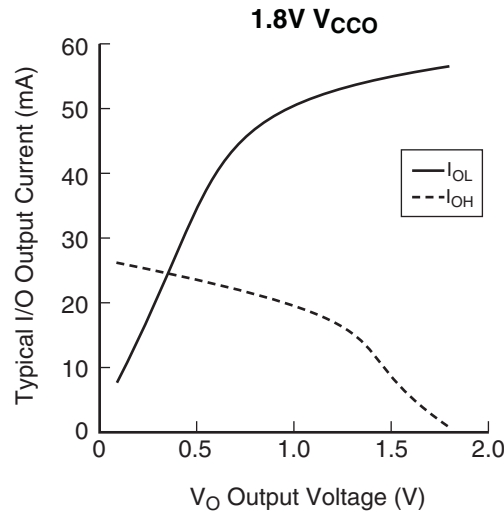
1. Frequency = 1.0 MHz.
2. Device configured with 16-bit counters.
3. I_{CC} varies with specific device configuration and operating frequency.
4. V_{CCO} = 3.6V, V_{IN} = 0V or V_{CCO}, bus maintenance turned off. V_{IN} above V_{CCO} will add transient current above the specified standby I_{CC}.
5. Includes V_{CCO} current without output loading.
6. This operating supply current is with the internal oscillator disabled. Enabling the internal oscillator adds approximately 15μA typical current plus additional current from any logic it drives.

I/O DC Electrical Characteristics

Over Recommended Operating Conditions

| Standard | V_{IL} | | V_{IH} | | V_{OL} Max (V) | V_{OH} Min (V) | I_{OL}^1 (mA) | I_{OH}^1 (mA) |
|-------------------------|----------|------------------------------|------------------------------|---------|---------------------|---------------------|--------------------|--------------------|
| | Min (V) | Max (V) | Min (V) | Max (V) | | | | |
| LVTTTL | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO} - 0.40$ | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO} - 0.20$ | 0.1 | -0.1 |
| LVCMOS 3.3 | -0.3 | 0.80 | 2.0 | 5.5 | 0.40 | $V_{CCO} - 0.40$ | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO} - 0.20$ | 0.1 | -0.1 |
| LVCMOS 2.5 | -0.3 | 0.70 | 1.70 | 3.6 | 0.40 | $V_{CCO} - 0.40$ | 8.0 | -4.0 |
| | | | | | 0.20 | $V_{CCO} - 0.20$ | 0.1 | -0.1 |
| LVCMOS 1.8 | -0.3 | $0.35 * V_{CC}$ | $0.65 * V_{CC}$ | 3.6 | 0.40 | $V_{CCO} - 0.45$ | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO} - 0.20$ | 0.1 | -0.1 |
| LVCMOS 1.5 ² | -0.3 | $0.35 * V_{CC}$ | $0.65 * V_{CC}$ | 3.6 | 0.40 | $V_{CCO} - 0.45$ | 2.0 | -2.0 |
| | | | | | 0.20 | $V_{CCO} - 0.20$ | 0.1 | -0.1 |
| PCI 3.3 | -0.3 | $0.3 * 3.3 * (V_{CC} / 1.8)$ | $0.5 * 3.3 * (V_{CC} / 1.8)$ | 5.5 | $0.1 V_{CCO}$ | $0.9 V_{CCO}$ | 1.5 | -0.5 |

1. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed $n * 8\text{mA}$. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.
2. For 1.5V inputs, there may be an additional DC current drawn from V_{CC} , if the ispMACH 4000ZE V_{CC} and the V_{CC} of the driving device (V_{CCd-d} ; that determines steady state V_{IH}) are in the extreme range of their specifications. Typically, DC current drawn from V_{CC} will be $2\mu\text{A}$ per input.



ispMACH 4000ZE External Switching Characteristics

Over Recommended Operating Conditions

| Parameter | Description ^{1,2} | LC4032ZE | | LC4064ZE | | All Devices | | | | Units |
|--|---|----------|------|----------|------|-------------|------|------|------|-------|
| | | -4 | | -4 | | -5 | | -7 | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{PD} | 20-PT combinatorial propagation delay | — | 4.4 | — | 4.7 | — | 5.8 | — | 7.5 | ns |
| t _S | GLB register setup time before clock | 2.2 | — | 2.5 | — | 2.9 | — | 4.5 | — | ns |
| t _{ST} | GLB register setup time before clock with T-type register | 2.4 | — | 2.7 | — | 3.1 | — | 4.7 | — | ns |
| t _{SIR} | GLB register setup time before clock, input register path | 1.0 | — | 1.1 | — | 1.3 | — | 1.4 | — | ns |
| t _{SIRZ} | GLB register setup time before clock with zero hold | 2.0 | — | 2.1 | — | 2.9 | — | 4.0 | — | ns |
| t _H | GLB register hold time after clock | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| t _{HT} | GLB register hold time after clock with T-type register | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| t _{HIR} | GLB register hold time after clock, input register path | 1.0 | — | 1.0 | — | 1.3 | — | 1.3 | — | ns |
| t _{HIRZ} | GLB register hold time after clock, input register path with zero hold | 0.0 | — | 0.0 | — | 0.0 | — | 0.0 | — | ns |
| t _{CO} | GLB register clock-to-output delay | — | 3.0 | — | 3.2 | — | 3.8 | — | 4.5 | ns |
| t _R | External reset pin to output delay | — | 5.0 | — | 6.0 | — | 7.5 | — | 9.0 | ns |
| t _{RW} | External reset pulse duration | 1.5 | — | 1.7 | — | 2.0 | — | 4.0 | — | ns |
| t _{P_{TOE/DIS}} | Input to output local product term output enable/disable | — | 7.0 | — | 8.0 | — | 8.2 | — | 9.0 | ns |
| t _{G_{P_{TOE/DIS}}} | Input to output global product term output enable/disable | — | 6.5 | — | 7.0 | — | 10.0 | — | 10.5 | ns |
| t _{GOE/DIS} | Global OE input to output enable/disable | — | 4.5 | — | 4.5 | — | 5.5 | — | 7.0 | ns |
| t _{CW} | Global clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | 3.3 | — | ns |
| t _{GW} | Global gate width low (for low transparent) or high (for high transparent) | 1.0 | — | 1.5 | — | 1.8 | — | 3.3 | — | ns |
| t _{WIR} | Input register clock width, high or low | 1.0 | — | 1.5 | — | 1.8 | — | 3.3 | — | ns |
| f _{MAX (Int.)} ³ | Clock frequency with internal feedback | 260 | — | 241 | — | 200 | — | 172 | — | MHz |
| f _{MAX (Ext.)} | clock frequency with external feedback, [1 / (t _S + t _{CO})] | 192 | — | 175 | — | 149 | — | 111 | — | MHz |

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate other standards.

2. Measured using standard switching GRP loading of 1 and 1 output switching.

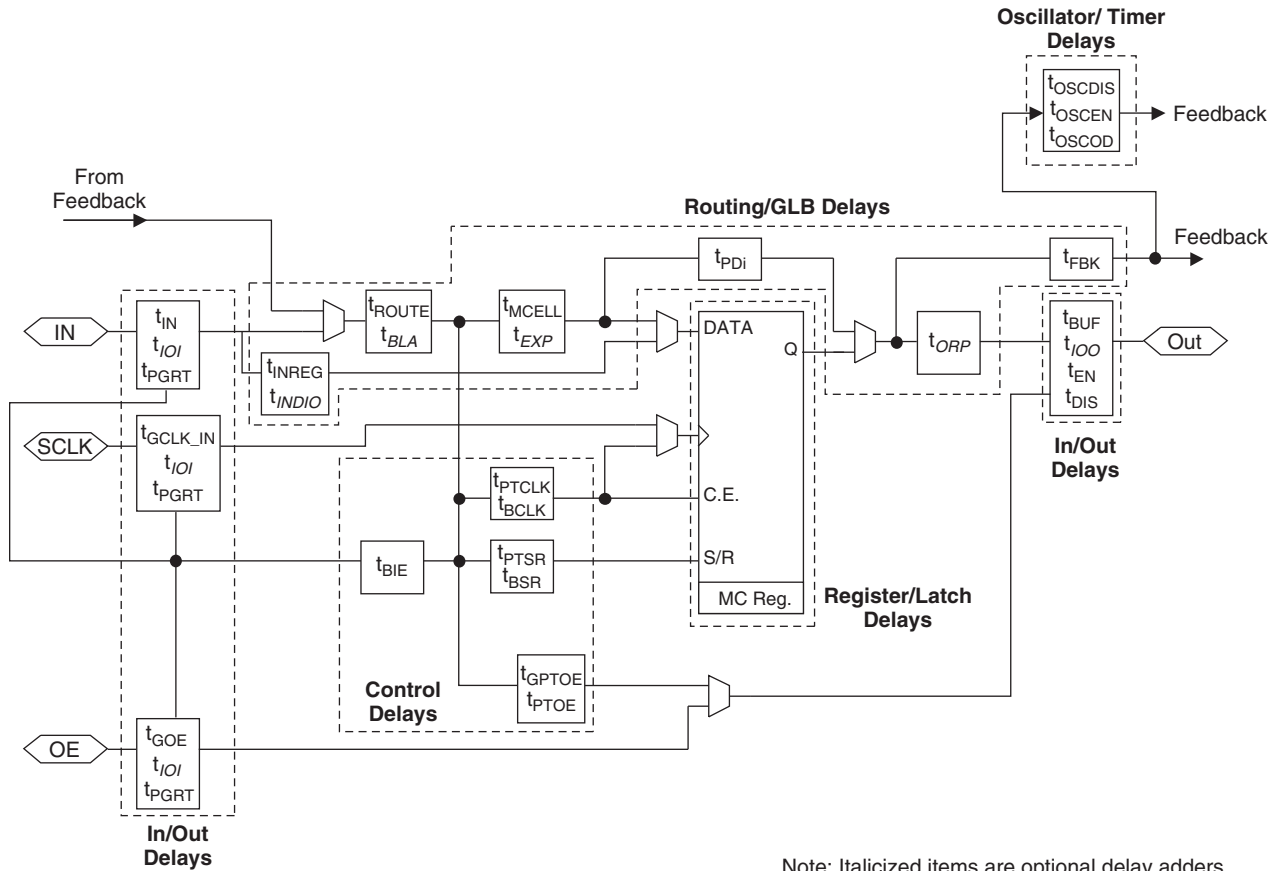
3. Standard 16-bit counter using GRP feedback.

Timing v.0.8

Timing Model

The task of determining the timing through the ispMACH 400ZE family, like any CPLD, is relatively simple. The timing model provided in Figure 16 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the software report file, the delay path of the function can easily be determined from the timing model. The Lattice design tools report the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device. For more information on the timing model and usage, please refer to technical note TN1168, *ispMACH 400ZE Timing Model Design and Usage Guidelines*.

Figure 16. ispMACH 400ZE Timing Model



Note: Italicized items are optional delay adders.

ispMACH 400ZE Internal Timing Parameters

Over Recommended Operating Conditions

| Parameter | Description | LC4032ZE | | LC4064ZE | | Units |
|------------------------------|--|----------|------|----------|------|-------|
| | | -4 | | -4 | | |
| | | Min. | Max. | Min. | Max. | |
| In/Out Delays | | | | | | |
| t_{IN} | Input Buffer Delay | — | 0.85 | — | 0.90 | ns |
| t_{GCLK_IN} | Global Clock Input Buffer Delay | — | 1.60 | — | 1.60 | ns |
| t_{GOE} | Global OE Pin Delay | — | 2.25 | — | 2.25 | ns |
| t_{BUF} | Delay through Output Buffer | — | 0.75 | — | 0.90 | ns |
| t_{EN} | Output Enable Time | — | 2.25 | — | 2.25 | ns |
| t_{DIS} | Output Disable Time | — | 1.35 | — | 1.35 | ns |
| t_{PGSU} | Input Power Guard Setup Time | — | 3.30 | — | 3.55 | ns |
| t_{PGH} | Input Power Guard Hold Time | — | 0.00 | — | 0.00 | ns |
| t_{PGPW} | Input Power Guard BIE Minimum Pulse Width | — | 5.00 | — | 5.00 | ns |
| t_{PGRT} | Input Power Guard Recovery Time Following BIE Dissertation | — | 5.00 | — | 5.00 | ns |
| Routing Delays | | | | | | |
| t_{ROUTE} | Delay through GRP | — | 1.60 | — | 1.70 | ns |
| t_{PDI} | Macrocell Propagation Delay | — | 0.25 | — | 0.25 | ns |
| t_{MCELL} | Macrocell Delay | — | 0.65 | — | 0.65 | ns |
| t_{INREG} | Input Buffer to Macrocell Register Delay | — | 0.90 | — | 1.00 | ns |
| t_{FBK} | Internal Feedback Delay | — | 0.55 | — | 0.55 | ns |
| t_{ORP} | Output Routing Pool Delay | — | 0.30 | — | 0.30 | ns |
| Register/Latch Delays | | | | | | |
| t_S | D-Register Setup Time (Global Clock) | 0.70 | — | 0.85 | — | ns |
| t_{S_PT} | D-Register Setup Time (Product Term Clock) | 1.25 | — | 1.85 | — | ns |
| t_H | D-Register Hold Time | 1.50 | — | 1.65 | — | ns |
| t_{ST} | T-Register Setup Time (Global Clock) | 0.90 | — | 1.05 | — | ns |
| t_{ST_PT} | T-register Setup Time (Product Term Clock) | 1.45 | — | 1.65 | — | ns |
| t_{HT} | T-Resister Hold Time | 1.50 | — | 1.65 | — | ns |
| t_{SIR} | D-Input Register Setup Time (Global Clock) | 0.85 | — | 0.80 | — | ns |
| t_{SIR_PT} | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | ns |
| t_{HIR} | D-Input Register Hold Time (Global Clock) | 1.15 | — | 1.30 | — | ns |
| t_{HIR_PT} | D-Input Register Hold Time (Product Term Clock) | 0.90 | — | 1.10 | — | ns |
| t_{COi} | Register Clock to Output/Feedback MUX Time | — | 0.35 | — | 0.40 | ns |
| t_{CES} | Clock Enable Setup Time | 1.00 | — | 2.00 | — | ns |
| t_{CEH} | Clock Enable Hold Time | 0.00 | — | 0.00 | — | ns |
| t_{SL} | Latch Setup Time (Global Clock) | 0.70 | — | 0.95 | — | ns |
| t_{SL_PT} | Latch Setup Time (Product Term Clock) | 1.45 | — | 1.85 | — | ns |
| t_{HL} | Latch Hold Time | 1.40 | — | 1.80 | — | ns |
| t_{GOi} | Latch Gate to Output/Feedback MUX Time | — | 0.40 | — | 0.35 | ns |
| t_{PDLi} | Propagation Delay through Transparent Latch to Output/Feedback MUX | — | 0.30 | — | 0.25 | ns |
| t_{SRI} | Asynchronous Reset or Set to Output/Feedback MUX Delay | — | 0.30 | — | 0.30 | ns |

ispMACH 400ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

| Parameter | Description | LC4032ZE | | LC4064ZE | | Units | |
|--|---|--|-------|----------|-------|-------|----|
| | | -4 | | -4 | | | |
| | | Min. | Max. | Min. | Max. | | |
| t _{SRR} | Asynchronous Reset or Set Recovery Delay | — | 2.00 | — | 1.70 | ns | |
| Control Delays | | | | | | | |
| t _{BCLK} | GLB PT Clock Delay | — | 1.20 | — | 1.30 | ns | |
| t _{PTCLK} | Macrocell PT Clock Delay | — | 1.40 | — | 1.50 | ns | |
| t _{BSR} | Block PT Set/Reset Delay | — | 1.10 | — | 1.85 | ns | |
| t _{PTSR} | Macrocell PT Set/Reset Delay | — | 1.20 | — | 1.90 | ns | |
| t _{BIE} | Power Guard Block Input Enable Delay | — | 1.60 | — | 1.70 | ns | |
| t _{P_{TOE}} | Macrocell PT OE Delay | — | 2.30 | — | 3.15 | ns | |
| t _{GPTOE} | Global PT OE Delay | — | 1.80 | — | 2.15 | ns | |
| Internal Oscillator | | | | | | | |
| t _{O_{SCSU}} | Oscillator DYNOSCDIS Setup Time | 5.00 | — | 5.00 | — | ns | |
| t _{O_{SCH}} | Oscillator DYNOSCDIS Hold Time | 5.00 | — | 5.00 | — | ns | |
| t _{O_{SCEN}} | Oscillator OSCOUT Enable Time (To Stable) | — | 5.00 | — | 5.00 | ns | |
| t _{O_{SCOD}} | Oscillator Output Delay | — | 4.00 | — | 4.00 | ns | |
| t _{O_{SCNOM}} | Oscillator OSCOUT Nominal Frequency | — | 5.00 | — | 5.00 | MHz | |
| t _{O_{SCvar}} | Oscillator Variation of Nominal Frequency | — | 30 | — | 30 | % | |
| t _{T_{MRCO20}} | Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider) | — | 12.50 | — | 12.50 | ns | |
| t _{T_{MRCO10}} | Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider) | — | 7.50 | — | 7.50 | ns | |
| t _{T_{MRCO7}} | Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider) | — | 6.00 | — | 6.00 | ns | |
| t _{T_{MRRSTO}} | Oscillator TIMEROUT Reset to Out (Going Low) | — | 5.00 | — | 5.00 | ns | |
| t _{T_{MRRR}} | Oscillator TIMEROUT Asynchronous Reset Recovery Delay | — | 4.00 | — | 4.00 | ns | |
| t _{T_{MRRSTPW}} | Oscillator TIMEROUT Reset Minimum Pulse Width | 3.00 | — | 3.00 | — | ns | |
| Optional Delay Adjusters | | Base Parameter | | | | | |
| t _{I_{NDIO}} | Input Register Delay | t _{I_{NREG}} | — | 1.00 | — | 1.00 | ns |
| t _{E_{XP}} | Product Term Expander Delay | t _{M_{CELL}} | — | 0.40 | — | 0.40 | ns |
| t _{B_{LA}} | Additional Block Loading Adders | t _{R_{ROUTE}} | — | 0.04 | — | 0.05 | ns |
| t_{I_{OI}} Input Buffer Delays | | | | | | | |
| LVTTL_in | Using LVTTTL standard | t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}} | — | 0.60 | — | 0.60 | ns |
| LVC _{MOS15_in} | Using LVC _{MOS} 1.5 Standard | t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}} | — | 0.20 | — | 0.20 | ns |
| LVC _{MOS18_in} | Using LVC _{MOS} 1.8 Standard | t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}} | — | 0.00 | — | 0.00 | ns |
| LVC _{MOS25_in} | Using LVC _{MOS} 2.5 Standard with Hysteresis | t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}} | — | 0.80 | — | 0.80 | ns |
| LVC _{MOS33_in} | Using LVC _{MOS} 3.3 Standard with Hysteresis | t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}} | — | 0.80 | — | 0.80 | ns |
| PCI_in | Using PCI Compatible Input with Hysteresis | t _{I_N} , t _{G_{CLK_IN}} , t _{G_{OE}} | — | 0.80 | — | 0.80 | ns |
| t_{I_{OO}} Output Buffer Delays | | | | | | | |
| LVTTL_out | Output Configured as TTL Buffer | t _{E_N} , t _{D_{IS}} , t _{B_{UF}} | — | 0.20 | — | 0.20 | ns |
| LVC _{MOS15_out} | Output Configured as 1.5V Buffer | t _{E_N} , t _{D_{IS}} , t _{B_{UF}} | — | 0.20 | — | 0.20 | ns |

ispMACH 400ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

| Parameter | Description | | LC4032ZE | | LC4064ZE | | Units |
|---------------|--|----------------------------------|----------|------|----------|------|-------|
| | | | -4 | | -4 | | |
| | | | Min. | Max. | Min. | Max. | |
| LVC MOS18_out | Output Configured as 1.8V Buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.00 | — | 0.00 | ns |
| LVC MOS25_out | Output Configured as 2.5V Buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.10 | — | 0.10 | ns |
| LVC MOS33_out | Output Configured as 3.3V Buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.20 | — | 0.20 | ns |
| PCI_out | Output Configured as PCI Compatible Buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.20 | — | 0.20 | ns |
| Slow Slew | Output Configured for Slow Slew Rate | t_{EN} , t_{BUF} | — | 1.00 | — | 1.00 | ns |

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

ispMACH 400ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

| Parameter | Description | All Devices | | | | Units |
|------------------------------|--|-------------|------|------|------|-------|
| | | -5 | | -7 | | |
| | | Min. | Max. | Min. | Max. | |
| In/Out Delays | | | | | | |
| t_{IN} | Input Buffer Delay | — | 1.05 | — | 1.90 | ns |
| t_{GCLK_IN} | Global Clock Input Buffer Delay | — | 1.95 | — | 2.15 | ns |
| t_{GOE} | Global OE Pin Delay | — | 3.00 | — | 4.30 | ns |
| t_{BUF} | Delay through Output Buffer | — | 1.10 | — | 1.30 | ns |
| t_{EN} | Output Enable Time | — | 2.50 | — | 2.70 | ns |
| t_{DIS} | Output Disable Time | — | 2.50 | — | 2.70 | ns |
| t_{PGSU} | Input Power Guard Setup Time | — | 4.30 | — | 5.60 | ns |
| t_{PGH} | Input Power Guard Hold Time | — | 0.00 | — | 0.00 | ns |
| t_{PGPW} | Input Power Guard BIE Minimum Pulse Width | — | 6.00 | — | 8.00 | ns |
| t_{PGRT} | Input Power Guard Recovery Time Following BIE Dis- sertation | — | 5.00 | — | 7.00 | ns |
| Routing Delays | | | | | | |
| t_{ROUTE} | Delay through GRP | — | 2.25 | — | 2.50 | ns |
| t_{PDi} | Macrocell Propagation Delay | — | 0.45 | — | 0.50 | ns |
| t_{MCELL} | Macrocell Delay | — | 0.65 | — | 1.00 | ns |
| t_{INREG} | Input Buffer to Macrocell Register Delay | — | 1.00 | — | 1.00 | ns |
| t_{FBK} | Internal Feedback Delay | — | 0.75 | — | 0.30 | ns |
| t_{ORP} | Output Routing Pool Delay | — | 0.30 | — | 0.30 | ns |
| Register/Latch Delays | | | | | | |
| t_S | D-Register Setup Time (Global Clock) | 0.90 | — | 1.25 | — | ns |
| t_{S_PT} | D-Register Setup Time (Product Term Clock) | 2.00 | — | 2.35 | — | ns |
| t_H | D-Register Hold Time | 2.00 | — | 3.25 | — | ns |
| t_{ST} | T-Register Setup Time (Global Clock) | 1.10 | — | 1.45 | — | ns |
| t_{ST_PT} | T-register Setup Time (Product Term Clock) | 2.20 | — | 2.65 | — | ns |
| t_{HT} | T-Register Hold Time | 2.00 | — | 3.25 | — | ns |
| t_{SIR} | D-Input Register Setup Time (Global Clock) | 1.20 | — | 0.65 | — | ns |
| t_{SIR_PT} | D-Input Register Setup Time (Product Term Clock) | 1.45 | — | 1.45 | — | ns |
| t_{HIR} | D-Input Register Hold Time (Global Clock) | 1.40 | — | 2.05 | — | ns |
| t_{HIR_PT} | D-Input Register Hold Time (Product Term Clock) | 1.10 | — | 1.20 | — | ns |
| t_{COi} | Register Clock to Output/Feedback MUX Time | — | 0.45 | — | 0.75 | ns |
| t_{CES} | Clock Enable Setup Time | 2.00 | — | 2.00 | — | ns |
| t_{CEH} | Clock Enable Hold Time | 0.00 | — | 0.00 | — | ns |
| t_{SL} | Latch Setup Time (Global Clock) | 0.90 | — | 1.55 | — | ns |
| t_{SL_PT} | Latch Setup Time (Product Term Clock) | 2.00 | — | 2.05 | — | ns |
| t_{HL} | Latch Hold Time | 2.00 | — | 1.17 | — | ns |
| t_{GOi} | Latch Gate to Output/Feedback MUX Time | — | 0.35 | — | 0.33 | ns |
| t_{PDLi} | Propagation Delay through Transparent Latch to Output/ Feedback MUX | — | 0.25 | — | 0.25 | ns |
| t_{SRi} | Asynchronous Reset or Set to Output/Feedback MUX Delay | — | 0.95 | — | 0.28 | ns |

ispMACH 400ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

| Parameter | Description | All Devices | | | | Units | |
|---|---|---|-------|------|-------|-------|----|
| | | -5 | | -7 | | | |
| | | Min. | Max. | Min. | Max. | | |
| t _{SRR} | Asynchronous Reset or Set Recovery Delay | — | 1.80 | — | 1.67 | ns | |
| Control Delays | | | | | | | |
| t _{BCLK} | GLB PT Clock Delay | — | 1.45 | — | 0.95 | ns | |
| t _{PTCLK} | Macrocell PT Clock Delay | — | 1.45 | — | 1.15 | ns | |
| t _{BSR} | Block PT Set/Reset Delay | — | 1.85 | — | 1.83 | ns | |
| t _{PTSR} | Macrocell PT Set/Reset Delay | — | 1.85 | — | 2.72 | ns | |
| t _{BIE} | Power Guard Block Input Enable Delay | — | 1.75 | — | 1.95 | ns | |
| t _{P_{TOE}} | Macrocell PT OE Delay | — | 2.40 | — | 1.90 | ns | |
| t _{GPTOE} | Global PT OE Delay | — | 4.20 | — | 3.40 | ns | |
| Internal Oscillator | | | | | | | |
| t _{OSCSU} | Oscillator DYNOSCDIS Setup Time | 5.00 | — | 5.00 | — | ns | |
| t _{OSCH} | Oscillator DYNOSCDIS Hold Time | 5.00 | — | 5.00 | — | ns | |
| t _{OSCEN} | Oscillator OSCOUT Enable Time (To Stable) | — | 5.00 | — | 5.00 | ns | |
| t _{OSCOD} | Oscillator Output Delay | — | 4.00 | — | 4.00 | ns | |
| t _{OSCNOM} | Oscillator OSCOUT Nominal Frequency | — | 5.00 | — | 5.00 | MHz | |
| t _{OSCvar} | Oscillator Variation of Nominal Frequency | — | 30 | — | 30 | % | |
| t _{TMRCO20} | Oscillator TIMEROUT Clock (Negative Edge) to Out (20-Bit Divider) | — | 12.50 | — | 14.50 | ns | |
| t _{TMRCO10} | Oscillator TIMEROUT Clock (Negative Edge) to Out (10-Bit Divider) | — | 7.50 | — | 9.50 | ns | |
| t _{TMRCO7} | Oscillator TIMEROUT Clock (Negative Edge) to Out (7-Bit Divider) | — | 6.00 | — | 8.00 | ns | |
| t _{TMRRSTO} | Oscillator TIMEROUT Reset to Out (Going Low) | — | 5.00 | — | 7.00 | ns | |
| t _{TMRRR} | Oscillator TIMEROUT Asynchronous Reset Recovery Delay | — | 4.00 | — | 6.00 | ns | |
| t _{TMRRSTPW} | Oscillator TIMEROUT Reset Minimum Pulse Width | 3.00 | — | 5.00 | — | ns | |
| Optional Delay Adjusters | | Base Parameter | | | | | |
| t _{INDIO} | Input Register Delay | t _{INREG} | — | 1.60 | — | 2.60 | ns |
| t _{EXP} | Product Term Expander Delay | t _{MCELL} | — | 0.45 | — | 0.50 | ns |
| t _{BLA} | Additional Block Loading Adders | t _{ROUTE} | — | 0.05 | — | 0.05 | ns |
| t_{IOI} Input Buffer Delays | | | | | | | |
| LVTTL_in | Using LVTTTL standard | t _{IN} , t _{GCLK_IN} , t _{GOE} | — | 0.60 | — | 0.60 | ns |
| LVC MOS15_in | Using LVC MOS 1.5 standard | t _{IN} , t _{GCLK_IN} , t _{GOE} | — | 0.20 | — | 0.20 | ns |
| LVC MOS18_in | Using LVC MOS 1.8 standard | t _{IN} , t _{GCLK_IN} , t _{GOE} | — | 0.00 | — | 0.00 | ns |
| LVC MOS25_in | Using LVC MOS 2.5 standard with Hysteresis | t _{IN} , t _{GCLK_IN} , t _{GOE} | — | 0.80 | — | 0.80 | ns |
| LVC MOS33_in | Using LVC MOS 3.3 standard with Hysteresis | t _{IN} , t _{GCLK_IN} , t _{GOE} | — | 0.80 | — | 0.80 | ns |
| PCI_in | Using PCI compatible input with Hysteresis | t _{IN} , t _{GCLK_IN} , t _{GOE} | — | 0.80 | — | 0.80 | ns |
| t_{IOO} Output Buffer Delays | | | | | | | |
| LVTTL_out | Output configured as TTL buffer | t _{EN} , t _{DIS} , t _{BUF} | — | 0.20 | — | 0.20 | ns |

ispMACH 400ZE Internal Timing Parameters (Cont.)

Over Recommended Operating Conditions

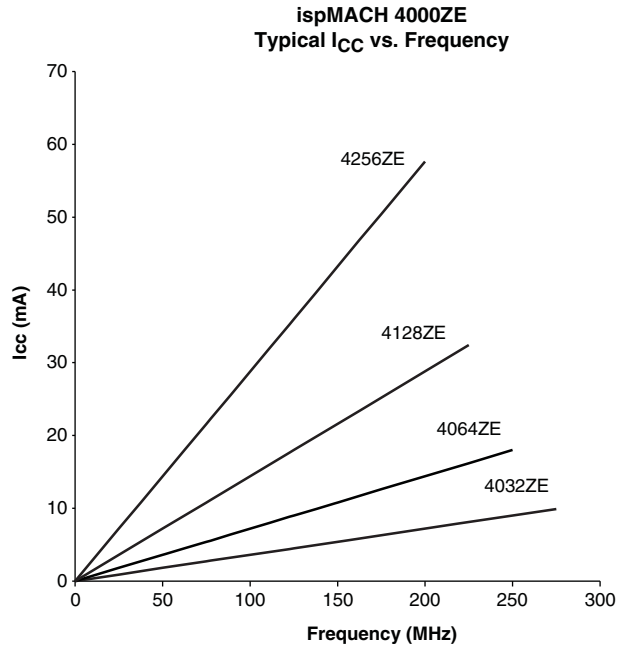
| Parameter | Description | All Devices | | | | Units | |
|---------------|--|----------------------------------|------|------|------|-------|----|
| | | -5 | | -7 | | | |
| | | Min. | Max. | Min. | Max. | | |
| LVC MOS15_out | Output configured as 1.5V buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.20 | — | 0.20 | ns |
| LVC MOS18_out | Output configured as 1.8V buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.00 | — | 0.00 | ns |
| LVC MOS25_out | Output configured as 2.5V buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.10 | — | 0.10 | ns |
| LVC MOS33_out | Output configured as 3.3V buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.20 | — | 0.20 | ns |
| PCI_out | Output configured as PCI compatible buffer | t_{EN} , t_{DIS} , t_{BUF} | — | 0.20 | — | 0.20 | ns |
| Slow Slew | Output configured for slow slew rate | t_{EN} , t_{BUF} | — | 1.00 | — | 1.00 | ns |

Note: Internal Timing Parameters are not tested and are for reference only. Refer to the timing model in this data sheet for further details.
Timing v.0.8

Boundary Scan Waveforms and Timing Specifications

| Symbol | Parameter | Min. | Max. | Units |
|--------------|--|------|------|-------|
| t_{BTCP} | TCK [BSCAN test] clock cycle | 40 | — | ns |
| t_{BTCH} | TCK [BSCAN test] pulse width high | 20 | — | ns |
| t_{BTCL} | TCK [BSCAN test] pulse width low | 20 | — | ns |
| t_{BTSU} | TCK [BSCAN test] setup time | 8 | — | ns |
| t_{BTH} | TCK [BSCAN test] hold time | 10 | — | ns |
| t_{BRF} | TCK [BSCAN test] rise and fall time | 50 | — | mV/ns |
| t_{BTO} | TAP controller falling edge of clock to valid output | — | 10 | ns |
| t_{BTOZ} | TAP controller falling edge of clock to data output disable | — | 10 | ns |
| t_{BTV0} | TAP controller falling edge of clock to data output enable | — | 10 | ns |
| t_{BTCPSU} | BSCAN test Capture register setup time | 8 | — | ns |
| t_{BTCPH} | BSCAN test Capture register hold time | 10 | — | ns |
| t_{BTU0} | BSCAN test Update reg, falling edge of clock to valid output | — | 25 | ns |
| t_{BTU0Z} | BSCAN test Update reg, falling edge of clock to output disable | — | 25 | ns |
| t_{BTU0V} | BSCAN test Update reg, falling edge of clock to output enable | — | 25 | ns |

Power Consumption



Power Estimation Coefficients¹

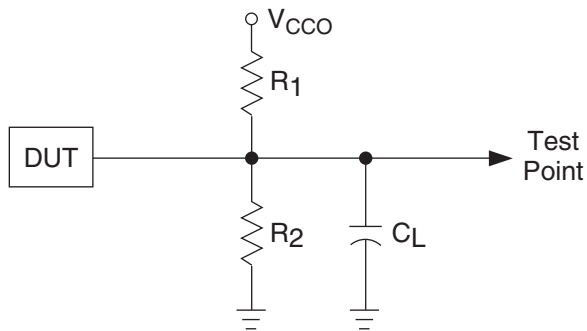
| Device | A | B |
|----------------|-------|-------|
| ispMACH 4032ZE | 0.010 | 0.009 |
| ispMACH 4064ZE | 0.011 | 0.009 |
| ispMACH 4128ZE | 0.012 | 0.009 |
| ispMACH 4256ZE | 0.013 | 0.009 |

1. For further information about the use of these coefficients, refer to Technical Note TN1175, *Power Estimation in ispMACH 4000ZE Devices*.

Switching Test Conditions

Figure 17 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 13.

Figure 17. Output Test Load, LVTTTL and LVCMOS Standards



0213A/ispm4k

Table 13. Test Fixture Required Components

| Test Condition | R ₁ | R ₂ | C _L ¹ | Timing Ref. | V _{CCO} |
|------------------------------|----------------|----------------|-----------------------------|----------------------------------|--------------------|
| LVCMOS I/O, (L -> H, H -> L) | 106Ω | 106Ω | 35pF | LVCMOS 3.3 = 1.5V | LVCMOS 3.3 = 3.0V |
| | | | | LVCMOS 2.5 = $\frac{V_{CCO}}{2}$ | LVCMOS 2.5 = 2.3V |
| | | | | LVCMOS 1.8 = $\frac{V_{CCO}}{2}$ | LVCMOS 1.8 = 1.65V |
| | | | | LVCMOS 1.5 = $\frac{V_{CCO}}{2}$ | LVCMOS 1.5 = 1.4V |
| LVCMOS I/O (Z -> H) | ∞ | 106Ω | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (Z -> L) | 106Ω | ∞ | 35pF | 1.5V | 3.0V |
| LVCMOS I/O (H -> Z) | ∞ | 106Ω | 5pF | V _{OH} - 0.3 | 3.0V |
| LVCMOS I/O (L -> Z) | 106Ω | ∞ | 5pF | V _{OL} + 0.3 | 3.0V |

1. C_L includes test fixtures and probe capacitance.

Signal Descriptions

| Signal Names | Description | |
|---------------------------------------|--|--------|
| TMS | Input – This pin is the IEEE 1149.1 Test Mode Select input, which is used to control the state machine. | |
| TCK | Input – This pin is the IEEE 1149.1 Test Clock input pin, used to clock through the state machine. | |
| TDI | Input – This pin is the IEEE 1149.1 Test Data In pin, used to load data. | |
| TDO | Output – This pin is the IEEE 1149.1 Test Data Out pin used to shift data out. | |
| GOE0/IO, GOE1/IO | These pins are configured to be either Global Output Enable Input or as general I/O pins. | |
| GND | Ground | |
| NC | Not Connected | |
| V _{CC} | The power supply pins for logic core and JTAG port. | |
| CLK0/I, CLK1/I, CLK2/I, CLK3/I | These pins are configured to be either CLK input or as an input. | |
| V _{CC00} , V _{CC01} | The power supply pins for each I/O bank. | |
| yzz | Input/Output ¹ – These are the general purpose I/O used by the logic array. y is GLB reference (alpha) and z is macrocell reference (numeric). z: 0-15. | |
| | ispMACH 4032ZE | y: A-B |
| | ispMACH 4064ZE | y: A-D |
| | ispMACH 4128ZE | y: A-H |
| | ispMACH 4256ZE | y: A-P |

1. In some packages, certain I/Os are only available for use as inputs. See the signal connections table for details.

ORP Reference Table

| | 4032ZE | 4064ZE | | | 4128ZE | | 4256ZE | | |
|------------------------------------|--------|--------|--------------------------|----|--------|----|--------|----|--------------------|
| Number of I/Os | 32 | 32 | 48 | 64 | 64 | 96 | 64 | 96 | 108 |
| Number of GLBs | 2 | 4 | 4 | 4 | 8 | 8 | 16 | 16 | 16 |
| Number of I/Os per GLB | 16 | 8 | Mixture of 9, 10, 14, 15 | 16 | 8 | 12 | 4 | 6 | Mixture of 6, 7, 8 |
| Reference ORP Table (I/Os per GLB) | 16 | 8 | 9, 10, 14, 15 | 16 | 8 | 12 | 4 | 6 | 6, 7, 8 |

ispMACH 4000ZE Power Supply and NC Connections¹

| Signal | 48 TQFP ² | 64 csBGA ^{3,4} | 100 TQFP ² |
|------------------------|----------------------|--|-----------------------|
| VCC | 12, 36 | E4, D5 | 25, 40, 75, 90 |
| VCCO0 VCCO (Bank 0) | 6 | 4032ZE: E3 4064ZE: E3, F4 | 13, 33, 95 |
| VCCO1 VCCO (Bank 1) | 30 | 4032ZE: D6 4064ZE: D6, C6 | 45, 63, 83 |
| GND | 13, 37 | D4, E5 | 1, 26, 51, 76 |
| GND (Bank 0) | 5 | D4, E5 | 7, 18, 32, 96 |
| GND (Bank 1) | 29 | D4, E5 | 46, 57, 68, 82 |
| NC | — | — | — |

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. All bonded grounds are connected to the following two balls, D4 and E5.

ispMACH 4000ZE Power Supply and NC Connections¹ (Cont.)

| Signal | 144 csBGA ³ | 144 TQFP ² |
|------------------------|--|---|
| VCC | H5, H8, E8, E5 | 36, 57, 108, 129 |
| VCCO0 VCCO (Bank 0) | E4, F4, G4, J5, D5 | 3, 19, 34, 47, 136 |
| VCCO1 VCCO (Bank 1) | J8, H9, G9, F9, D8 | 64, 75, 91, 106, 119 |
| GND | F6, G6, G7, F7 | 1, 37, 73, 109 |
| GND (Bank 0) | G5, H4, H6, E6, F5 | 10, 18 ⁴ , 27, 46, 127, 137 |
| GND (Bank 1) | H7, J9, G8, F8, E7 | 55, 65, 82, 90 ⁴ , 99, 118 |
| NC | 4064ZE: E4, B2, B1, D2, D3, E1, H1, H3, H2, L1, G4, M1, K3, M2, M4, L5, H7, L8, M8, L10, K9, M11, H9, L12, L11, J12, J11, H10, D10, F10, D12, B12, F9, A12, C10, B10, A9, B8, E6, B5, A5, C4, B3, A2 4128ZE: D2, D3, H2, M1, K3, M11, J12, J11, D12, A12, C10, A2 | 4128ZE: 17, 20, 38, 45, 72, 89, 92, 110, 117, 144 4256ZE: 18, 90 |

1. All grounds must be electrically connected at the board level. However, for the purposes of I/O current loading, grounds are associated with the bank shown.
2. Pin orientation follows the conventional order from pin 1 marking of the top side view and counter-clockwise.
3. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.
4. For the LC4256ZE, pins 18 and 90 are no connects.

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP

| Pin Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|------------|-------------|----------------|----------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | TDI | TDI |
| 2 | 0 | A5 | A8 |
| 3 | 0 | A6 | A10 |
| 4 | 0 | A7 | A11 |
| 5 | 0 | GND (Bank 0) | GND (Bank 0) |
| 6 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 7 | 0 | A8 | B15 |
| 8 | 0 | A9 | B12 |
| 9 | 0 | A10 | B10 |
| 10 | 0 | A11 | B8 |
| 11 | - | TCK | TCK |
| 12 | - | VCC | VCC |
| 13 | - | GND | GND |
| 14 | 0 | A12 | B6 |
| 15 | 0 | A13 | B4 |
| 16 | 0 | A14 | B2 |
| 17 | 0 | A15 | B0 |
| 18 | 0 | CLK1/I | CLK1/I |
| 19 | 1 | CLK2/I | CLK2/I |
| 20 | 1 | B0 | C0 |
| 21 | 1 | B1 | C1 |
| 22 | 1 | B2 | C2 |
| 23 | 1 | B3 | C4 |
| 24 | 1 | B4 | C6 |
| 25 | - | TMS | TMS |
| 26 | 1 | B5 | C8 |
| 27 | 1 | B6 | C10 |
| 28 | 1 | B7 | C11 |
| 29 | 1 | GND (Bank 1) | GND (Bank 1) |
| 30 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 31 | 1 | B8 | D15 |
| 32 | 1 | B9 | D12 |
| 33 | 1 | B10 | D10 |
| 34 | 1 | B11 | D8 |
| 35 | - | TDO | TDO |
| 36 | - | VCC | VCC |
| 37 | - | GND | GND |
| 38 | 1 | B12 | D6 |
| 39 | 1 | B13 | D4 |
| 40 | 1 | B14 | D2 |
| 41 | 1 | B15/GOE1 | D0/GOE1 |
| 42 | 1 | CLK3/I | CLK3/I |

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 48 TQFP (Cont.)

| Pin Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|------------|-------------|----------------|----------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 43 | 0 | CLK0/I | CLK0/I |
| 44 | 0 | A0/GOE0 | A0/GOE0 |
| 45 | 0 | A1 | A1 |
| 46 | 0 | A2 | A2 |
| 47 | 0 | A3 | A4 |
| 48 | 0 | A4 | A6 |

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA

| Ball Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|-------------|-------------|----------------|----------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| B2 | - | TDI | TDI |
| B1 | 0 | A5 | A8 |
| C2 | 0 | A6 | A10 |
| C1 | 0 | A7 | A11 |
| GND* | 0 | GND (Bank 0) | GND (Bank 0) |
| C3 | 0 | NC | A12 |
| E3 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| D1 | 0 | A8 | B15 |
| D2 | 0 | NC | B14 |
| E1 | 0 | A9 | B13 |
| D3 | 0 | A10 | B12 |
| F1 | 0 | A11 | B11 |
| E2 | 0 | NC | B10 |
| G1 | 0 | NC | B9 |
| F2 | 0 | NC | B8 |
| H1 | - | TCK | TCK |
| E4 | - | VCC | VCC |
| GND* | - | GND | GND |
| G2 | 0 | A12 | B6 |
| H2 | 0 | NC | B5 |
| H3 | 0 | A13 | B4 |
| GND* | 0 | NC | GND (Bank 0) |
| F4 | 0 | NC | VCCO (Bank 0) |
| G3 | 0 | A14 | B3 |
| F3 | 0 | NC | B2 |
| H4 | 0 | A15 | B0 |
| G4 | 0 | CLK1/I | CLK1/I |
| H5 | 1 | CLK2/I | CLK2/I |
| F5 | 1 | B0 | C0 |
| G5 | 1 | B1 | C1 |
| G6 | 1 | B2 | C2 |
| H6 | 1 | B3 | C4 |
| F6 | 1 | B4 | C5 |
| H7 | 1 | NC | C6 |
| H8 | - | TMS | TMS |
| G7 | 1 | B5 | C8 |
| F7 | 1 | B6 | C10 |
| G8 | 1 | B7 | C11 |
| GND* | 1 | GND (Bank 0) | GND (Bank 1) |
| F8 | 1 | NC | C12 |
| D6 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| E8 | 1 | B8 | D15 |

ispMACH 4032ZE and 4064ZE Logic Signal Connections: 64 csBGA (Cont.)

| Ball Number | Bank Number | ispMACH 4032ZE | ispMACH 4064ZE |
|-------------|-------------|----------------|----------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| E7 | 1 | NC | D14 |
| E6 | 1 | B9 | D13 |
| D7 | 1 | B10 | D12 |
| D8 | 1 | NC | D11 |
| C5 | 1 | NC | D10 |
| C7 | 1 | B11 | D9 |
| C8 | 1 | NC | D8 |
| B8 | - | TDO | TDO |
| D5 | - | VCC | VCC |
| GND* | - | GND | GND |
| A8 | 1 | B12 | D7 |
| A7 | 1 | NC | D6 |
| B7 | 1 | NC | D5 |
| A6 | 1 | B13 | D4 |
| GND* | 1 | NC | GND (Bank 1) |
| C6 | 1 | NC | VCCO (Bank 1) |
| B6 | 1 | B14 | D3 |
| A5 | 1 | NC | D2 |
| B5 | 1 | B15/GOE1 | D0/GOE1 |
| A4 | 1 | CLK3/I | CLK3/I |
| C4 | 0 | CLK0/I | CLK0/I |
| B4 | 0 | A0/GOE0 | A0/GOE0 |
| B3 | 0 | A1 | A1 |
| A3 | 0 | A2 | A2 |
| A2 | 0 | A3 | A4 |
| A1 | 0 | A4 | A6 |

* All bonded grounds are connected to the following two balls, D4 and E5.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
100 TQFP**

| Pin Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|------------|-------------|---------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | GND | GND | GND |
| 2 | - | TDI | TDI | TDI |
| 3 | 0 | A8 | B0 | C12 |
| 4 | 0 | A9 | B2 | C10 |
| 5 | 0 | A10 | B4 | C6 |
| 6 | 0 | A11 | B6 | C2 |
| 7 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 8 | 0 | A12 | B8 | D12 |
| 9 | 0 | A13 | B10 | D10 |
| 10 | 0 | A14 | B12 | D6 |
| 11 | 0 | A15 | B13 | D4 |
| 12* | 0 | I | I | I |
| 13 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 14 | 0 | B15 | C14 | E4 |
| 15 | 0 | B14 | C12 | E6 |
| 16 | 0 | B13 | C10 | E10 |
| 17 | 0 | B12 | C8 | E12 |
| 18 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 19 | 0 | B11 | C6 | F2 |
| 20 | 0 | B10 | C5 | F6 |
| 21 | 0 | B9 | C4 | F10 |
| 22 | 0 | B8 | C2 | F12 |
| 23* | 0 | I | I | I |
| 24 | - | TCK | TCK | TCK |
| 25 | - | VCC | VCC | VCC |
| 26 | - | GND | GND | GND |
| 27* | 0 | I | I | I |
| 28 | 0 | B7 | D13 | G12 |
| 29 | 0 | B6 | D12 | G10 |
| 30 | 0 | B5 | D10 | G6 |
| 31 | 0 | B4 | D8 | G2 |
| 32 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 33 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 34 | 0 | B3 | D6 | H12 |
| 35 | 0 | B2 | D4 | H10 |
| 36 | 0 | B1 | D2 | H6 |
| 37 | 0 | B0 | D0 | H2 |
| 38 | 0 | CLK1/I | CLK1/I | CLK1/I |
| 39 | 1 | CLK2/I | CLK2/I | CLK2/I |
| 40 | - | VCC | VCC | VCC |
| 41 | 1 | C0 | E0 | I2 |

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
100 TQFP (Cont.)**

| Pin Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|------------|-------------|---------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| 42 | 1 | C1 | E2 | I6 |
| 43 | 1 | C2 | E4 | I10 |
| 44 | 1 | C3 | E6 | I12 |
| 45 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| 46 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| 47 | 1 | C4 | E8 | J2 |
| 48 | 1 | C5 | E10 | J6 |
| 49 | 1 | C6 | E12 | J10 |
| 50 | 1 | C7 | E14 | J12 |
| 51 | - | GND | GND | GND |
| 52 | - | TMS | TMS | TMS |
| 53 | 1 | C8 | F0 | K12 |
| 54 | 1 | C9 | F2 | K10 |
| 55 | 1 | C10 | F4 | K6 |
| 56 | 1 | C11 | F6 | K2 |
| 57 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| 58 | 1 | C12 | F8 | L12 |
| 59 | 1 | C13 | F10 | L10 |
| 60 | 1 | C14 | F12 | L6 |
| 61 | 1 | C15 | F13 | L4 |
| 62* | 1 | I | I | I |
| 63 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| 64 | 1 | D15 | G14 | M4 |
| 65 | 1 | D14 | G12 | M6 |
| 66 | 1 | D13 | G10 | M10 |
| 67 | 1 | D12 | G8 | M12 |
| 68 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| 69 | 1 | D11 | G6 | N2 |
| 70 | 1 | D10 | G5 | N6 |
| 71 | 1 | D9 | G4 | N10 |
| 72 | 1 | D8 | G2 | N12 |
| 73* | 1 | I | I | I |
| 74 | - | TDO | TDO | TDO |
| 75 | - | VCC | VCC | VCC |
| 76 | - | GND | GND | GND |
| 77* | 1 | I | I | I |
| 78 | 1 | D7 | H13 | O12 |
| 79 | 1 | D6 | H12 | O10 |
| 80 | 1 | D5 | H10 | O6 |
| 81 | 1 | D4 | H8 | O2 |
| 82 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
100 TQFP (Cont.)**

| Pin Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|------------|-------------|---------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| 83 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| 84 | 1 | D3 | H6 | P12 |
| 85 | 1 | D2 | H4 | P10 |
| 86 | 1 | D1 | H2 | P6 |
| 87 | 1 | D0/GOE1 | H0/GOE1 | P2/GOE1 |
| 88 | 1 | CLK3/I | CLK3/I | CLK3/I |
| 89 | 0 | CLK0/I | CLK0/I | CLK0/I |
| 90 | - | VCC | VCC | VCC |
| 91 | 0 | A0/GOE0 | A0/GOE0 | A2/GOE0 |
| 92 | 0 | A1 | A2 | A6 |
| 93 | 0 | A2 | A4 | A10 |
| 94 | 0 | A3 | A6 | A12 |
| 95 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| 96 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| 97 | 0 | A4 | A8 | B2 |
| 98 | 0 | A5 | A10 | B6 |
| 99 | 0 | A6 | A12 | B10 |
| 100 | 0 | A7 | A14 | B12 |

* This pin is input only.

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
144 csBGA**

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|-------------|-------------|---------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| F6 | - | GND | GND | GND |
| A1 | - | TDI | TDI | TDI |
| E4 | 0 | NC Ball | VCCO (Bank 0) | VCCO (Bank 0) |
| B2 | 0 | NC Ball | B0 | C12 |
| B1 | 0 | NC Ball | B1 | C10 |
| C3 | 0 | A8 | B2 | C8 |
| C2 | 0 | A9 | B4 | C6 |
| C1 | 0 | A10 | B5 | C4 |
| D1 | 0 | A11 | B6 | C2 |
| G5 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| D2 | 0 | NC Ball | NC Ball | D14 |
| D3 | 0 | NC Ball | NC Ball | D12 |
| E1 | 0 | NC Ball | B8 | D10 |
| E2 | 0 | A12 | B9 | D8 |
| F2 | 0 | A13 | B10 | D6 |
| D4 | 0 | A14 | B12 | D4 |
| F1 | 0 | A15 | B13 | D2 |
| F3* | 0 | I | B14 | D0 |
| F4 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| G1 | 0 | B15 | C14 | E0 |
| E3 | 0 | B14 | C13 | E2 |
| G2 | 0 | B13 | C12 | E4 |
| G3 | 0 | B12 | C10 | E6 |
| H1 | 0 | NC Ball | C9 | E8 |
| H3 | 0 | NC Ball | C8 | E10 |
| H2 | 0 | NC Ball | NC Ball | E12 |
| H4 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| J1 | 0 | B11 | C6 | F2 |
| J3 | 0 | B10 | C5 | F4 |
| J2 | 0 | B9 | C4 | F6 |
| K1 | 0 | B8 | C2 | F8 |
| K2* | 0 | I | C1 | F10 |
| L1 | 0 | NC Ball | C0 | F12 |
| G4 | 0 | NC Ball | VCCO (Bank 0) | VCCO (Bank 0) |
| L2 | - | TCK | TCK | TCK |
| H5 | - | VCC | VCC | VCC |
| G6 | - | GND | GND | GND |
| M1 | 0 | NC Ball | NC Ball | G14 |
| K3 | 0 | NC Ball | NC Ball | G12 |
| M2 | 0 | NC Ball | D14 | G10 |
| L3* | 0 | I | D13 | G8 |

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
144 csBGA (Cont.)**

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|-------------|-------------|---------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| J4 | 0 | B7 | D12 | G6 |
| K4 | 0 | B6 | D10 | G4 |
| M3 | 0 | B5 | D9 | G2 |
| L4 | 0 | B4 | D8 | G0 |
| H6 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| J5 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| M4 | 0 | NC Ball | D6 | H12 |
| L5 | 0 | NC Ball | D5 | H10 |
| K5 | 0 | B3 | D4 | H8 |
| J6 | 0 | B2 | D2 | H6 |
| M5 | 0 | B1 | D1 | H4 |
| K6 | 0 | B0 | D0 | H2 |
| L6 | 0 | CLK1/I | CLK1/I | CLK1/I |
| H7 | 1 | NC Ball | GND (Bank 1) | GND (Bank 1) |
| M6 | 1 | CLK2/I | CLK2/I | CLK2/I |
| H8 | - | VCC | VCC | VCC |
| K7 | 1 | C0 | E0 | I2 |
| M7 | 1 | C1 | E1 | I4 |
| L7 | 1 | C2 | E2 | I6 |
| J7 | 1 | C3 | E4 | I8 |
| L8 | 1 | NC Ball | E5 | I10 |
| M8 | 1 | NC Ball | E6 | I12 |
| J8 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| J9 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| M9 | 1 | C4 | E8 | J2 |
| L9 | 1 | C5 | E9 | J4 |
| K8 | 1 | C6 | E10 | J6 |
| M10 | 1 | C7 | E12 | J8 |
| L10 | 1 | NC Ball | E13 | J10 |
| K9 | 1 | NC Ball | E14 | J12 |
| M11 | 1 | NC Ball | NC Ball | J14 |
| G7 | - | GND | GND | GND |
| M12 | - | TMS | TMS | TMS |
| H9 | 1 | NC Ball | VCCO (Bank 1) | VCCO (Bank 1) |
| L12 | 1 | NC Ball | F0 | K12 |
| L11 | 1 | NC Ball | F1 | K10 |
| K10 | 1 | C8 | F2 | K8 |
| K12 | 1 | C9 | F4 | K6 |
| J10 | 1 | C10 | F5 | K4 |
| K11 | 1 | C11 | F6 | K2 |
| G8 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
144 csBGA (Cont.)**

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|-------------|-------------|---------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| J12 | 1 | NC Ball | NC Ball | L14 |
| J11 | 1 | NC Ball | NC Ball | L12 |
| H10 | 1 | NC Ball | F8 | L10 |
| H12 | 1 | C12 | F9 | L8 |
| G11 | 1 | C13 | F10 | L6 |
| H11 | 1 | C14 | F12 | L4 |
| G12 | 1 | C15 | F13 | L2 |
| G10* | 1 | I | F14 | L0 |
| G9 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| F12 | 1 | D15 | G14 | M0 |
| F11 | 1 | D14 | G13 | M2 |
| E11 | 1 | D13 | G12 | M4 |
| E12 | 1 | D12 | G10 | M6 |
| D10 | 1 | NC Ball | G9 | M8 |
| F10 | 1 | NC Ball | G8 | M10 |
| D12 | 1 | NC Ball | NC Ball | M12 |
| F8 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| E10 | 1 | D11 | G6 | N2 |
| D11 | 1 | D10 | G5 | N4 |
| E9 | 1 | D9 | G4 | N6 |
| C12 | 1 | D8 | G2 | N8 |
| C11* | 1 | I | G1 | N10 |
| B12 | 1 | NC Ball | G0 | N12 |
| F9 | 1 | NC Ball | VCCO (Bank 1) | VCCO (Bank 1) |
| B11 | - | TDO | TDO | TDO |
| E8 | - | VCC | VCC | VCC |
| F7 | - | GND | GND | GND |
| A12 | 1 | NC Ball | NC Ball | O14 |
| C10 | 1 | NC Ball | NC Ball | O12 |
| B10 | 1 | NC Ball | H14 | O10 |
| A11* | 1 | I | H13 | O8 |
| D9 | 1 | D7 | H12 | O6 |
| B9 | 1 | D6 | H10 | O4 |
| C9 | 1 | D5 | H9 | O2 |
| A10 | 1 | D4 | H8 | O0 |
| E7 | 1 | GND (Bank 1) | GND (Bank 1) | GND (Bank 1) |
| D8 | 1 | VCCO (Bank 1) | VCCO (Bank 1) | VCCO (Bank 1) |
| A9 | 1 | NC Ball | H6 | P12 |
| B8 | 1 | NC Ball | H5 | P10 |
| C8 | 1 | D3 | H4 | P8 |
| A8 | 1 | D2 | H2 | P6 |

**ispMACH 4064ZE, 4128ZE and 4256ZE Logic Signal Connections:
144 csBGA (Cont.)**

| Ball Number | Bank Number | LC4064ZE | LC4128ZE | LC4256ZE |
|-------------|-------------|---------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad | GLB/MC/Pad |
| D7 | 1 | D1 | H1 | P4 |
| B7 | 1 | D0/GOE1 | H0/GOE1 | P2/GOE1 |
| C7 | 1 | CLK3/I | CLK3/I | CLK3/I |
| E6 | 0 | NC Ball | GND (Bank 0) | GND (Bank 0) |
| A7 | 0 | CLK0/I | CLK0/I | CLK0/I |
| E5 | - | VCC | VCC | VCC |
| D6 | 0 | A0/GOE0 | A0/GOE0 | A2/GOE0 |
| B6 | 0 | A1 | A1 | A4 |
| A6 | 0 | A2 | A2 | A6 |
| C6 | 0 | A3 | A4 | A8 |
| B5 | 0 | NC Ball | A5 | A10 |
| A5 | 0 | NC Ball | A6 | A12 |
| D5 | 0 | VCCO (Bank 0) | VCCO (Bank 0) | VCCO (Bank 0) |
| F5 | 0 | GND (Bank 0) | GND (Bank 0) | GND (Bank 0) |
| A4 | 0 | A4 | A8 | B2 |
| B4 | 0 | A5 | A9 | B4 |
| C5 | 0 | A6 | A10 | B6 |
| A3 | 0 | A7 | A12 | B8 |
| C4 | 0 | NC Ball | A13 | B10 |
| B3 | 0 | NC Ball | A14 | B12 |
| A2 | 0 | NC Ball | NC Ball | B14 |

* This pin is input only for the LC4064ZE.

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP

| Pin Number | Bank Number | LC4128ZE | LC4256ZE |
|------------|-------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 1 | - | GND | GND |
| 2 | - | TDI | TDI |
| 3 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 4 | 0 | B0 | C12 |
| 5 | 0 | B1 | C10 |
| 6 | 0 | B2 | C8 |
| 7 | 0 | B4 | C6 |
| 8 | 0 | B5 | C4 |
| 9 | 0 | B6 | C2 |
| 10 | 0 | GND (Bank 0) | GND (Bank 0) |
| 11 | 0 | B8 | D14 |
| 12 | 0 | B9 | D12 |
| 13 | 0 | B10 | D10 |
| 14 | 0 | B12 | D8 |
| 15 | 0 | B13 | D6 |
| 16 | 0 | B14 | D4 |
| 17* | 0 | NC | I |
| 18 | 0 | GND (Bank 0) | NC |
| 19 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 20* | 0 | NC | I |
| 21 | 0 | C14 | E2 |
| 22 | 0 | C13 | E4 |
| 23 | 0 | C12 | E6 |
| 24 | 0 | C10 | E8 |
| 25 | 0 | C9 | E10 |
| 26 | 0 | C8 | E12 |
| 27 | 0 | GND (Bank 0) | GND (Bank 0) |
| 28 | 0 | C6 | F2 |
| 29 | 0 | C5 | F4 |
| 30 | 0 | C4 | F6 |
| 31 | 0 | C2 | F8 |
| 32 | 0 | C1 | F10 |
| 33 | 0 | C0 | F12 |
| 34 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 35 | - | TCK | TCK |
| 36 | - | VCC | VCC |
| 37 | - | GND | GND |
| 38* | 0 | NC | I |
| 39 | 0 | D14 | G12 |
| 40 | 0 | D13 | G10 |
| 41 | 0 | D12 | G8 |
| 42 | 0 | D10 | G6 |

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | Bank Number | LC4128ZE | LC4256ZE |
|------------|-------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 43 | 0 | D9 | G4 |
| 44 | 0 | D8 | G2 |
| 45* | 0 | NC | I |
| 46 | 0 | GND (Bank 0) | GND (Bank 0) |
| 47 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 48 | 0 | D6 | H12 |
| 49 | 0 | D5 | H10 |
| 50 | 0 | D4 | H8 |
| 51 | 0 | D2 | H6 |
| 52 | 0 | D1 | H4 |
| 53 | 0 | D0 | H2 |
| 54 | 0 | CLK1/I | CLK1/I |
| 55 | 1 | GND (Bank 1) | GND (Bank 1) |
| 56 | 1 | CLK2/I | CLK2/I |
| 57 | - | VCC | VCC |
| 58 | 1 | E0 | I2 |
| 59 | 1 | E1 | I4 |
| 60 | 1 | E2 | I6 |
| 61 | 1 | E4 | I8 |
| 62 | 1 | E5 | I10 |
| 63 | 1 | E6 | I12 |
| 64 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 65 | 1 | GND (Bank 1) | GND (Bank 1) |
| 66 | 1 | E8 | J2 |
| 67 | 1 | E9 | J4 |
| 68 | 1 | E10 | J6 |
| 69 | 1 | E12 | J8 |
| 70 | 1 | E13 | J10 |
| 71 | 1 | E14 | J12 |
| 72* | 1 | NC | I |
| 73 | - | GND | GND |
| 74 | - | TMS | TMS |
| 75 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 76 | 1 | F0 | K12 |
| 77 | 1 | F1 | K10 |
| 78 | 1 | F2 | K8 |
| 79 | 1 | F4 | K6 |
| 80 | 1 | F5 | K4 |
| 81 | 1 | F6 | K2 |
| 82 | 1 | GND (Bank 1) | GND (Bank 1) |
| 83 | 1 | F8 | L14 |
| 84 | 1 | F9 | L12 |
| 85 | 1 | F10 | L10 |

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

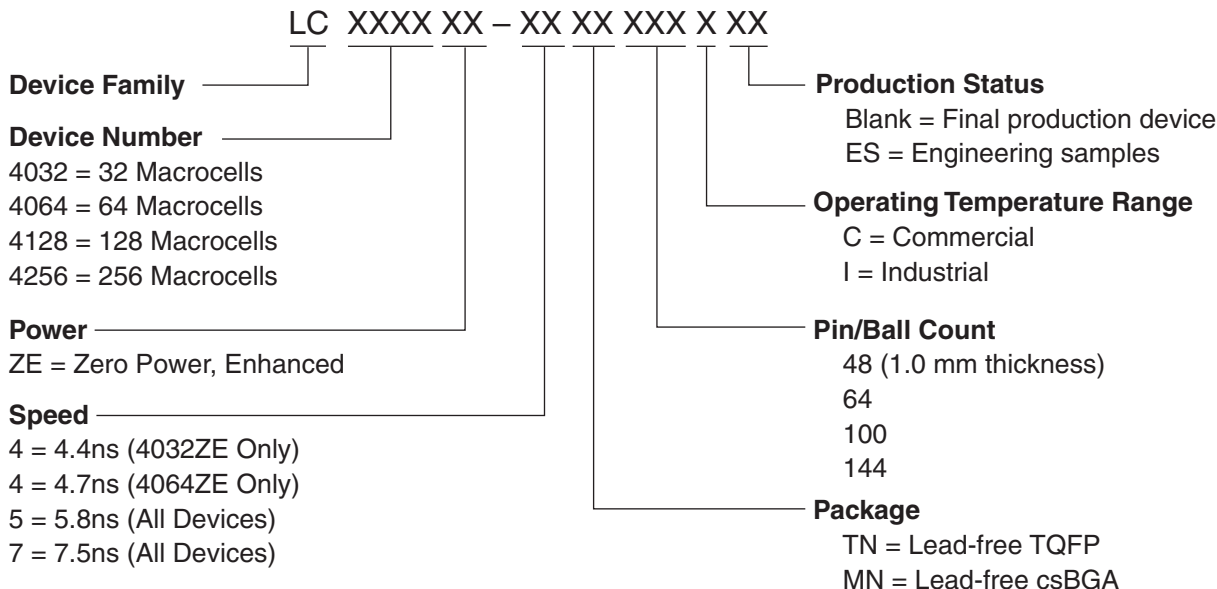
| Pin Number | Bank Number | LC4128ZE | LC4256ZE |
|------------|-------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 86 | 1 | F12 | L8 |
| 87 | 1 | F13 | L6 |
| 88 | 1 | F14 | L4 |
| 89* | 1 | NC | I |
| 90 | 1 | GND (Bank 1) | NC |
| 91 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 92* | 1 | NC | I |
| 93 | 1 | G14 | M2 |
| 94 | 1 | G13 | M4 |
| 95 | 1 | G12 | M6 |
| 96 | 1 | G10 | M8 |
| 97 | 1 | G9 | M10 |
| 98 | 1 | G8 | M12 |
| 99 | 1 | GND (Bank 1) | GND (Bank 1) |
| 100 | 1 | G6 | N2 |
| 101 | 1 | G5 | N4 |
| 102 | 1 | G4 | N6 |
| 103 | 1 | G2 | N8 |
| 104 | 1 | G1 | N10 |
| 105 | 1 | G0 | N12 |
| 106 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 107 | - | TDO | TDO |
| 108 | - | VCC | VCC |
| 109 | - | GND | GND |
| 110* | 1 | NC | I |
| 111 | 1 | H14 | O12 |
| 112 | 1 | H13 | O10 |
| 113 | 1 | H12 | O8 |
| 114 | 1 | H10 | O6 |
| 115 | 1 | H9 | O4 |
| 116 | 1 | H8 | O2 |
| 117* | 1 | NC | I |
| 118 | 1 | GND (Bank 1) | GND (Bank 1) |
| 119 | 1 | VCCO (Bank 1) | VCCO (Bank 1) |
| 120 | 1 | H6 | P12 |
| 121 | 1 | H5 | P10 |
| 122 | 1 | H4 | P8 |
| 123 | 1 | H2 | P6 |
| 124 | 1 | H1 | P4 |
| 125 | 1 | H0/GOE1 | P2/GOE1 |
| 126 | 1 | CLK3/I | CLK3/I |
| 127 | 0 | GND (Bank 0) | GND (Bank 0) |
| 128 | 0 | CLK0/I | CLK0/I |

ispMACH 4128ZE and 4256ZE Logic Signal Connections: 144 TQFP (Cont.)

| Pin Number | Bank Number | LC4128ZE | LC4256ZE |
|------------|-------------|---------------|---------------|
| | | GLB/MC/Pad | GLB/MC/Pad |
| 129 | - | VCC | VCC |
| 130 | 0 | A0/GOE0 | A2/GOE0 |
| 131 | 0 | A1 | A4 |
| 132 | 0 | A2 | A6 |
| 133 | 0 | A4 | A8 |
| 134 | 0 | A5 | A10 |
| 135 | 0 | A6 | A12 |
| 136 | 0 | VCCO (Bank 0) | VCCO (Bank 0) |
| 137 | 0 | GND (Bank 0) | GND (Bank 0) |
| 138 | 0 | A8 | B2 |
| 139 | 0 | A9 | B4 |
| 140 | 0 | A10 | B6 |
| 141 | 0 | A12 | B8 |
| 142 | 0 | A13 | B10 |
| 143 | 0 | A14 | B12 |
| 144* | 0 | NC | I |

* This pin is input only for the LC4256ZE.

Part Number Description



ispMACH 4000ZE Family Speed Grade Offering

| | -4 | -5 | | -7 | |
|----------------|-----|-----|-----|-----|-----|
| | Com | Com | Ind | Com | Ind |
| ispMACH 4032ZE | ✓ | ✓ | ✓ | ✓ | ✓ |
| ispMACH 4064ZE | ✓ | ✓ | ✓ | ✓ | ✓ |
| ispMACH 4128ZE | | ✓ | | ✓ | ✓ |
| ispMACH 4256ZE | | ✓ | | ✓ | ✓ |

Ordering Information

Note: ispMACH 4000ZE devices are dual marked except for the slowest commercial speed grade. For example, the commercial speed grade LC4128ZE-5TN100C is also marked with the industrial grade -7I. The commercial grade is always one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade devices are marked as commercial grade only. The markings appear as follows:

Figure 18. Mark Format for 100 TQFP and 144 TQFP Packages

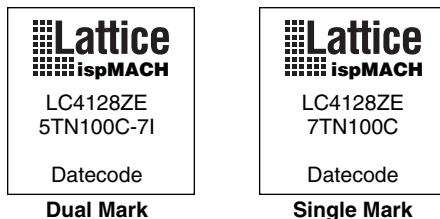
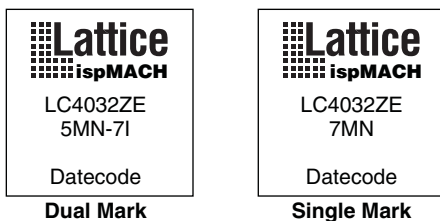


Figure 19. Mark Format for 48 TQFP, 64 csBGA and 144 csBGA Packages



Lead-Free Packaging

Commercial Devices

| Device | Part Number | Macrocells | Voltage | t _{PD} | Package | Pin/Ball Count | I/O | Grade |
|------------------|------------------|------------|---------|-----------------|-----------------|----------------|-----|-------|
| LC4032ZE | LC4032ZE-4TN48C | 32 | 1.8 | 4.4 | Lead-Free TQFP | 48 | 32 | C |
| | LC4032ZE-5TN48C | 32 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | C |
| | LC4032ZE-7TN48C | 32 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | C |
| | LC4032ZE-4MN64C | 32 | 1.8 | 4.4 | Lead-Free csBGA | 64 | 32 | C |
| | LC4032ZE-5MN64C | 32 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 32 | C |
| | LC4032ZE-7MN64C | 32 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 32 | C |
| LC4064ZE | LC4064ZE-4TN48C | 64 | 1.8 | 4.7 | Lead-Free TQFP | 48 | 32 | C |
| | LC4064ZE-5TN48C | 64 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | C |
| | LC4064ZE-7TN48C | 64 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | C |
| | LC4064ZE-4TN100C | 64 | 1.8 | 4.7 | Lead-Free TQFP | 100 | 64 | C |
| | LC4064ZE-5TN100C | 64 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | C |
| | LC4064ZE-7TN100C | 64 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | C |
| | LC4064ZE-4MN64C | 64 | 1.8 | 4.7 | Lead-Free csBGA | 64 | 48 | C |
| | LC4064ZE-5MN64C | 64 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 48 | C |
| | LC4064ZE-7MN64C | 64 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 48 | C |
| | LC4064ZE-4MN144C | 64 | 1.8 | 4.7 | Lead-Free csBGA | 144 | 64 | C |
| | LC4064ZE-5MN144C | 64 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 64 | C |
| LC4064ZE-7MN144C | 64 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 64 | C | |
| LC4128ZE | LC4128ZE-5TN100C | 128 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | C |
| | LC4128ZE-7TN100C | 128 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | C |
| | LC4128ZE-5TN144C | 128 | 1.8 | 5.8 | Lead-Free TQFP | 144 | 96 | C |
| | LC4128ZE-7TN144C | 128 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | C |
| | LC4128ZE-5MN144C | 128 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 96 | C |
| | LC4128ZE-7MN144C | 128 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 96 | C |
| LC4256ZE | LC4256ZE-5TN100C | 256 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | C |
| | LC4256ZE-7TN100C | 256 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | C |
| | LC4256ZE-5TN144C | 256 | 1.8 | 5.8 | Lead-Free TQFP | 144 | 96 | C |
| | LC4256ZE-7TN144C | 256 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | C |
| | LC4256ZE-5MN144C | 256 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 108 | C |
| | LC4256ZE-7MN144C | 256 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 108 | C |

Industrial

| Device | Part Number | Macrocells | Voltage | t _{PD} | Package | Pin/Ball Count | I/O | Grade |
|----------|------------------|------------|---------|-----------------|-----------------|----------------|-----|-------|
| LC4032ZE | LC4032ZE-5TN48I | 32 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032ZE-7TN48I | 32 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4032ZE-5MN64I | 32 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 32 | I |
| | LC4032ZE-7MN64I | 32 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 32 | I |
| LC4064ZE | LC4064ZE-5TN48I | 64 | 1.8 | 5.8 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064ZE-7TN48I | 64 | 1.8 | 7.5 | Lead-Free TQFP | 48 | 32 | I |
| | LC4064ZE-5TN100I | 64 | 1.8 | 5.8 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064ZE-7TN100I | 64 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4064ZE-5MN64I | 64 | 1.8 | 5.8 | Lead-Free csBGA | 64 | 48 | I |
| | LC4064ZE-7MN64I | 64 | 1.8 | 7.5 | Lead-Free csBGA | 64 | 48 | I |
| | LC4064ZE-5MN144I | 64 | 1.8 | 5.8 | Lead-Free csBGA | 144 | 64 | I |
| | LC4064ZE-7MN144I | 64 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 64 | I |
| LC4128ZE | LC4128ZE-7TN100I | 128 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4128ZE-7TN144I | 128 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | I |
| | LC4128ZE-7MN144I | 128 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 96 | I |
| LC4256ZE | LC4256ZE-7TN100I | 256 | 1.8 | 7.5 | Lead-Free TQFP | 100 | 64 | I |
| | LC4256ZE-7TN144I | 256 | 1.8 | 7.5 | Lead-Free TQFP | 144 | 96 | I |
| | LC4256ZE-7MN144I | 256 | 1.8 | 7.5 | Lead-Free csBGA | 144 | 108 | I |

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with the ispMACH 4000ZE family:

- TN1168 – *ispMACH 4000ZE Timing Model Design and Usage Guidelines*
- TN1174 – *Advanced Features of the ispMACH 4000ZE*
- TN1175 – *Power Estimation and Management for ispMACH 4000ZE Devices*

Technical Support Assistance

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Revision History

| Date | Version | Change Summary |
|-------------|---------|--|
| April 2008 | 01.0 | Initial release. |
| July 2008 | 01.1 | Updated Features bullets. |
| | | Updated typical Hysteresis voltage. |
| | | Updated Power Guard for Dedicated Inputs section. |
| | | Updated DC Electrical Characteristics table. |
| | | Updated Supply Current table. |
| | | Updated I/O DC Electrical Characteristics table and note 2. |
| | | Updated ispMACH 4000ZE Timing Model. |
| | | Added new parameters for the Internal Oscillator. |
| | | Updated ORP Reference table. |
| | | Updated Power Supply and NC Connections table. |
| | | Updated 100 TQFP Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Updated 144 csBGA Logic Signal Connections table with LC4128ZE and 4256ZE. |
| | | Added 144 TQFP Logic Signal Connections table. |
| August 2008 | 01.2 | Data sheet status changed from advance to final. |
| | | Updated Supply Current table. |
| | | Updated External Switching Characteristics. |
| | | Updated Internal Timing Parameters. |
| | | Updated Power Consumption graph and Power Estimation Coefficients table. |
| | | Updated Ordering Information mark format example. |