

MACO™

Masked Array for Cost Reduction

MACO Overview

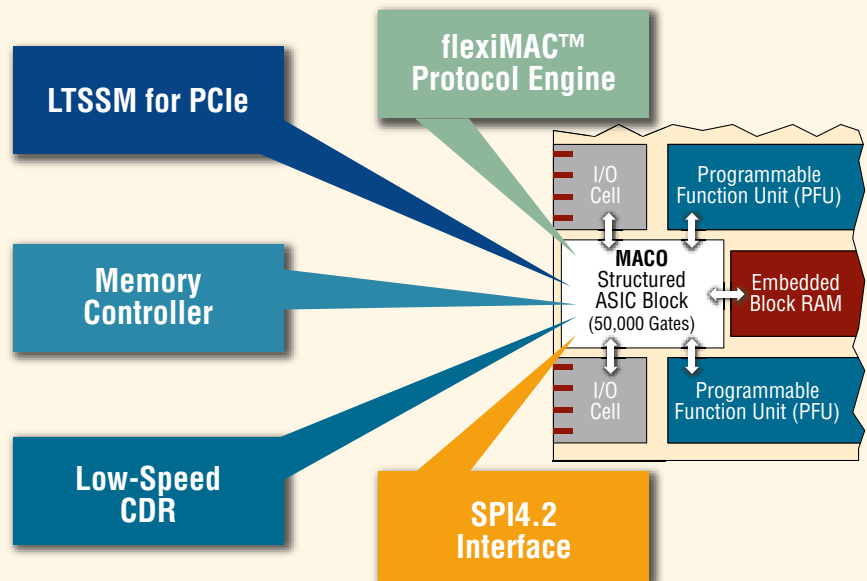
Think of MACO blocks as structured ASICs embedded in an FPGA fabric. MACO technology is based on a unique library of cells created with Fujitsu's 90nm CMOS process technology and optimized for speed, power and area. Each MACO block is equivalent to approximately 50,000 ASIC gates. Lattice provides a set of pre-engineered standard-compliant MACO functions on each LatticeSCM™ device, reducing your design effort and time-to-market. Once you purchase a LatticeSCM device, no additional IP license fees are required.

A MACO core occupies only 10% of the area of an equivalent FPGA implementation. With multiple MACO blocks per device, this results in a substantial cost savings to the designer, both by lowering the development cost and saving significant silicon area. Because MACO is a cell-based technology, it typically offers twice the performance while consuming less than half the power of a standard implementation using FPGA gates. All MACO blocks are easily configured using IPexpress in Lattice's ispLEVER® design tool.

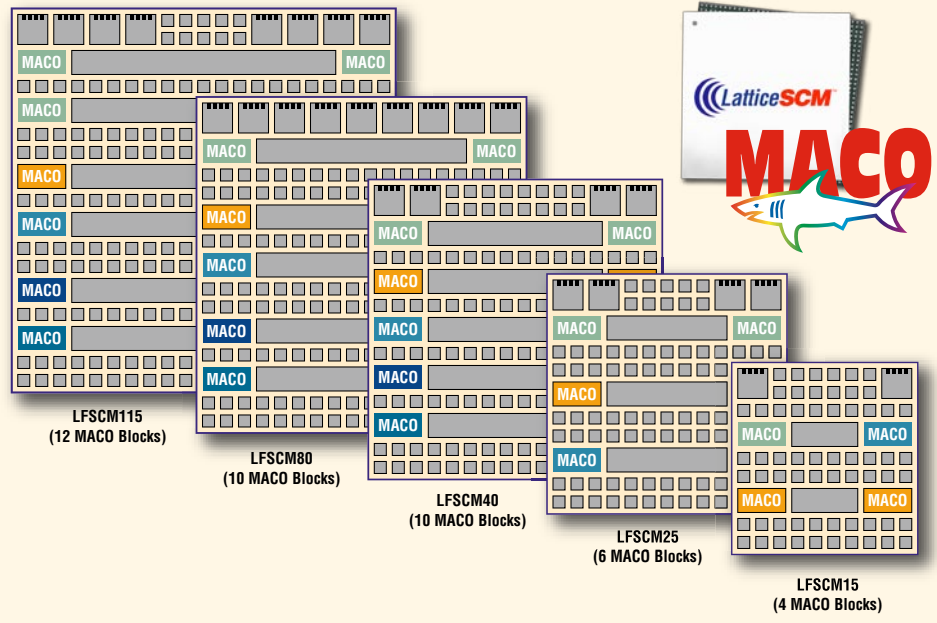
MACO for System Level Connectivity

MACO blocks are an integral part of the LatticeSCM connectivity solution. In applications such as Ethernet and PCIe, the MACO blocks function seamlessly with the embedded PCS layer and SERDES in the LatticeSCM device to provide the industry's most integrated FPGA solution for modern serial protocols. Additional MACO blocks handle standards driven interfaces to ASSPs such as network processors, traffic managers, and memory devices through SPI4.2, DDR I/II, QDR II and RLLDRAM

5 MACO Blocks Available Today!

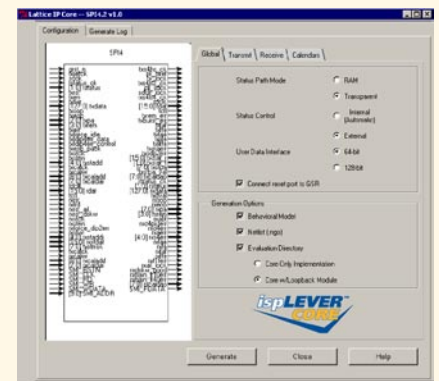


LatticeSCM Devices are Loaded with up to 12 MACO Blocks!



IPexpress Tool

Lattice's IPexpress™ tool greatly simplifies the MACO design process. The IPexpress design flow enables users to fully parameterize MACO blocks in real-time. Designers can then instantiate the user-configured IP and complete the design process, including full timing simulation and bitstream generation.



More of the Best

www.latticesemi.com



MACO Blocks in Detail

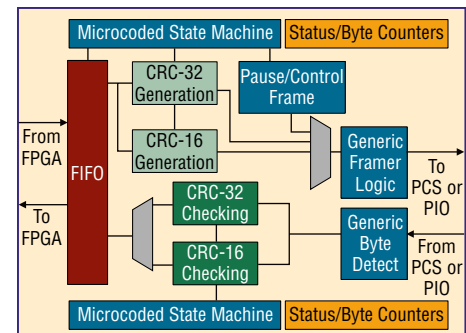
flexiMAC Protocol Engine – Configurable at design time for:

PCI Express

- Appends/Strips Sequence Number and LCRC to/from TLP
- Stores Transaction Layer Protocols (TLPs) for DLL Retry
- Provides Data Link Layer Packets (DLLPs)
- Data Link Control & Management State Machine
- Data Integrity Checks (LCRC)
- Collapses Multiple DLLPs

Ethernet

- 1GbE or 10GbE MAC Function
- Flexible Packet Framing and Parser
- Seamlessly Connects with SERDES/PCS
- Provides Multi-Protocol Functionality
- Complete Layer 1/2 Solution



Memory Controller – Configurable at design time for:

DDR II (267MHz/ 534Mbps)

- Data Path Widths of 8-72 Bits
- Programmable Address Widths
- Burst Length of 4 or 8
- 2 Chip Selects
- Programmable Timing Parameters
- True and Complementary DQS

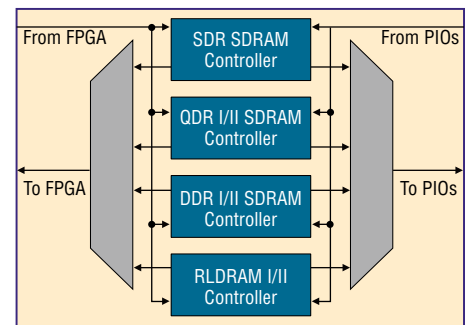
- Supports Cascading
- Cyclic Bank Access
- Programmable Data Path Widths
- Supports Data Mask

RLDRAM II (400MHz/800Mbps)

- CIO and SIO Devices
- Burst Lengths of 2, 4 or 8

QDR I/II (300MHz/600Mbps)

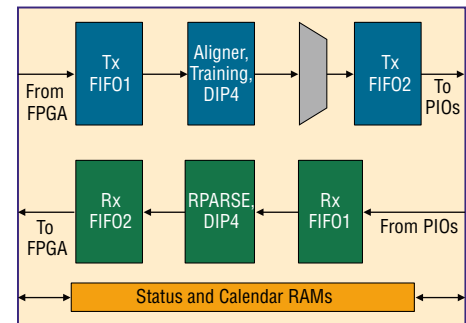
- Programmable Data and Address Widths
- Programmable Burst Sizes
- Supports Read and Write Interleaving



SPI4.2

- Fully Compliant With OIF-SPI4-02.0 Specification
- Up to 256 Logical Ports
- Static and Dynamic Alignment Modes
- Up to 1 Gbps Dynamic Phase Alignment
- Up to 700Mbps Static Alignment

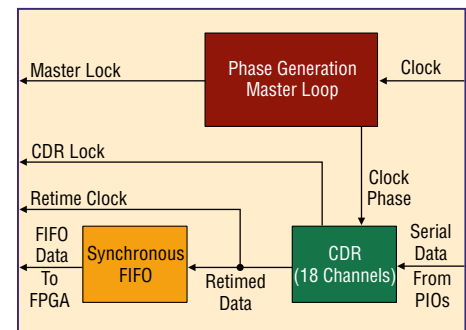
- Additional Quarter Rate Mode for Sub-10G Traffic
- Programmable Burst Modes to Support Intel Requirements
- Optional User Defined Status Path
- Lowest Power Solution Available!



Low Speed CDR

- Used for Retiming Slow Speed Data Streams from 100 - 550 Mbps
- Jitter Tolerance of 0.85UI
- No Additional Logic Required (FIFOs are Built-in)
- Supports 18 Data Channels

- Includes Synchronous Mode for 36-bit AIL-like Channels
- Supports Pathological Signals
- Multi-rate Support on a Single Pin!



LTSSM for PCIe

- Integral part of PCI Express Solution
- V1.0 and V1.0a Scrambling Polynomials
- PHY Framing
- Link Training & Status State Machine
- Link Width & Lane Negotiation

- Checking of Violations of the Link Initialization and Training Protocols
- Disables the Scrambling Function Upon Being Notified by the Data Link Layer

