

Lattice Military/Aerospace Solutions

Proven Programmable Technology

Today's military and aerospace systems designers have to satisfy multiple and often competing system objectives. Designers must balance issues such as system security, low power consumption, flexibility, cost, integration and fast time-to-market.

Programmable technologies have become increasingly popular as a method to meet these objectives, particularly in low to medium volume applications typically required in military and aerospace environments. Unlike ASICs, Lattice programmable solutions are standard products, avoiding long lead-times, NREs and long design cycles typical of full- or semi-custom ASIC products.

Advantages of Programmability

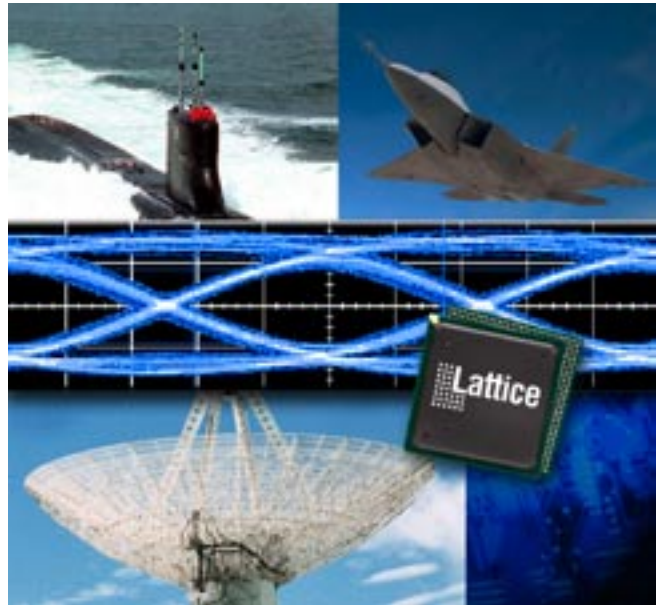
Programmable Logic	ASIC
<ul style="list-style-type: none"> • Standard product • Reduced time-to-market 	<ul style="list-style-type: none"> • Custom product • Long lead time for first silicon; may require respin
<ul style="list-style-type: none"> • Reprogrammable in the field • No NRE • Lowest cost for most applications 	<ul style="list-style-type: none"> • Fixed function • High NRE • Low cost for high volume, mature designs

Commercial-Off-The-Shelf (COTS)

Lattice offers an industry-leadership portfolio of Programmable Logic Devices (PLDs), FPGAs, CPLDs, Programmable Interface and Programmable Mixed Signal products in support of a wide range of military and aerospace applications. Supporting the mil / aero demand for Commercial-Off-The-Shelf (COTS) components, Lattice offers a comprehensive array of high-performance, low-power, Automotive (-40 to 125° C), Industrial (-40 to 85° C) and Commercial (0 to 70° C) grade product families. For those applications requiring Military (-55 to 125° C) grade components, Lattice offers simple PLDs (SPLDs) and complex PLDs (CPLDs) in the DESC Standard Military Drawing (SMD) configuration. The SMD Program offers a cost effective alternative to source control drawings and provides standardized MIL-STD-883 product specifications to simplify military procurement.

Advantages of COTS

- Ensures Access to Latest Technologies
- Commercial Marketplace Funds Research and Development
- Lower Cost Due to Commercial Market Competition and Quantities
- Implementation with COTS Provides Major Development and Recurring Cost Advantages over Unique Design Implementation



Key Features and Benefits

- **Broadest Range of Military and Aerospace Programmable Solutions**
 - COTS: Automotive, Industrial and Commercial temperature grades
 - Military: Standard Military Drawing (SMD)
- **Easy to Use**
 - In-System Programmable (ISP™)
 - Boundary scan testable
 - Programmable support for up to 21 I/O standards, including LVDS, SSTL and HSTL
 - Instant-on – quick availability of logic at boot-up
 - Industry standard third-party design tools
- **Low Power CMOS Operation**
 - Lowest dynamic power consumption (one-third to one-half of competitive devices)
 - Lowest static power consumption (10µA static I_{cc})
- **System-Level Integration**
 - 2K-16K LUT4 FPGAs
 - 32-1,024 Macrocell CPLDs
 - 32-496 I/Os
 - Advanced, space-saving packages
 - 5, 3.3, 2.5, 1.8, 1.5 volt power supply operation
 - RAM, PLLs, SERDES integrated on single chip
- **Security**
 - Non-volatile, single-chip solution
 - No external bit-stream required for configuration
 - Security bits prevent unauthorized read-back
- **Robust High Speed**
 - World's fastest programmable logic devices (2.3ns pin-to-pin delay)
 - Fastest programmable SERDES (3.7 Gbps per channel)
 - 10 Gbps stand-alone SERDES

Lattice Mil/Aero Prod

ISP

Lattice Semiconductor pioneered In-System Programmability (ISP) over ten years ago, and now it's an industry standard, utilized in a wide spectrum of applications. Why have designers embraced the ISP concept? For many, the manufacturing cost benefits and faster logic design and prototyping have been the most significant benefits of ISP. In addition, ISP's ability to reconfigure systems immediately prior to and after shipment has opened up new possibilities. System designers are now able to exploit hardware that can evolve after the product has shipped; features can be changed based on updates transmitted from a central site. Hardware can be configured and optimized for every mission. The combination of ISP with infinite reprogrammability is the next evolution in programmable technology, ispXP™.

ispXP Technology

ispXP (in-system programmable eXpanded Programming) is an innovative, new programming technology that combines E²CMOS® and SRAM cells on the same device. ispXP eliminates the requirement for an off-chip boot memory! The device configuration is stored in on-chip E²CMOS and automatically loaded into the SRAM array for device configuration at power-up. Thus, devices with ispXP technology are both non-volatile and infinitely reconfigurable. ispXP technology results in an instant-on, highly-secure, single-chip programmable solution, ideal for military and aerospace applications. ispXP technology is available in the new ispXPGA™ family of FPGAs and in the ispXPLD™ 5000MX family of CPLDs.

Comparison of FPGA Technologies

Feature	Lattice ispXP	Flash FPGA	Antifuse FPGA	SRAM FPGA
Non-volatile	Yes	Yes	Yes	No
Instant-on	Yes	Yes	Yes	No
Infinitely Reconfigurable	Yes	No	No	Yes
Single-chip Solution	Yes	Yes	Yes	No
Reprogrammable	Yes	Yes	No	Yes
"On-the-fly" Reprogrammable	Yes	No	No	Yes
Security Level	Secure	Secure	Secure	Vulnerable
Power-up Sequencing	Simple	Complex	Simple	Complex
Programming Voltages	1	3	1	1
5V Tolerance	Yes	No	With external resistors	With external resistors

Lattice Products by Temperature Grade

Temperature Grade	Lattice Products
Military: -55 to 125° C	GAL®, ispLSI® 1000
Automotive: -40 to 125° C	ispMACH 4000V, ispMACH 4000Z, ispPAC®-POWR1208, ispPAC-POWR604
Industrial: -40 to 85° C	All Lattice Products
Commercial: 0 to 70° C	All Lattice Products

ispXPGA – Non-volatile, Reconfigurable, Secure FPGAs

FPGAs are ideal for replacing expensive ASICs, gate-arrays, and ASSPs, such as bus interface chip sets. The ispXPGA family is the world's first FPGA to offer in-system programmability, non-volatility, instant-on and infinite reconfigurability. Other FPGA solutions force a compromise, being either volatile (SRAM-FPGA), one-time programmable (Antifuse), or complex to program (Flash FPGA). The ispXPGA family offers all these capabilities with a mainstream FPGA architecture containing the features required for today's system-level designs, including:

- Programmable support for up to 16 I/O standards, including LVDS, SSTL and HSTL
- Wide range of IP, including advanced DSP and interface cores
- On-chip Block RAM and Distributed Memory
- Phase Lock Loops (PLLs) for clock management
- 850Mbps SERDES for high-speed serial interfaces

ispXPLD 5000MX – CPLDs with Memory

The ispXPLD (eXpanded Programmable Logic Device) 5000MX combines the best attributes of CPLDs and FPGAs in a single architecture, built around a new building block, the Multi-Function Block (MFB). These MFBs can be configured as 136-input logic, single- or dual-port memory, FIFO or CAM depending on the user's application. This unparalleled PLD flexibility is combined with sysIO™ interfaces to support popular advanced I/O standards including LVDS, SSTL and HSTL. The devices also feature sysCLOCK™ PLLs for chip-level and board-level clock management and IP to ease the design process and speed time-to-market.



With security bits to prevent readback and no external bitstream, ispXPGA and ispXPLD devices offer an excellent solution for security-sensitive applications.

Device Family	Description	Supply Voltage (VCC)	5V Tolerant I/O	Packages	Commercial	Industrial	Automotive	Military/SMD
Simple and Complex PLDs (Programmable Logic Devices)								
GAL	8-12 Macrocells, Standard PLD Architectures, t_{PD} as Low as 3.5ns (250MHz)	5, 3.3	✓	J20, J28, P20, P24, P28, R20, R28, D20, D24	✓	✓		✓
ispGAL22V10	In-System Programmable 22V10, t_{PD} as Low as 2.3ns (455MHz)	5, 3.3, 2.5, 1.8	✓	J28, K28, N32	✓	✓		
ispLSI 1000	64-192 Macrocells, t_{PD} as Low as 4.5ns (200MHz)	5	✓	J44, Q128, T44, T100, T128, H44, H68, G84, G133	✓	✓		✓
ispLSI 5000VE	128-512 Macrocells, SuperWIDE™ Architecture, t_{PD} as Low as 5ns (180MHz)	3.3	✓	T100, T128, B272, B388, F256, F388	✓	✓		
ispMACH 4000Z	32-256 Macrocells, Zero Standby Power, t_{PD} as Low as 3.5ns (267MHz)	1.8	✓	T48, T100, T176, M56, M132	✓	✓	✓	
ispMACH 4000V	32-512 Macrocells, t_{PD} as Low as 2.5ns (400MHz), Low Power	3.3	✓	T44, T48, T100, T128, T144, T176, F256	✓	✓	✓	
ispMACH 4000B	32-512 Macrocells, t_{PD} as Low as 2.5ns (400MHz), Low Power	2.5	✓	T44, T48, T100, T128, T176, F256	✓	✓		
ispMACH 4000C	32-512 Macrocells, t_{PD} as Low as 2.5ns (400MHz), Low Power	1.8	✓	T44, T48, T100, T128, T176, F256	✓	✓		
ispMACH 5000B	128-512 Macrocells, 14 I/O Standards, SuperWIDE Inputs, t_{PD} as Low as 3.0ns (275MHz)	2.5		T128, Q208, F256, F484	✓	✓		
ispMACH 4A5	32-256 Macrocells, t_{PD} as Low as 5ns (182MHz)	5	✓	J44, V44, V48, V100, V144, Y100, Y208	✓	✓		
ispXPLD 5000MV	256-1024 Macrocells, up to 512K on-chip RAM, 15 I/O Standards, PLLs, t_{PD} as Low as 4ns (300MHz)	3.3	✓	Q208, F256, F484, F672	✓	✓		
ispXPLD 5000MB	256-1024 Macrocells, up to 512K on-chip RAM, 15 I/O Standards, PLLs, t_{PD} as Low as 4ns (300MHz)	2.5	✓	Q208, F256, F484, F672	✓	✓		
ispXPLD 5000MC	256-1024 Macrocells, up to 512K on-chip RAM, 15 I/O Standards, PLLs, t_{PD} as Low as 4ns (300MHz)	1.8	✓	Q208, F256, F484, F672	✓	✓		
Field Programmable Gate Arrays (FPGAs)								
ispXPGA-B	139K-1.25M Gates (2K-15K LUT4), up to 414K Block RAM, Non-volatile, up to 20@850Mbps SERDES, 16 I/O Standards, 8 PLLs	3.3/2.5	✓	F256, FH516, FE680, F900	✓	✓		
ispXPGA-C	139K-1.25M Gates (2K-15K LUT4), up to 414K Block RAM, Non-volatile, up to 20@850Mbps SERDES, 16 I/O Standards, 8 PLLs	1.8	✓	F256, FH516, FE680, F900	✓	✓		
ORCA 4	397K-899K Gates (5K-16K LUT4), 74K-148K Block RAM, 17 I/O Standards, 8 PLLs	1.5		BA352, BM416, BM680	✓	✓		
ORCA 3	36K-340K Gates (1K-12K LUT4)	3.3, 2.5	✓	Q208, Q240, BA352, BA432, BA600, BM680	✓	✓		
ORCA 2	11K-99K Gates (400-3.6K LUT4)	5, 3.3	✓	J84, T100, T144, Q160, Q208, Q240, Q304, BA256, BA352, BA432	✓	✓		
ORCA 4 FPSC Family – SERDES/Line Interface + FPGA								
ORT82G5/ ORT42G5	8/4@3.7Gbps SERDES, XAUI/FC support, 17 I/O Standards, 4 PLLs, 643K Gates (10K LUT4), 111K Block RAM	1.5		BM484, BM680	✓	✓		
ORSO82G5/ ORSO42G5	8/4@2.7Gbps SERDES, SONET support, 17 I/O Standards, 4 PLLs, 643K Gates (10K LUT4), 111K Block RAM	1.5		BM484, BM680	✓	✓		
ORT8850H ORT8850L	8@850Mbps SERDES, SONET support, 17 I/O Standards, 4 PLLs, 297K/899K Gates (5K/16K LUT4), 74/148K Block RAM	1.5		BM680	✓	✓		
ORLI10G	10 GbE Line Interface, XSBI/XGMII support, 17 I/O Standards, 4 PLLs, 643K Gates (10K LUT4), 111K Block RAM	1.5		BM680	✓	✓		
XPIO™ Family – 10Gbps PHY Physical Layer Transceivers								
XPIO 110GXS	9.95-10.71 Gbps Data Rates, SONET OC-192, 10GE, 10GFC, XSBI/SFI4.1 and XFP Support, 0.8W Power Consumption	1.3		CF269	✓			
ispPAC Family – Programmable Power Supply Sequencing and Monitoring, Filters, Analog Front Ends and Feedback Control Loops								
ispPAC-POWR1208 ispPAC-POWR604	Power Supply Sequencing and Monitoring: Total Power Management for up to 12 Power Supplies on Multi-voltage Circuit Board	2.25-5.5	✓	T44		✓	✓	
ispPAC10	In-System Programmable Mixed Signal Circuit, 4 Programmable Filter Blocks, Signal Conditioning	5	✓	S28, P28		✓		
ispPAC20	In-System Programmable Mixed Signal Circuit, 4 Programmable Gain Instrumentation Amplifiers, Programmable Filter/Comparator/DAC, Control Loop and Monitoring	5	✓	J44, T44		✓		
ispPAC30	In-System Programmable Analog Filter, Versatile Analog Front-End	5	✓	S24, P28		✓		
ispPAC80/81	Ultra-flexible, Continuous Time, 5th Order Lowpass Filter 10kHz - 750kHz	5	✓	S16, P16		✓		
ispGDx Family – Programmable SERDES, Interface + Interconnect								
ispGDx2™-V	64-256 I/O, Up to 188:1 MUX Width, t_{PD} as Low as 3ns (330MHz), 18 I/O Standards, 4-12@850Mbps SERDES, 2-4 PLLs	3.3	✓	F100, F208, F484	✓	✓		
ispGDx2-B	64-256 I/O, Up to 188:1 MUX Width, t_{PD} as Low as 3ns (330MHz), 18 I/O Standards, 4-12@850Mbps SERDES, 2-4 PLLs	2.5	✓	F100, F208, F484	✓	✓		
ispGDx2-C	64-256 I/O, Up to 188:1 MUX Width, t_{PD} as Low as 3ns (330MHz), 18 I/O Standards, 4-12@850Mbps SERDES, 2-4 PLLs	1.8	✓	F100, F208, F484	✓	✓		
ispGDxV™	80-240 I/O, Programmable Interface + Interconnect, Up to 16:1 MUX Width, t_{PD} as Low as 3ns (300MHz)	3.3	✓	T100, Q208, B272, F208, F388	✓	✓		
ispGDx®	80-160 I/O, Programmable Interface + Interconnect, Up to 4:1 MUX Width, t_{PD} as Low as 5ns (143MHz)	5	✓	T100, T176, Q160, Q208, B272	✓	✓		

Lattice Quality and Reliability

Lattice Semiconductor is committed to providing its customers with the highest quality and most reliable products in the industry. The first major PLD manufacturer to complete ISO9000 registration, Lattice has been registered to the ISO9001 standard since September 1993. In addition, Lattice internal specifications are compliant with applicable JEDEC and Military standards and our quality program is in full compliance with the quality assurance requirements of MIL-I-38535B Appendix C and all of the inspection systems requirements of MIL-I-45208.

Longevity and Commitment

Lattice has manufactured devices for the military and aerospace markets for more than 10 years. In an industry where programs often last more than 10 years, Lattice understands the importance of continuity of supply. When processes change, Lattice devices retain their original functionality and pinout compatibility. Lattice is committed to helping our customers achieve success both now and in the long term.

Lattice ispLEVER™ Design Tools

Lattice's ispLEVER programmable logic design software is both powerful and easy to use, helping to maximize productivity and shorten the design cycle. ispLEVER supports all Lattice programmable logic products, the most popular design entry methods and advanced simulation capabilities. Lattice has partnered with leaders in the CAE industry to include



VHDL and Verilog Synthesis from Mentor Graphics and Synplicity, and RTL simulation from Mentor Graphics. PC and UNIX versions are available. For more information, visit www.latticesemi.com/isplever.

Intellectual Property

Lattice offers an expanding range of reusable IP cores (ispLeverCORE™ IP modules) that allow customers to easily integrate many common functions into their Lattice programmable devices. Lattice IP cores help minimize the effort of complex designs, significantly reducing time-to-market and cost. Most ispLeverCORE modules are parameterized. That is, the core can be quickly reconfigured to meet specific system needs. Listed below is a sample of the Lattice IP Cores that are particularly useful in military and aerospace applications. For more information, visit www.latticesemi.com/ip.

- Turbo Encoder
- Turbo Decoder
- Convolutional Encoder
- Reed-Solomon Encoder
- Reed-Solomon Decoder
- Parallel FIR Filter
- Serial FIR Filter
- UARTs
- Encryption Cores
- PCI Master/Target



Software Product	GAL, ispGAL, ispGDX/2, ispXPLD, ispMACH CPLD	ispXPGA, ORCA FPGA	ORCA FPSC	ispPAC	Leonardo Spectrum Synthesis	Synplify Synthesis	ModelSim Simulation
ispLEVER™ (Starter - PC) Downloadable	✓	ispXPGA 125, ispXPGA 200 only			✓	✓	
ispLEVER - HDL (Base - PC)	✓	✓			✓	✓	✓
ispLEVER - Exemplar (Advanced - PC)	✓	✓	✓		✓		✓
ispLEVER - HDL (Advanced - PC)	✓	✓	✓		✓	✓	✓
ispLEVER (Advanced - UNIX)	✓	✓	✓				
PAC-Designer®				✓			

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Bringing the Best Together