

Introduction

The LSC BSCAN-1 is a multiple boundary scan test access port (TAP) addressable buffer function that can be accessed through a standard IEEE 1149.1 interface. With three Local Scan Ports (LSP), the BSCAN-1 function can be structured as hierarchical ports with the ability to add and remove local scan chains to improve test throughput. The LSP can also be accessed individually or in combination of two or three ports at a time to streamline the test flow of similar devices.

The LSP is configured by accessing the Mode Register from the primary TAP interface. In addition to the standard TAP interface signals TDI, TMS, TCK, TDO and TRST, the test signal source interface also includes the six static ID inputs and the TOE input. The Mode Register is used to configure the configuration of the local or secondary scan port. It also allows daisy chaining and bypassing of the local scan ports. The static ID inputs are capable of supporting up to 64 unique addresses. The active low TOE signal is used to disable all the local scan ports.

The major functional blocks and general architecture of the LSC BSCAN-1 are illustrated in Figure 1. As defined in IEEE Standard 1149.1, the instruction register and various test data registers can be scanned to exercise the functions of the LSC BSCAN-1. The 16-state state machine TAP controller provides the main control for the device.

The primary function of the selection controller is to compare the address shifted into the Instr Register to the static identification inputs, allowing the 1149.1 protocol to be used with the multidrop environment. It then enables the LSC BSCAN-1, as appropriate, for other operations. Multiplexing logic for selecting different port configurations is contained in the Local Scan Port (LSP).

The LSC BSCAN-1 instruction register, mode register and the TAP controller are all read into the LSP control block where the local scan port controllers are located (LSP₁, LSP₂ and LSP₃). All four TAP boundary scan signals are then fed from their respective ports to the local scan chains.

Functional Overview

In a multidrop scan system, the scan tester has the ability to select individual LSC BSCAN-1 devices as needed for scan operations. Scan chains are selected when a particular device address is sent to all LSC BSCAN-1 devices. The device with the corresponding, hardcoded address is enabled to receive instructions from the scan tester. This selection is done using a “Level 1” protocol and subsequent instructions are sent to the appropriate LSC BSCAN-1 by using a “Level 2” protocol.

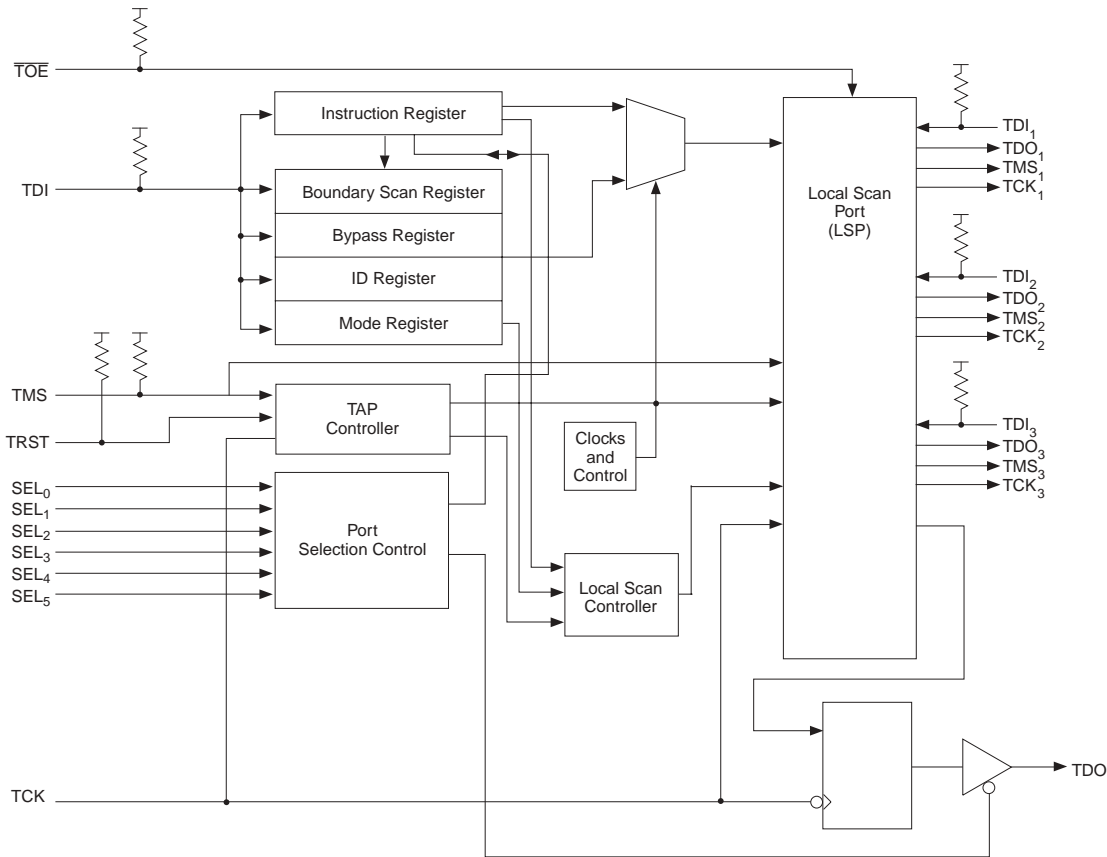
As is described in Figure 2, the LSC BSCAN-1 contains an 1149.1 TAP control state machine (Figure 3), a selection state machine (Figure 4) and a local port state machine (identical for each local port, see Figure 5).

The selection state machine is responsible for the addressing and multidrop capability. It also supports functionality for single access and the chip’s Level 1 protocol. The local port state machine allows the individual enabling and disabling of local scan chains from the overall scan chain.

The port configuration state machine controls which local scan ports are included in, and which ports are isolated from, the overall scan chain. Therefore, to the system scan controller, each LSC BSCAN-1 represents only a single scan chain. Internal to the LSC BSCAN-1 is the logic that controls which or how many of the local ports are included in the chain presented to the master. There are two stable states in which a local port can be parked: Parked-TLR and Parked-RTI. Once a chain is parked, it is removed from the active scan chain indefinitely, or until “unparked.” Unparking a chain moves it into the active chain. As is shown in Figure 5, the state of each of the local ports is independent of the states of other local ports on the LSC BSCAN-1. It is important to understand that some states depend on the current state of the TAP control state machine, while in others the state of the LSC BSCAN-1’s TAP control state machine can be forced by transitions of the scan port configuration state machine. The LSC BSCAN-1’s scan port configuration state machine provides part of the Level 2 protocol and has a number of Level 2 instructions other than local scan port configuration that provide access to and control of various registers within the LSC BSCAN-1. The instructions include:

LSC BSCAN-1: IEEE 1149.1 Multiple Scan Port Addressable Buffer

Figure 1. LSC BSCAN-1 Block Diagram



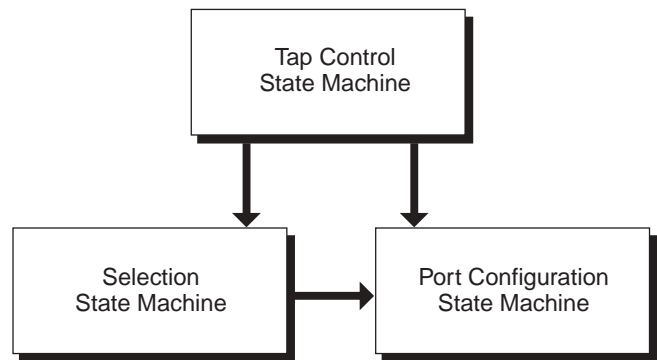
BYPASS	EXTEST
SAMPLE/PRELOAD	IDCODE
MODESEL	GOTOWAIT

Each LSC BSCAN-1 can be selected as an individual. Level 2 protocol commands are used to park or unpark. After a reset, the LSC BSCAN-1 is ready for Level 1 protocol and Level 2 protocol instructions, in that order. The TAP controller state machine is reset to the TLR (Test-Logic-Reset) state, the selection state machine is in the Wait-for-Address state and the three local port selection state machines are in the Parked-TLR state.

Backplane Interface

Via its backplane port, the LSC BSCAN-1 receives instructions from the IEEE 1149.1 tester. The LSC BSCAN-1 enters the Wait-for-Address state following the test logic reset. Data is shifted in through the TDI input and into the LSC BSCAN-1 Instruction register when the TAP controller is sequenced to the Shift-IR state. Note that if LSC BSCAN-1 is not properly addressed and successfully selected, no data is shifted out of the instruction register.

Figure 2. Internal State Machines



Instead, as data is shifted into the instruction register, the data shifted out is discarded rather than exiting through the TDO output. Upon updating the instruction register with the address data, the scanned-in address is compared with the six least significant bits of the IR and the static address signals SEL(0-5).

If no address match is detected, the device enters an unselected state. When an address is matched, it enters

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Figure 3. IEEE 1149.1 State Machine

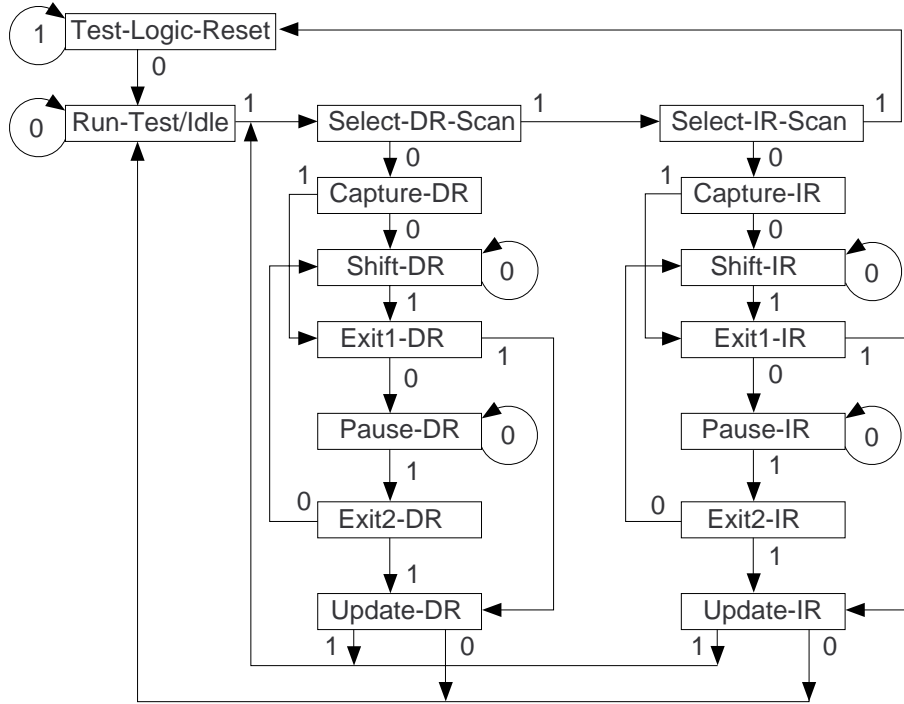


Figure 4. Selection Controller State Machine

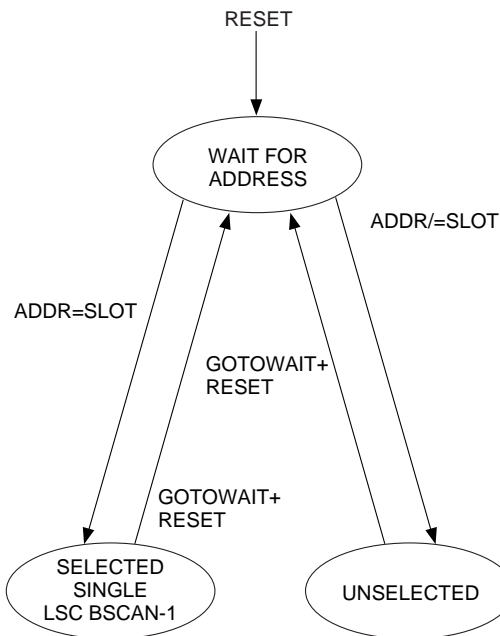
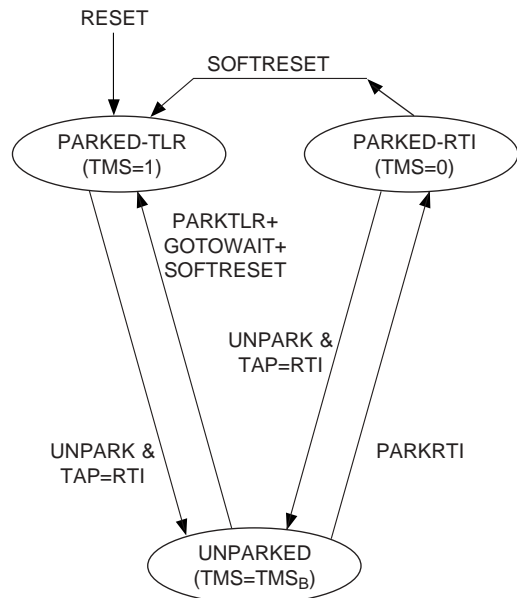


Figure 5. Local Port Configuration State Machine



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the selected state. Level 2 protocol is used to issue commands and access registers once a LSC BSCAN-1 has been selected.

Register Set

Selection and configuration, scan data manipulation and scan support operations registers can all be grouped as shown in Table 1. When a register is selected, data enters through the MSB and is shifted out through the scan input of the next device in the daisy chain.

Addressing Scheme

The basic function of the LSC BSCAN-1 is to allow a large or complex system to be divided into smaller blocks for testing purposes. A central test controller is networked with one or more LSC BSCAN-1 devices and given the capability to address individual LSC BSCAN-1 devices. Both multidrop and hierarchical connectivity are supported and the test controller can dynamically select any part of the network.

The LSC BSCAN-1 supports two levels of partitioning. Level 1 protocol supports the selection of one LSC BSCAN-1 device. Within each device, a Level 2 protocol supports the selection of individual ports. The selected ports of the individual device are then presented as a single chain that can be included in the final network of the selected LSC BSCAN-1 device.

Addressing with Level 1 Protocol

One mode of addressing is supported by the LSC BSCAN-1. Individual LSC BSCAN-1 devices can be selected in the “single” mode, also known as Direct Addressing.

Direct Addressing

Table 1. Registers

Register Name	Signal Description
Instruction Register	Addressing and Instruction Decode IEEE Standard 1149.1 Required Register
Boundary Scan Register	IEEE Standard 1149.1 Required Register
Bypass Register	IEEE Standard 1149.1 Required Register
Device Identification Register	IEEE Standard 1149.1 Required Register
Mode Register	Local Port Configuration and Control Bits

Table 2. Direct Address Mode

Address Type/Hex Address	Binary Address	TDO State
Direct Address 00 to 3F	XX000000 to XX111111	Normal IEEE Standard 1149.1

Note: Only the six LSBs of the address are compared to the S (0-5) inputs. The two MSBs are “don’t cares.”

The LSC BSCAN-1 enters the Wait-for-Address state when: (1) Its TAP Controller enters the Test-Logic-Reset state, or (2) Its instruction register is updated with the GOTOWAIT instruction, while either selected or unselected.

While in the Wait-for-Address state, the LSC BSCAN-1 controller receives data shifted in through the instruction register. In the Update-IR state, bits 5 through 0 of the instruction register are compared with the statically configured address bits SEL(0-5). (Every LSC BSCAN-1 device in a scan network must be individually set with a unique address on its SEL(0-5) inputs.) A LSC BSCAN-1 device becomes selected, or active in the chain, when the six least significant bits of the instruction register match the static address bits SEL(0-5) (Figure 6). The selected device is now ready to receive Level 2 protocol. When active, the selected device’s identification register is inserted as part of the active scan chain.

Unselected devices (where the static address did not match the six LSBs of the IR) will remain that way until their instruction register is updated with the GOTOWAIT instruction or their TAP controller enters the Test-Logic-Reset state.

Level 2 Protocol

Level 2 protocol follows IEEE standard 1149.1 TAP protocol. After being addressed and selected in the active chain, the LSC BSCAN-1 device is accessed by Level 2 protocol. Once the LSC BSCAN-1 is selected, the local scan ports remain parked in one of two TAP Controller states (Run-Test/Idle, Test-Logic-Reset). The scan chain comes in through the TDI, through the instruction register or IDCODER register, and out through the TDO.

LSC BSCAN-1: IEEE 1149.1 Multiple Scan Port Addressable Buffer

Figure 6. Direct Addressing: Device Address Loaded into Instruction Register

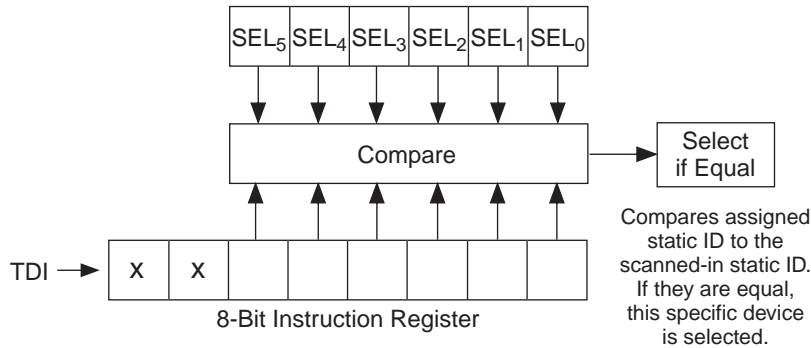


Table 3. Instruction Set

Instruction	Hex Opcode	Binary Opcode	Data Register
EXTEST	00	00000000	Boundary Scan Register
SOFTRESET	88	10001000	Device Identification Register
MODESEL	8E	10001110	Mode Register
PARKRTI	84	10000100	Device Identification Register
SAMPLE/PRELOAD	81	10000001	Boundary Scan Register
PARKTLR	C5	11000101	Device Identification Register
GOTOWAIT*	C3	11000011	Device Identification Register
IDCODE	AA	10101010	Device Identification Register
UNPARK	E7	11100111	Device Identification Register
BYPASS	FF	11111111	Bypass Register
Other Undefined	TBD	TBD	Device Identification Register

Note: All instructions act on selected LSC BSCAN-1s only.

Local scan ports can be inserted into the chain using the UNPARK instruction. The mode register is discussed later.

Level 2 Instruction Types

Level 2 has two instruction types (Table 3):

1) Insert instructions bring the LSC BSCAN-1 register into the active chain, making it available to be captured or updated. (SAMPLE/PRELOAD, EXTEST, IDCODE, MODESEL and BYPASS).

2) Configure/control instructions insert the device identification into the active scan chain. (GOTOWAIT, SOFTRESET, PARKRTI, PARKTLR, UNPARK and other undefined op codes).

Level 2 Instruction Descriptions

Bypass: When the LSC BSCAN-1 is selected, the BYPASS instruction inserts the bypass register into the active chain.

EXTEST: This instruction is the same as the SAMPLE/PRELOAD instruction since there are no scaleable outputs on the device. EXTEST inserts the boundary scan register into the active chain. The boundary scan register is a bank of seven “sample only” cells connected to the OE and SEL(0-5) inputs.

SAMPLE/PRELOAD: This instruction inserts the boundary scan register into the active chain (refer to EXTEST).

IDCODE: IDCODE inserts the device identification register into the active scan chain. When exiting the Capture-DR state and IDCODE is the current active instruction, the device identification “0FC0E01F” Hex is captured.

PARKTLR: Parks all unparked local scan ports in the Test-Logic-Reset TAP controller state and removes them from the active scan chain. A logic “1” is forced on the TMS_n output while the LSP controller is in the Parked-TLR state (Figure 5).

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Multiple Scan Port Addressable Buffer

PARKRTI: Parks all unparked Local Scan Ports in the Run-Test/Idle TAP controller state and removes them from the active scan chain. A logic “0” is forced on the TMS_n output while the LSP controller is in the Parked-TLR state (Figure 5).

UNPARK: Unpark takes the Local Scan Port Network out of park and inserts it into the active scan chain. The mode register determines the configuration of the chain, as described later. While local scan ports (LSP) are unparked, they are synchronously sequenced with the TAP controller. An LSP can only be unparked when the TAP controller enters the state it was in when the LSP became parked. For example: if the LSP was parked in the Test-Logic-Reset or Run-Test/Idle states, it is not unparked until an UNPARK instruction is followed by the TAP controller entering the Run-Test/Idle state (Figure 5).

GOTOWAIT: Parks all unparked local scan ports in the Test-Logic-Reset TAP controller state. All LSC BSCAN-1 devices are returned to the Wait-For-Address state (Figure 5).

MODESEL: Puts the mode register in the active scan chain.

SOFTRESET: Parks all local ports in the Test-Logic-Reset state within five TCK cycles by causing all three port configuration controllers to enter the Parked-TLR state. TMS_n is forced high (Figure 5).

Register Descriptions

Instruction Register

This is an 8-bit serial shift register placed in series with the active scan chain when the TAP controller of the LSC BSCAN-1 is in the Shift-IR state. When the LSC BSCAN-1 exits the Capture-IR state, the instruction register captures the value “XXXXXX01” where the don’t cares represent the SEL(0-5) inputs. When it is in the Wait-for-Address state, the LSC BSCAN-1’s instruction register is used for address matching. This is done by the individual chip comparing a hardwired value on the LSC BSCAN-1’s static ID inputs to the address in the instruction register. Address 00 through 3F (000000 through 111111 binary) are reserved for individual LSC BSCAN-1 addressing.

Boundary Scan Register

This is a 7-bit register consisting of cells from the OE and S(0-5) inputs. In order to allow testing of external circuitry, the Boundary Scan Register samples the inputs it is connected to without altering the internal logic of the chip. The shift order of the Boundary Scan register is:

TDI->OE ->SEL5 ->SEL4 -> SEL3 ->SEL2 ->SEL1 ->SEL0 ->LSP ->TDO.

Bypass Register

This one-bit register is defined by IEEE Standard 1149.1. Its primary purpose is to pass data between TDI and the local scan port. This register provides a passthrough path when none of the other registers are necessary. Using this register provides the shortest path to other registers located in the chain.

Mode Register

This is an 8-bit data register. Its primary function is to configure the local scan port network. When the LSC BSCAN-1 enters the Test-Logic-Reset State, the register is initialized with “01” Hex. The scan chain layout will be configured as shown in Table 4 when an UNPARK instruction executes. When all Local Scan Ports are parked, the configuration of the scan chain will be: TDI ->LSC BSCAN-1-register->TDO.

The third bit of the mode register can be used to disconnect all the TCK signals from TCK. Its normal configuration has it set to logic “0” so that TCK_n is free-running when the local scan ports are parked. Programming the third bit with a logic “1” forces the all the TCK_n signals to stop. Changing the value of this Mode register bit should only be done while all the local ports are parked. Power sensitive applications can use this feature to reduce the power consumed by the test circuitry in parts of the system currently not under test.

Bits 5, 6 and 7 are currently unused (don’t care) but are reserved for future use.

Device Identification Register

This 32-bit register is defined by IEEE Standard 1149.1. When an IDCODE instruction is received, this register is loaded with “0FC0E01F” Hex when the device Capture-DR state is left on the rising edge of TCK.

Reset

There are three levels of reset. The top level resets every LSC BSCAN-1 register and every local scan chain of both selected and unselected LSC BSCAN-1 devices. Entering the Test-Logic-Reset State automatically invokes this reset level. There are two ways to enter Test-Logic-Reset: 1) It is entered asynchronously when \overline{TRST} is pulled low or 2) It can be entered synchronously by pulling TSM high for five or more TCK pulses. When a top level reset occurs, all LSC BSCAN-1 registers are initialized, all local scan chains are parked in the

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Table 4. Mode Register Control of LSP

Mode Register	Scan Chain Configuration (if Unparked)
XXX0X000	TDI -> Register -> TDO
XXX0X001	TDI -> Register -> LSP ₁ -> PAD -> TDO
XXX0X010	TDI -> Register -> LSP ₂ -> PAD -> TDO
XXX0X011	TDI -> Register -> LSP ₁ -> PAD -> LSP ₂ -> PAD -> TDO
XXX0X100	TDI -> Register -> LSP ₃ -> PAD -> TDO
XXX0X101	TDI -> Register -> LSP ₁ -> PAD -> LSP ₃ -> PAD -> TDO
XXX0X110	TDI -> Register -> LSP ₂ -> PAD -> LSP ₃ -> PAD -> TDO
XXX0X111	TDI -> Register -> LSP ₁ -> PAD -> LSP ₂ -> PAD -> LSP ₃ -> PAD -> TDO
XXX1XXXX	TDI -> Register -> TDO (Loopback)

X = don't care

Register = LSC BSCAN-1 instruction register or any of the LSC BSCAN-1 test data registers

PAD = insertion of a 1-bit register for synchronization

Table 5. Detailed Device Identification (Binary)

Bits 31-28	Bits 27-12	Bits 11-1	Bit 0
Version	Part Number	Manufacturer Identity	1
0000	1111 1100 0000 1110	0000 0001 111	1

Table 6. Reset Configurations for Registers

Register	Bit Width	Initial Hex Value
Instruction	8	AA (IDCODE Instruction)
Mode	8	01

Test-Logic-Reset State, and all LSC BSCAN-1 are put into the Wait-for-Address state.

The SOFTRESET instruction is provided to perform a reset of all the LSPs of a selected LSC BSCAN-1. SOFTRESET forces all TMS signals high, placing the corresponding local TAP controllers in the Test-Logic-Reset state within five TCK cycles. The third level of reset is the resetting of individual local ports. An individual LSP can be reset by parking the port in the Test-Logic-Reset state via the PARKTLR instruction. To reset an individual LSP that is parked in the other parked state, the LSP must first be unparked via the UNPARK instruction.

Port Synchronization

When a LSP is not being accessed, it is placed in one of the two TAP controller states: Test-Logic-Reset or Run-Test/Idle. The LSC BSCAN-1 is able to park a local chain by controlling the local Test Mode Select outputs (TMS₁₋₃) (Figure 5). TMS is forced high for parking in the Test-Logic-Reset state and forced low for parking in the Run-Test/Idle state. Local chain access is achieved by issuing the UNPARK instruction. The LSPs do not become unparked until the LSC BSCAN-1 TAP controller is

sequenced through a specified synchronization state. Synchronization occurs in the Run-Test/Idle state for LSPs parked in Test-Logic-Reset and Run-Test/Idle states. Figures 7 and 8 show the waveforms for synchronization of a local chain that was parked in the Test-Logic-Reset state. Once the UNPARK instruction is received in the instruction register, the LSP Controller forces TMS_n low on the falling edge of TCK. This moves the local chain TAP controllers to the synchronization state (Run-Test/Idle), where they stay until synchronization occurs. If the next state of the LSC BSCAN-1 TAP Controller is Run-Test/Idle, TMS_n is connected to TMS and the local TAP controllers are synchronized to the LSC BSCAN-1 TAP controller as shown in Figure 7. If the next state after Update-IR were Select-DR, TMS_n would remain low and synchronization would not occur until the TAP controller entered the Run-Test/Idle state, as shown in Figure 7.

Each local port has its own Local Port Controller. This is necessary because the LSP can be configured in any one of eight possible combinations. Either one, some, or all of the local ports can be accessed simultaneously. Configuring the LSP is accomplished with the mode register, in

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Figure 7. Local Scan Port Synchronization on Second Pass

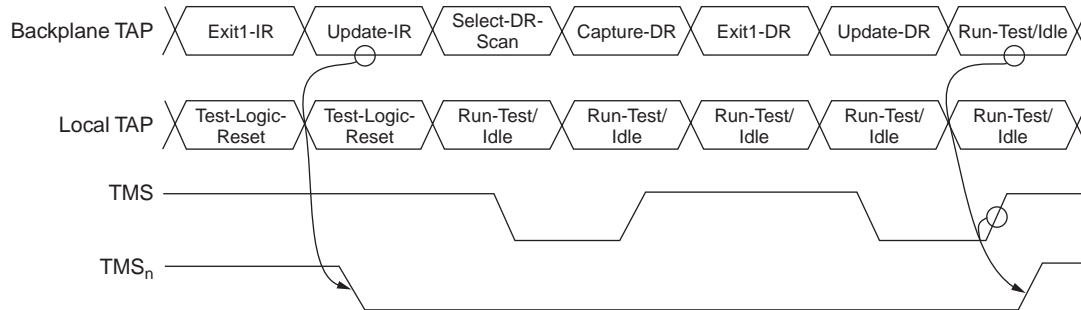
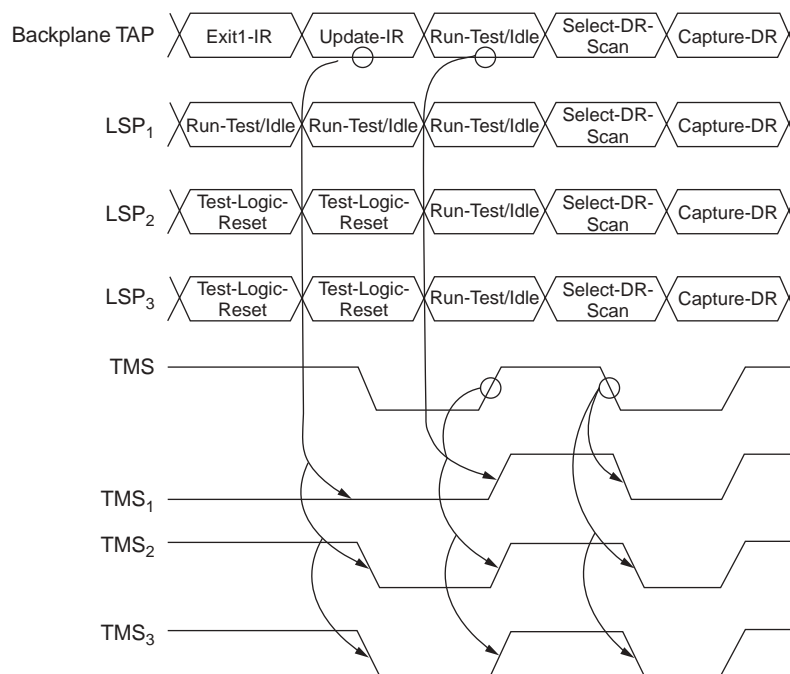


Figure 8. Synchronization of the Three Local Scan Ports (LSP₁, LSP₂ and LSP₃)



conjunction with the UNPARK instruction. The LSP can be unparked in one of seven different configurations, as specified by bits 0-2 of the mode register. Using multiple ports presents not only the task of synchronizing the LSC BSCAN-1 TAP Controller with the TAP Controllers of an individual local port, but also of synchronizing the individual local ports to one another. When multiple local ports are selected for access, it is possible that two ports are parked in different states. This could occur when previous operations accessed the two ports separately and parked them in the two different states. The LSP Controllers handle this situation gracefully.

Implementation

The LSC BSCAN-1 design has been implemented in a Lattice ispLSI 2192VE device. The ispLSI[®] device families are ideally suited to high-speed controller and state machine intensive applications. This design uses about 57% of the device macrocells with 24 I/O pins. The maximum operating frequency is 35MHz with the ispLSI 2192VE-100. The number of macrocells required varies, depending on the addition of new functions and/or removal of unneeded features. The ispLSI 2192VE features In-System Programmability (ISP[™]) and can be programmed up to 10,000 times for design configuration.

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This design was designed and simulated in VHDL using Lattice design tools. After the design was completed, the VHDL code was compiled. The use of VHDL with a CPLD allows functional and hardware changes to be made quickly and easily. When driving the backplane directly, buffers are needed for the ispLSI 2000VE device because of its limited drive.

JEDEC File

The JEDEC file for this reference design targeting the ispLSI 2192VE-xxLT128 or ispLSI 2192VE-xxLB144 is available from your Lattice sales representative. This design supports a maximum TCK frequency of 35MHz when using the ispLSI 2192VE-100 device. The pinouts are shown in Tables 7 and 8.

Ordering Information

TCKmax	JEDEC File OPN	Device OPN	Package
35MHz	LSC_BSCAN-1LT128	ispLSI 2192VE-100LT128	128-Pin TQFP
35MHz	LSC_BSCAN-1LB144	ispLSI 2192VE-100LB144	144-Ball BGA

Glossary

LSP: Local Scan Port. A four signal port that drives a “local” (i.e. non-backplane) scan chain. (e.g., TCK₁, TMS₁, TDO₁, TDI₁).

Local: Local is used to describe IEEE Standard 1149.1 compliant scan rings and the LSC BSCAN-1 Test Access Port that drives them. The term “local” was adopted from the system test architecture that the LSC BSCAN-1 is most commonly used in: a system test backplane with an LSC BSCAN-1 on each card driving up to three “local” scan rings per card. Each card can contain multiple LSC BSCAN-1s, with three local scan ports per LSC BSCAN-1.

Park/Unpark: Park, parked, unpark and unparked are used to describe the state of the LSP controller and the state of the local TAP controllers (the TAP controllers of the scan components that make up a local scan ring). Park is also used to describe the action of parking an LSP (transitioning into one of the Parked LSP controller states). It is important to understand that when an LSP controller is in a parked state, TMS_n is held constant, thereby holding or “parking” the local TAP controllers in a given state.

TAP: Test Access Port as defined by IEEE Standard 1149.1

Selected/Unselected: Selected and Unselected refers to the state of the Selection Controller. A selected LSC BSCAN-1 has been properly addressed and is ready to receive Level 2 protocol. Unselected LSC BSCAN-1 devices monitor the system test backplane, but do not accept Level 2 protocol (except for the GOTOWAIT instruction). The data registers and LSPs of unselected LSC BSCAN-1 devices are not accessible from the system test master.

Active Scan Chain: The Active Scan Chain refers to the scan chain configuration as seen by the test master at a given moment. When an LSC BSCAN-1 is selected with all of its LSPs parked, the active scan chain refers to the current scan bridge register only. When an LSP is unparked, the active scan chain becomes: TDI ->the current LSC BSCAN-1 register ->the local scan ring registers ->a PAD bit ->TDO. Refer to Table 4 for Unparked configurations of the LSP network.

Level 1 Protocol: Level 1 is the protocol used to address an LSC BSCAN-1.

Level 2 Protocol: Level 2 is the protocol that is used once an LSC BSCAN-1 is selected. Level 2 protocol is IEEE Standard 1149.1 compliant when an individual LSC BSCAN-1 is selected.

LSB: Least Significant Bit, the right-most position in a register (bit 0).

MSB: Most Significant Bit, the left-most position in a register.

PAD: A one-bit register that is placed at the end of each local scan port scan chain. The PAD bit eliminates the propagation delay that would be added by the LSC BSCAN-1 LSP logic between TDI_n and TDO_(n+1) or TDO by buffering and synchronizing the TDI_n inputs to the falling edge of TCK. This allows data to be scanned at higher frequencies without violating set-up and hold times.

Signal Descriptions

TMS: BACKPLANE TEST MODE SELECT – Controls sequencing through the TAP controller of the LSC BSCAN-1. Also controls sequencing of the TAPs on the three local scan chains.

TDI: BACKPLANE TEST DATA INPUT – All backplane scan data is supplied to the LSC BSCAN-1 through this input pin.

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TDO: BACKPLANE TEST DATA OUTPUT – This output drives test data from the LSC BSCAN-1 and the local TAPs, back toward the scan master controller

TCK: TEST CLOCK INPUT FROM THE BACKPLANE – This is the master clock signal that controls all scan operations of the LSC BSCAN-1 and of the three local scan ports.

TRST: TEST RESET – An asynchronous reset signal (active low) which initializes the LSC BSCAN-1 logic.

SEL(0-5): STATIC IDENTIFICATION – The configuration of these six pins is used to identify (assign a unique address to) each LSC BSCAN-1 on the system backplane

TOE: OUTPUT ENABLE – For the Local Scan Ports, active low. When low, this active low control signal tristates all three local scan ports on the LSC BSCAN-1. This enables an alternate resource to access one or more of the three local scan chains.

TDO₍₁₋₃₎: TEST DATA OUTPUTS – Individual output for each of the three local scan ports

TDI₍₁₋₃₎: TEST DATA INPUTS – Individual scan data input for each of the three local scan ports.

TMS₍₁₋₃₎: TEST MODE SELECT OUTPUTS – Individual output for each of the three local scan ports.

TCK₍₁₋₃₎: LOCAL TEST CLOCK OUTPUTS – Individual output for each of the three local scan ports. These are buffered versions of TCK.

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-826-6002 (International)
e-mail: techsupport@latticesemi.com

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Table 7. ispLSI 2192VE Pin Locations (128 TQFP)

Pin Name	Function	Pin Number
VCC	SYS	2
TOE	IN	7
TDO	OUT	9
TMS	IN	10
TCK	IN	11
TDI	IN	12
TRST	IN	15
VCC	SYS	16
GND	SYS	18
SEL(0)	IN	21
SEL(1)	IN	22
SEL(2)	IN	23
SEL(3)	IN	24
SEL(4)	IN	25
SEL(5)	IN	26
VCC	SYS	31
GND	SYS	34
VCC	SYS	47
GND	SYS	50
TMS_L3	OUT	51
TDO_L3	OUT	52
TCK_L3	OUT	53
TDI_L3	IN	54
GND	SYS	63
VCC	SYS	66
GND	SYS	79
VCC	SYS	81
TMS_L2	OUT	85
TDO_L2	OUT	86
TCK_L2	OUT	87
TDI_L2	IN	88
VCC	SYS	95
GND	SYS	98
TMS_L1	OUT	107
TDO_L1	OUT	108
TCK_L1	OUT	109
TDI_L1	IN	110
GND	SYS	111
VCC	SYS	114
GND	SYS	127

LSC BSCAN-1: IEEE 1149.1 Multiple Scan Port Addressable Buffer

Table 8. ispLSI 2192VE Pin Locations (144 BGA)

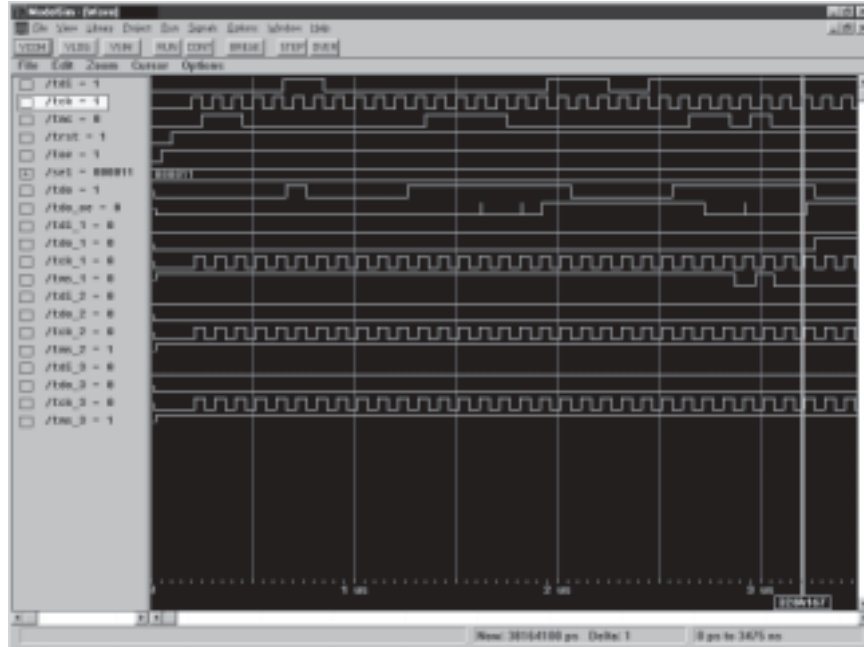
Pin Name	Function	Pin Number
GND	SYS	A1
VCC	SYS	L1
GND	SYS	D4
VCC	SYS	G8
GND	SYS	G7
VCC	SYS	B12
GND	SYS	M12
VCC	SYS	F5
TOE	IN	E2
GND	SYS	H5
VCC	SYS	L12
GND	SYS	E5
VCC	SYS	F8
TDO	OUT	E3
GND	SYS	A12
VCC	SYS	H6
TMS	IN	E4
GND	SYS	D9
VCC	SYS	E7
TCK	IN	D1
GND	SYS	G6
VCC	SYS	B1
TDI	IN	F4
GND	SYS	J9
VCC	SYS	G5
GND	SYS	F7
VCC	SYS	H7
GND	SYS	M1
VCC	SYS	E6
GND	SYS	H8
TRST	IN	G4
GND	SYS	E8
GND	SYS	J4
GND	SYS	F6
SEL(0)	IN	H4
SEL(1)	IN	G1
TMS_L2	OUT	F11
SEL(2)	IN	H2
TDO_L2	OUT	D12
SEL(3)	IN	H1
TCK_L2	OUT	E9
SEL(4)	IN	H3
TDI_L2	IN	E10
SEL(5)	IN	J1
TCK_L3	OUT	C12

Pin Name	Function	Pin Number
TMS_L1	OUT	A8
TDO_L1	OUT	B7
TCK_L1	OUT	A7
TDI_L1	IN	D7
TMS_L3	OUT	L7
TDO_L3	OUT	K7
TDI_L3	IN	M8

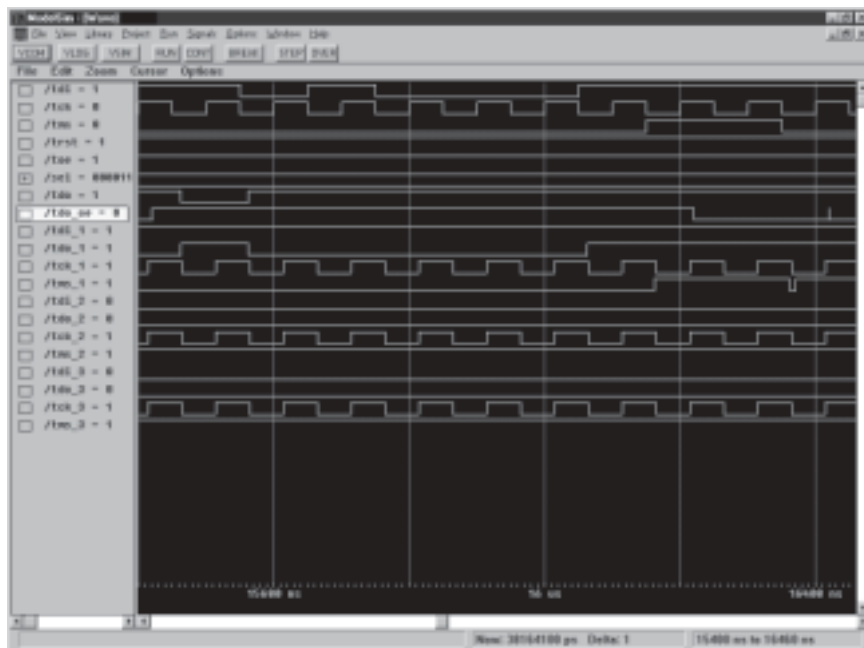
LSC BSCAN-1: IEEE 1149.1 Multiple Scan Port Addressable Buffer

Appendix

1. Select LSC BSCAN-1 by loading the instruction register in Shift-IR with the matching address. Unpark default LSP₁ and synchronize TAP controllers in Run-Test/Idle.



2. Park LSP₁ in Test-Logic-Reset by loading the PARKTLR instruction in Shift-IR and clocking TCK at least five times.

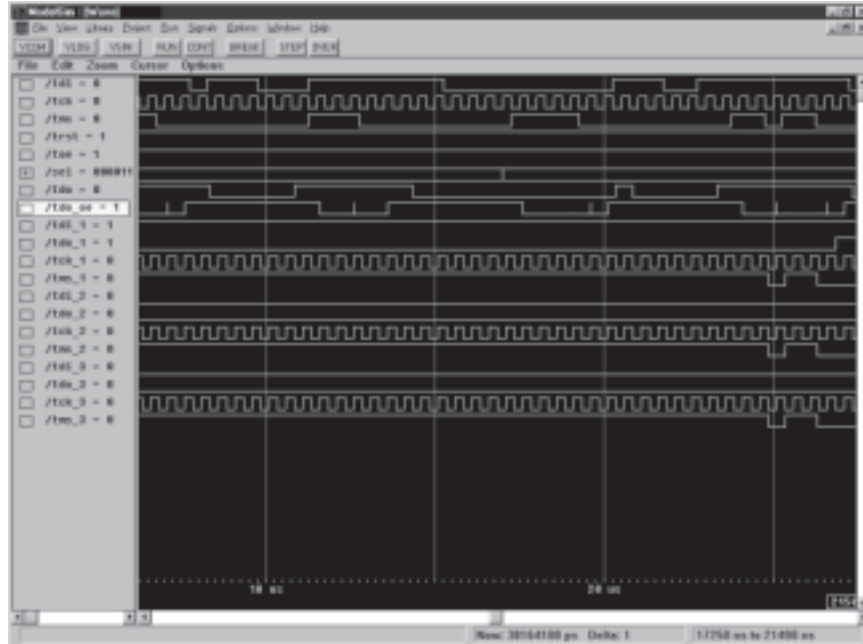


LSC BSCAN-1: IEEE 1149.1

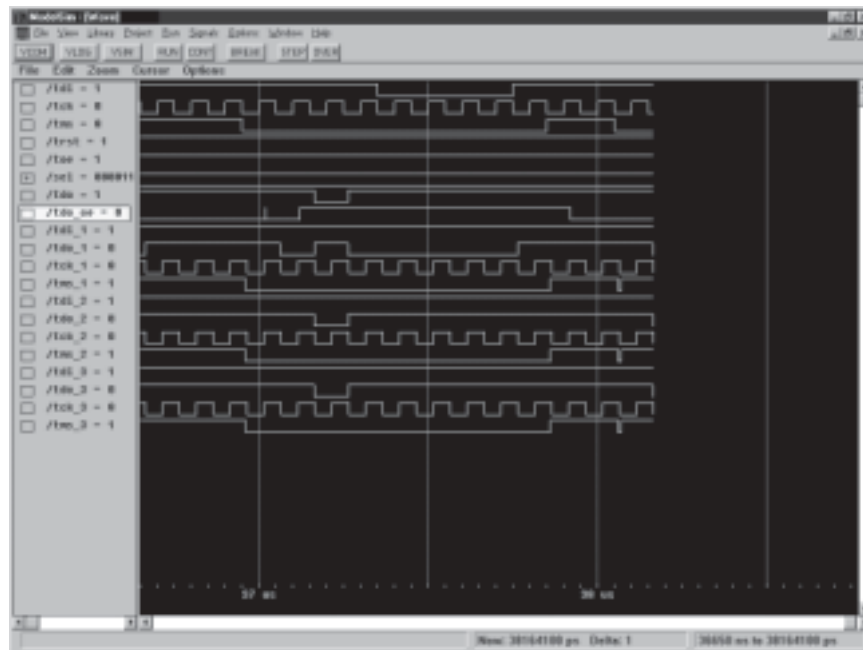
Multiple Scan Port Addressable Buffer

Appendix (Continued)

3. Enable all local scan ports by loading the MODESEL instruction in Shift-IR, moving to Shift-DR to configure the Mode register, loading the UNPARK instruction in Shift-IR and synchronizing all the TAP controllers in the Run-Test/Idle state.



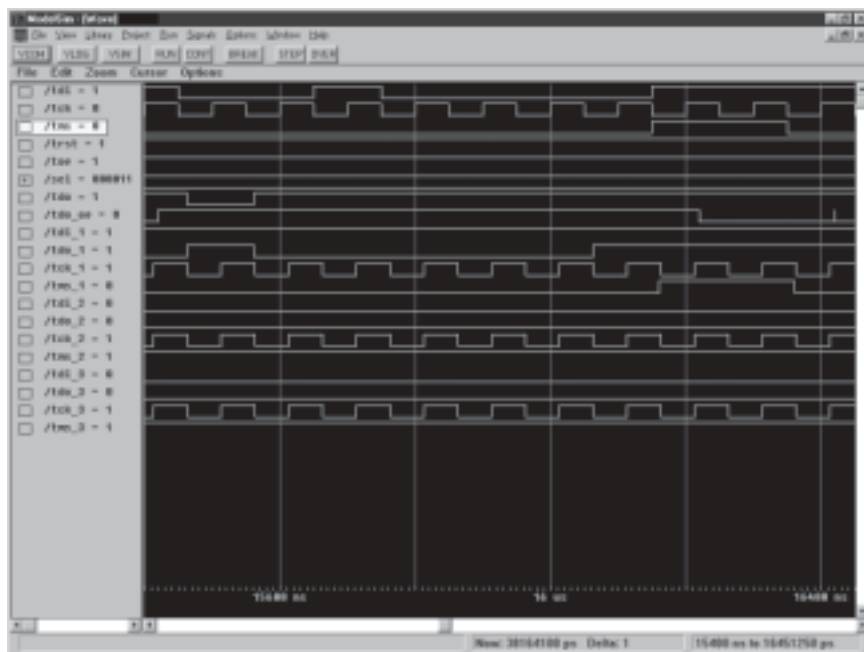
4. Park all local scan ports in Test-Logic-Reset by loading the GOTOWAIT instruction in Shift-IR and then clocking TCK at least five times.



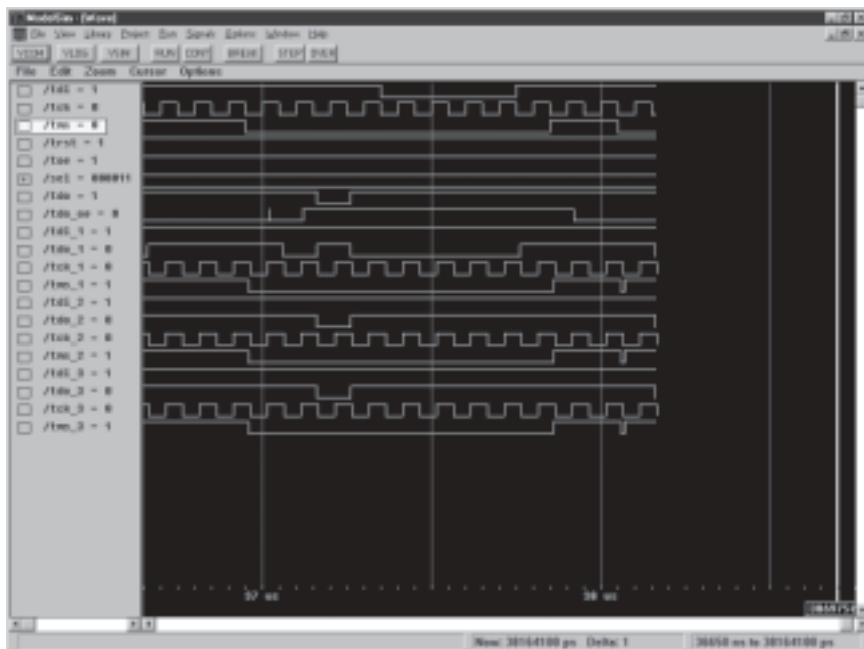
LSC BSCAN-1: IEEE 1149.1 Multiple Scan Port Addressable Buffer

Appendix (Continued)

5. Park LSP₁ in Run-Test/Idle by loading the PARKRTI instruction in Shift-IR and clocking to Run-Test/Idle.



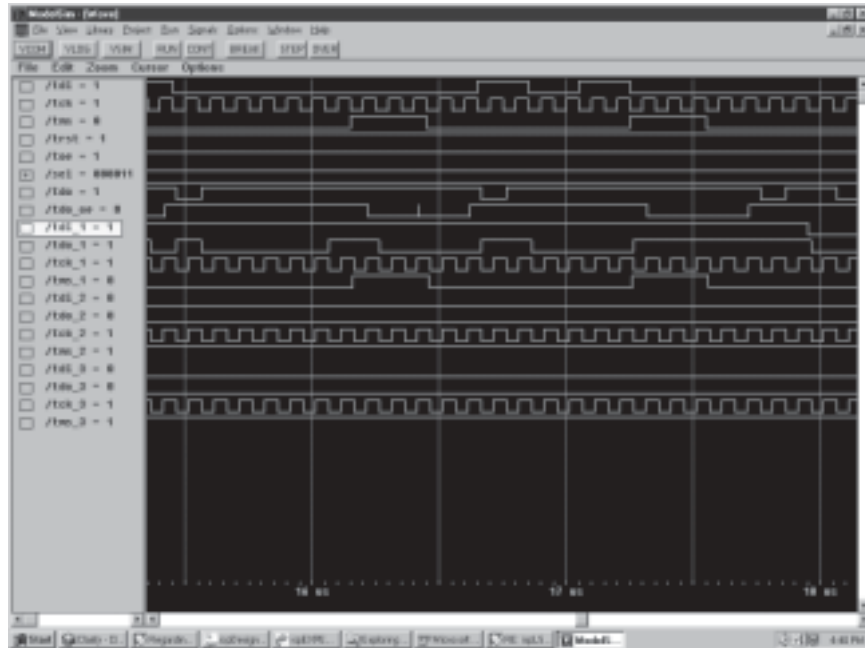
6. Park all local scan ports in Test-Logic-Reset by loading the SOFTRESET instruction in Shift-IR and then clocking TCK at least five times.



LSC BSCAN-1: IEEE 1149.1 Multiple Scan Port Addressable Buffer

Appendix (Continued)

7. Check the boundary scan register with LSP₁ unparked by loading the EXTEST instruction in Shift-IR and then shifting the data out in Shift-DR. Notice that the boundary scan data comes out TDO₁.



8. Check the boundary scan register with LSP₁ unparked by loading the SAMPLE/PRELOAD instruction in Shift-IR and then shifting the data out in Shift-DR. Notice that the boundary scan data comes out TDO₁.

