LSC BSCAN-2: Multiple Scan Port Linker

Introduction

According to the IEEE 1149.1 Boundary Scan System, every complex system can have more than one boundary scan compliant scan port. If each of these scan ports are linked together, then the chances of enhancing the scan capability would definitely increase. In this design, these multipe scan ports are linked together using a 4-bit Indentification Bus. The MSP (Multiple Scan Port) device can be used to link the four local scan ports or it can be completely bypassed. The four local scan ports or any combination of these four ports can be selected by entering the necessary data into the instruction and data registers.

Design Features

Functional Block Diagram

The MSP is comprised of four major logic blocks (Figure 1). The Port Control block is responsible for controlling the operation of the instruction register and data register. The instruction register and data register blocks shift and load one instruction register and three data registers. The scan port configuration block links any combination of the four secondary scan ports. The input signal 'ENABLE_MSP' is used as an output enable control signal for the MSP outputs associated with the four local scans. When low, the device outputs are tri-stated so a Lattice ispDOWNLOAD® Cable can be used directly on the secondary chains for in-system programming.

The value in any of the registers is loaded in such a way that the least significant bit (LSB) is the first to be shifted in closest to the TDO and the most significant one (MSB) is the last closest to TDI.

PIN LIST

The following pins are used:

MSPCLK (Multiple Scan Port Clock 1-4) – Used to output the buffered TCK to the Multiple Scan Ports.

MSPTDI 1:4 (Multiple Scan Port Test Data Input 1-4) – Each of these receives data serially from the associated TDO outputs of the MSP.

Figure 1. Functional Block Diagram

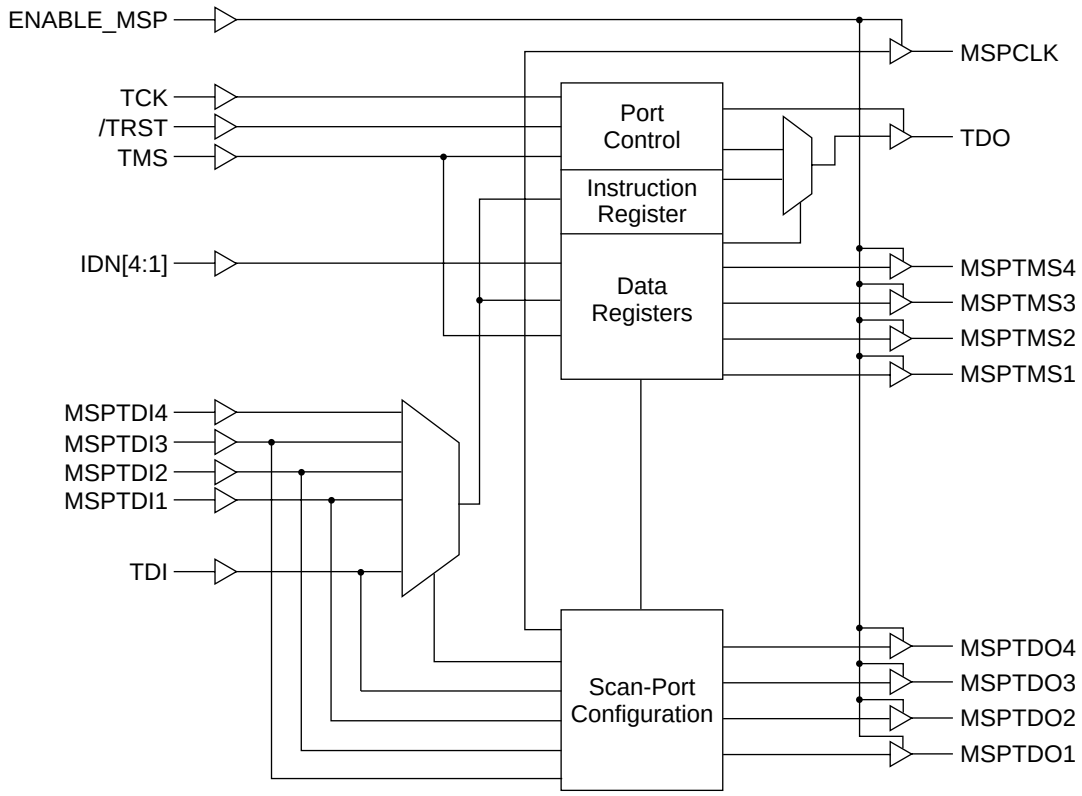


Figure 2. TAP Controller State Diagram

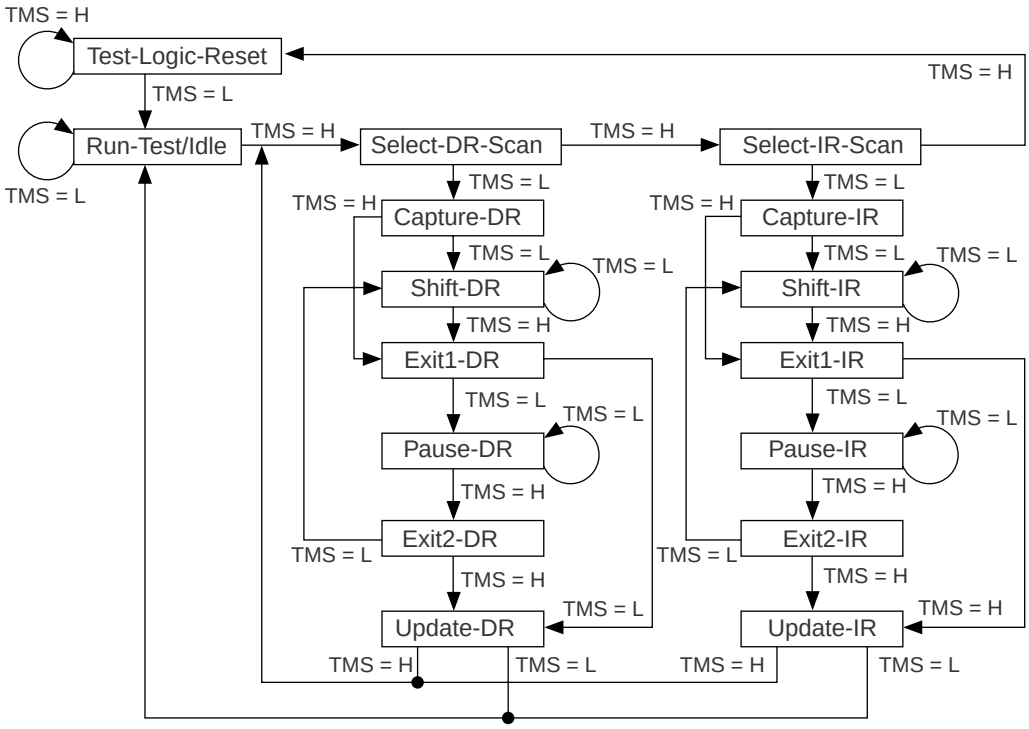


Table 1. Instruction Register Operation Codes

Bit Loaded	Value in Hex	Data Register	Instruction	Action Performed	Operation Mode
11111100	FC	ID Bus	SCANIDB	Scan ID	Normal
01111101	7D	ID Bus	READIDB	ID Bus Register Scan	Normal
01111110	7E	Select	SCANSEL	Select Register Scan	Normal
All Others		Bypass	BYPASS	Bypass Scan	Normal

Table 2. Instruction Register Default Status Word

IR Bit	Value
7	0
6	0
5	0
4	0
3	0
2	0
1	0
0	1

Table 3. Register Summary

Register Name	Length (Bits)	Function
Instruction	8	Holds the command instruction for the device
Select	8	Defines Local Scan Paths (LSP)
ID Bus	4	Holds subsystem indentification codes
Bypass	1	Removes the MSP device from the scan path

MSPTDO 1:4 (Multiple Scan Port Test Data Output 1-4) – These are the outputs from the MSPs to the TDI inputs.

MSPTMS 1:4 (Multiple Scan Port Test Mode Select 1-4) – These are configured through the Select register, to follow the TMS and put the MSPs through the TAP states.

IDN 1:4 (Identification 1-4) – These provide identification to the system under test.

TCK (Test Clock) – All operations are synchronous to the test clock. Inputs are captures at the rising edge and outputs change at the falling edge of the TCK.

TDI (Test Data Input) – This is a serial input used to get information into the selected data register and the instruction register.

TDO (Test Data Output) – IEEE Standard 1149.1

TMS (Test Mode Select) – IEEE Standard 1149.1

TRST (Test Reset) – IEEE Standard 1149.1

Enable_MSP – Enables outputs of the MSPs.

Port Control

The test port consists of three signals: TMS, TCK and TRST and includes a TAP controller that adheres to the IEEE Standard 1149.1 protocol. This port controls the operation of the circuit by issuing the proper control instructions to the data registers. The state diagram for the TAP controller is shown in Figure 2.

Instruction Register

The device is controlled by the instructions loaded into one 8-bit-wide serial shift register known as the Instruction Register. Data is shifted in via either the TDI pin or one of the MSPTDI pins, and out via the TDO pin.

Table 1 lists the instructions implemented in the MSP and the data register selected by each instruction. During the Capture-IR state, the default instruction is loaded (Table 2).

The operation of the MSP is dependent on the instruction loaded into the IR. Each instruction designates a data register to be placed between TDI or MSPTDI and TDO during the Shift-DR TAP state.

Data Registers

The following three registers are included in the Multiple Scan Port :

Select Register
ID Bus Register
Bypass Register

The data in each of these registers in loaded through TDI or MSPTDI serially and the outputs through TDO or MSPTDO.

Table 4. Select Register-Bit Controlling for MSPTMS and MSPTDO

Bit n	Bit n-1	MSPTMS	MSPTDO
0	0	H	Z
0	1	L	Z
1	X	TMS	Active

Note: n can be chosen as 1, 3, 5 or 7.

Select Register

The Select Register (SR) is an 8-bit serial register that determines which, if any, of the local scan paths (LSPs) will be included in the primary scan port. A reset operation forces all bits to zero. The register is divided into four 2-bit sections, each controlling one LSP. That is, bit 7,6 for LSP4, bit 5,4 for LSP3, bit 3,2 for LSP2, and bit 1,0 for LSP1. Table 4 shows the SR bit controlling for MSTMS and DTO.

The Select register is loaded with an 8-bit value. This value leads one or more MSPTMS pins to change to a static high or low level.The MSPTMS only assumes this level on the falling edge of the TCK in the Update-DR TAP state. The new value of the Select register forces the MSPTMS pin to follow TMS (by which the local scan port is selected). If one or more MSPTMS pins are in the follow TMS mode, then the transfer occurs only at the falling edge of the TCK in the Update-DR TAP state. The MSPTMS pin follows the TMS pin only if no other MSPTMS pin is selected at that time. The MSPTMS pin is forced low and it does so only at the falling edge of TCK in the Run-Test/Idle state. Hence, the TAP state should go from Update-DR to the Run-Test/Idle state when the LSP is selected.

Table 5. ID Bus Bit Mapping

Bit	Terminal Name	Signal Description
3	IDN4	Identification Bus Bit 4
2	IDN3	Identification Bus Bit 3
1	IDN2	Identification Bus Bit 2
0	IDN1	Identification Bus Bit 1

ID Bus Register

During the SCANIDB IR operation, the ID register is placed in the scan path and preloaded with data from the ID bus during the rising edge of TCK in the Capture-DR state.

During the READIDB IR operation, the ID register is placed in the scan port but is not preloaded in the Capture-DR TAP state.

Bypass Register (BR)

The Bypass Register is a 1-bit serial register where the MSP is removed from the primary scan port when it is not required. During the Bypass instruction, the BR is placed in the scan port and is preloaded with logic '0' during the Capture-DR TAP state.

Scan Port Selection

The bits in the Select Register are decoded and by doing this, it determines which of the local scan ports are included in the primary scan port. The MSP data flow is defined by the instruction register and the value in the Select register.

If no paths are selected then no LSPs are included in the primary scan port. TDI->MSP->TDO

If one of the LSPs are selected , then this LSP is placed in the primary scan port as follows :

TDI(1) -> LSP1->MSP->TDO

If multiple LSPs are selected, these LSPs are placed in the primary scan port then the scan port would be:

TDI(1)->LSP(1)->LSP3->MSP->TDO

The MSP will cause a delay of 1 bit from TDI or MSPTDI to MSTDO .

The local scan port selected depends on the value in the SR register. Table 6 shows how the SR register value is used to select the LSP .

Table 6. LSP Selection

SR BIT				
7	5	3	1	Local Scan Port Selected
0	0	0	0	None
0	0	0	1	LSP1
0	0	1	0	LSP2
0	0	1	1	LSP1, LSP2
0	1	0	0	LSP3
0	1	0	1	LSP1, LSP3
0	1	1	0	LSP2, LSP3
0	1	1	1	LSP1, LSP2, LSP3
1	0	0	0	LSP4
1	0	0	1	LSP1, LSP4
1	0	1	0	LSP2, LSP4
1	0	1	1	LSP1, LSP2, LSP4
1	1	0	0	LSP3, LSP4
1	1	0	1	LSP1, LSP3, LSP4
1	1	1	0	LSP2, LSP3, LSP4
1	1	1	1	LSP1, LSP2, LSP3, LSP4

Implementation

This MSP design has been implemented in a Lattice ispLSI 2064VE device. The ispLSI device families are ideally suited to high-speed controller and state machine intensive applications. This design uses about 93% of the device macrocells with 23 I/O pins. The operating frequency is 35MHz with the ispLSI 2064VE-100. The number of macrocells required varies depending on the addition of new functions and/or removal of unneeded features. The ispLSI 2064VE features In-System Programmability (ISP™) and can be programmed up to 10,000 times for design configuration.

The MSP design was designed and simulated in VHDL using Lattice design tools. After the design was completed, the VHDL code was compiled. The use of VHDL with a CPLD allows functional and hardware changes to be made quickly and easily.

When driving the backplane directly, buffers are needed for the ispLSI 2000VE device because of its limited drive.

Table 7. ispLSI 2064VE Pin Locations

Pin Name	Function	Pin Number
ENABLE_MSP	IN	5
VCC	SYS	6
TMS	IN	23
TCK	IN	26
TDO	OUT	9
TDI	IN	44
MSPTDO(1)	OUT	11
MSPTDO(2)	OUT	12
MSPTDO(3)	OUT	13
MSPTDO(4)	OUT	10
MSPCLK	OUT	16
GND	SYS	17
VCC	SYS	28
TRST	IN	29
MSPTDI(1)	IN	31
MSPTDI(2)	IN	14
MSPTDI(3)	IN	41
MSPTDI(4)	IN	32
IDN(1)	IN	24
IDN(2)	IN	34
IDN(3)	IN	1
IDN(4)	IN	20
MSPTMS(1)	OUT	35
MSPTMS(2)	OUT	38
MSPTMS(3)	OUT	15
MSPTMS(4)	OUT	33
GND	SYS	39

JEDEC File

The JEDEC file for this reference design targeting the ispLSI 2064VE-xxLT44 is available from your Lattice sales representative. This design supports a maximum TCK frequency of 35MHz when using the ispLSI 2064VE-100LT44 device. The pinout is shown in Table 7.

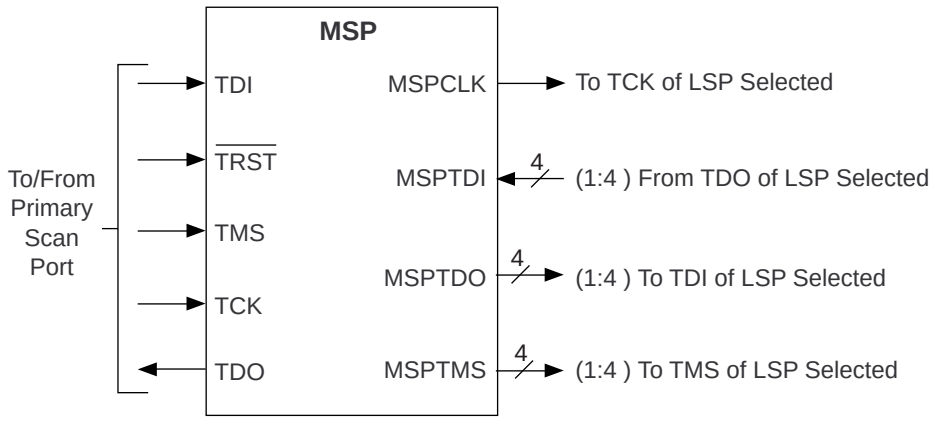
Ordering Information

TCKmax	JEDEC File OPN	Device OPN	Package
35MHz	LSC_BSCAN -2LT44	ispLSI 2064VE -100LT44	44-Pin TQFP

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-826-6002 (International)
e-mail: techsupport@latticesemi.com

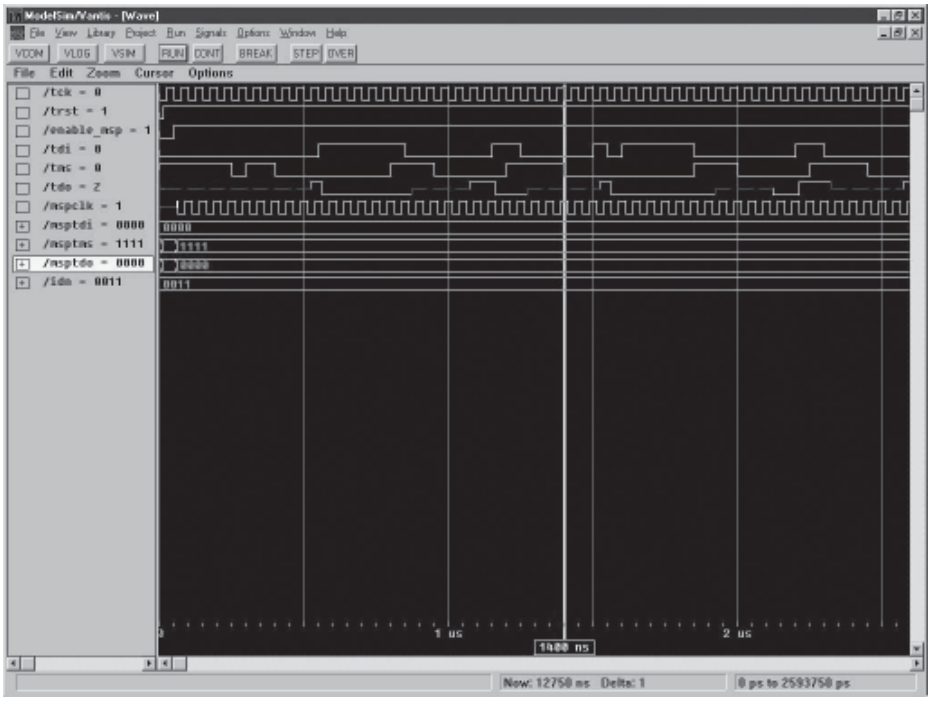
Figure 4. Application Example



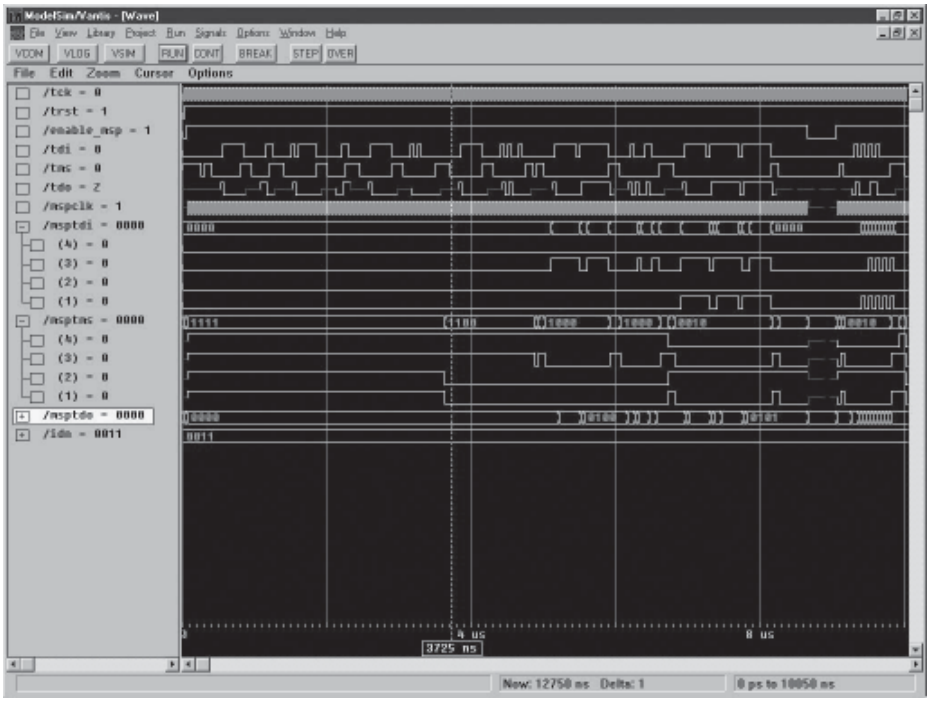
Appendix

Expected and Simulation Waveforms

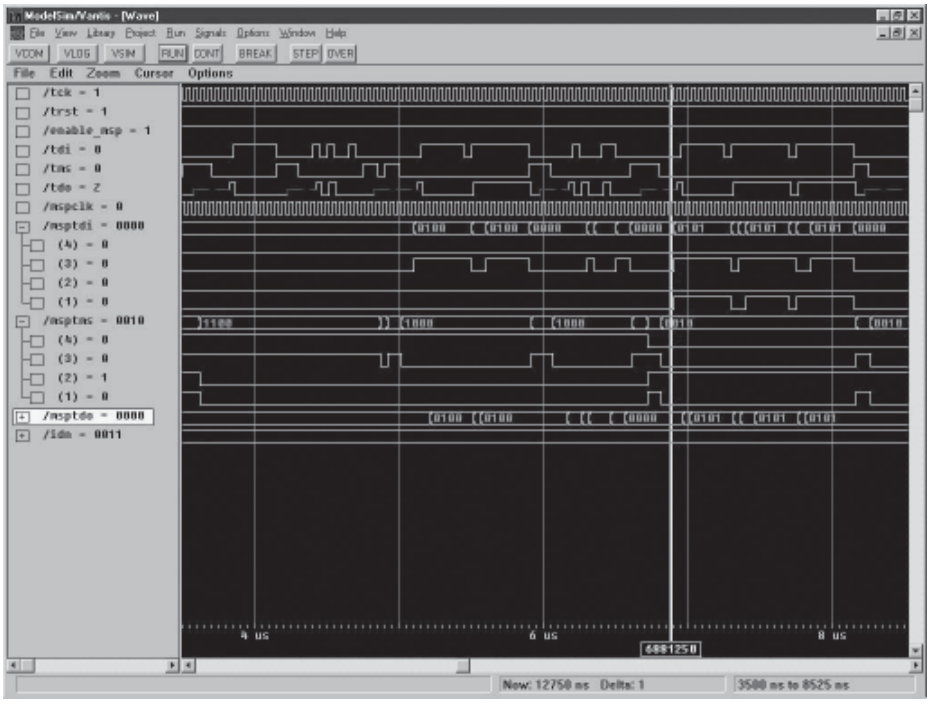
1. Receive ‘SCANIDB’ instruction and Scan IDN bus register (before 1400ns)
   Receive ‘READIDB’ instruction and Read IDN bus register (after 1400ns)



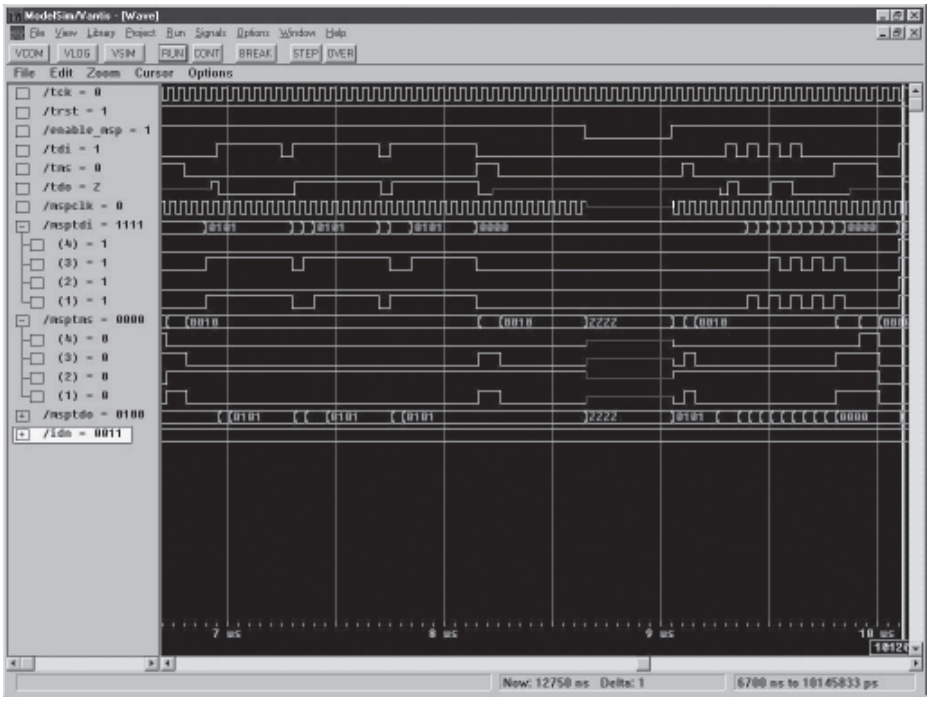
2. Receive ‘SCANSEL’ instruction and Scan select register with X”05” (before 7325ns)
   Receive ‘SCANSEL’ instruction and Scan select register with X”25” for selecting LSP3 (after 7325ns)



3. Receive ‘SCANSEL’ instruction and Scan select register with X”62” for selecting LSP1/LSP3 while LSP3 selected



4. Receive ‘SCANSEL’ instruction and Scan select register with X”AA” for selecting LSP1/LSP2/LSP3/LSP4 while LSP1/LSP3 selected. OE signal ‘ENABLE_MSP’ is off for a period of time during this section of test



5. Receive ‘BYPASS’ instruction for the chip while LSP1/LSP2/LSP3/LSP4 selected