

sysHSI SERDES Technology

Proven SERDES Leadership

Over the last several years designers have been challenged to obtain higher data rates, reduce PCB traces, reduce connectors, and reduce EMI emissions and susceptibility. SERDES technologies have become increasingly popular as a method to meet these challenges for chip-to-chip, board-to-board, and backplane applications.

“FPSC technology allowed NEC to place our custom backplane interface design in the programmable portion of the device, while utilizing the built-in SERDES channels provided in the embedded core of the ORT8850. Lattice FPSCs provide a distinct advantage over a discrete SERDES and FPGA solution.”

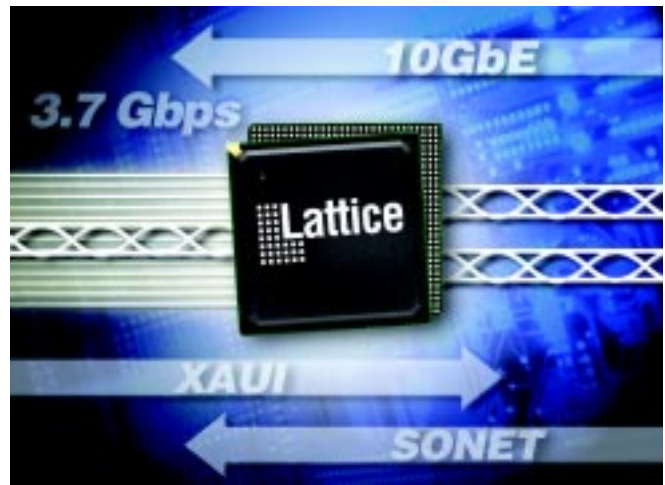
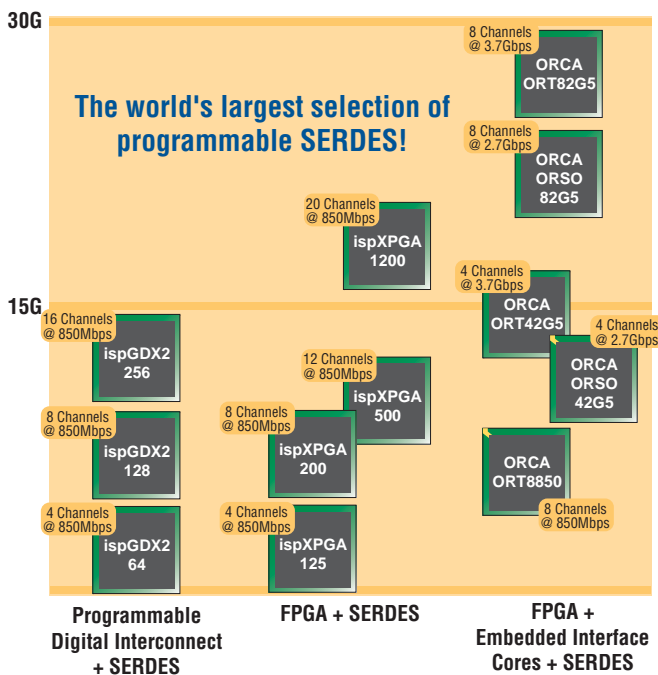
Shigeki Suyama, General Manager
NEC Corporation

Lattice has implemented sysHSI™ SERDES technologies in a variety of programmable products. High performance SERDES are integrated into Lattice’s Field Programmable System Chip (FPSC) devices. A cost effective SERDES is implemented in Lattice’s ispXPGA™ family of FPGAs and its ispGDX2 programmable interconnect family.

Lattice sysHSI SERDES technology leads the programmable logic industry in terms of maximum bit rate, low TX jitter, RX jitter tolerance and power consumption per channel. With sysHSI SERDES technology, Lattice products demonstrate the fastest bit rates and the longest error-free connections.

Lattice Programmable SERDES

Aggregate Bandwidth per Device



sysHSI SERDES Key Capabilities

- **Wide Range of Bandwidth Supported**
 - 126 Mbps to 3.7 Gbps
 - Roadmap to 10 Gbps
- **Low TX Jitter**
 - 0.17UI @ 3.125 Gbps
- **Excellent RX Jitter Tolerance**
 - 0.75UI @ 3.125 Gbps
- **Programmable Pre-emphasis (FPSCs)**
 - 0%, 12.5%, 25%
- **Robust High Speed**
 - Reliable transmission over:
 - 26 inches of FR4 at 3.7 Gbps
 - 40 inches of FR4 at 3.125 Gbps
 - 75 feet of co-axial cable at 622 Mbps
- **Low Power CMOS Operation**
 - <225 mW per channel at 3.125 Gbps
 - <50 mW per channel at 622 Mbps
- **Choice of Programmable Fabric**
 - ispGDX® – Programmable digital interconnect
 - ispXPGA – FPGA
 - FPSC – FPGA + embedded interface core
- **Support For Multiple Standards**
 - XAUI, Fibre channel, Gigabit Ethernet, SONET

“Lattice’s ORSO82G5 FPSC technology allows our Zeus™ grooming switch to seamlessly interface with existing and emerging SONET line cards, thus preserving the carrier’s enormous investment made in SONET-based systems.”

Bill Woodruff, VP of Marketing
Velio Communication

SERDES Solutions

High Performance SERDES Solutions

Lattice has integrated high performance SERDES into five of its ORCA® FPSC (Field Programmable System Chip) devices for use in a variety of communications applications. Key features of these SERDES include:

- High bit rates up to 3.7 Gbps
- TX jitter as low as 0.17UI at 3.125 Gbps
- RX jitter tolerance up to 0.75UI at 3.125 Gbps
- Power per channel \leq 225 mW at 3.125 Gbps

Lattice's high performance SERDES is available on the ORT82G5, ORT42G5, ORSO82G5, ORSO42G5, and ORT8850 FPSC devices.



Interoperability

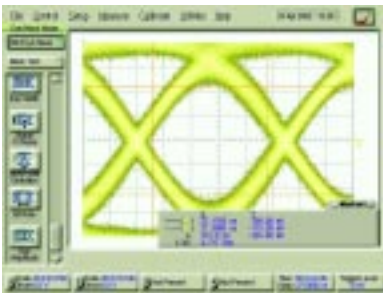
Designers may successfully use Lattice's sysHSI SERDES in conjunction with a variety of other SERDES implemented in a standard chip or ASIC. To date, interoperability has been demonstrated between Lattice SERDES and devices from Velio, AMCC and Agere.



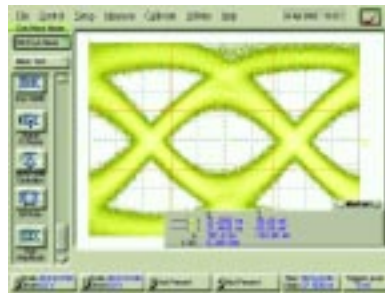
Typical SERDES evaluation test setup for Lattice devices.

Superior SERDES Performance

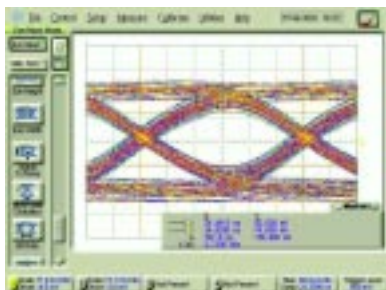
Lattice sysHSI SERDES technology leads the programmable logic industry in terms of maximum bit rate and low jitter. The following actual eye diagrams illustrate the outstanding characteristics of Lattice's sysHSI SERDES technology.



ORT82G5 RX Eye Diagram over 26 inches (65 centimeters) of FR4 at 3.7 Gbps



ORT82G5 RX Eye Diagram over 40 inches (100 centimeters) of FR4 at 3.125 Gbps



ORSO82G5 RX Eye Diagram over 30 inches (75 centimeters) of FR4 at 2.7 Gbps

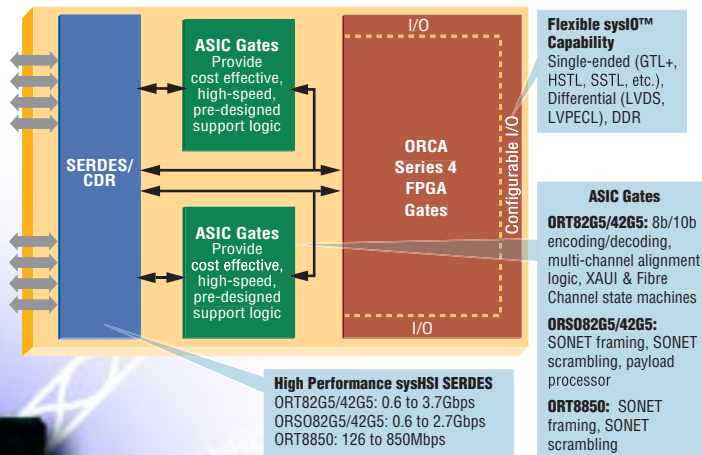


ORT82G5/42G5 FPGAs with Embedded Core

3.7 Gbps SERDES + XAUI / Fibre Channel + FPGA

ORT82G5 and ORT42G5 devices provide eight or four high performance SERDES, respectively. Standard compliance and on-chip link state machines make these devices ideal for implementing XAUI, 10 Gbps Ethernet and Fibre Channel links in chip-to-chip and backplane applications.

FPSC Block Diagram



ORS082G5/42G5 FPGA with Embedded Core

2.7Gbps SERDES + SONET Framing + FPGA

ORS082G5 and ORSO42G5 devices include eight or four high performance SERDES, respectively. Coupled with on-chip SONET framing, these device provide an excellent SONET-based solution for implementing chip-to-chip or backplane applications.

ORT8850 FPGA with Embedded Core

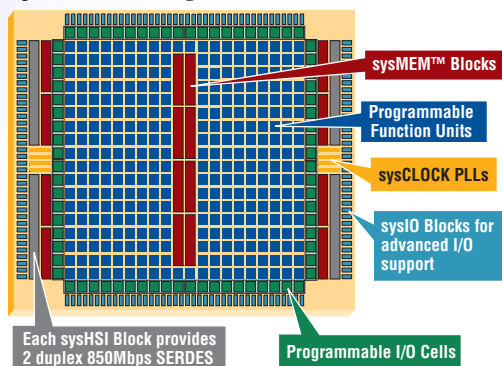
850Mbps SERDES + SONET Framing + FPGA

The ORT8850 includes eight 850Mbps SERDES channels plus on-chip SONET framing. The ORT8850 provides an alternative to Ethernet technology for implementing chip-to-chip or backplane applications.

Cost Effective SERDES Solutions

Lattice has developed its most cost effective SERDES for use in a variety of chip-to-chip, board-to-board, and backplane applications where a moderate speed SERDES is required. This SERDES is available on the ispXPGA and ispGDX2 devices.

ispXPGA Block Diagram

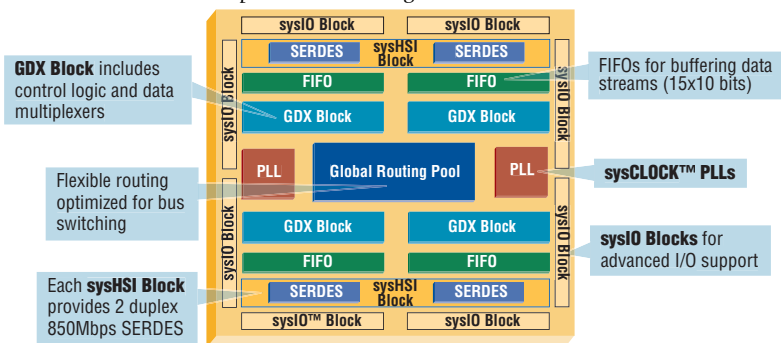


ispXPGA FPGA

Up to 20 x 850 Mbps SERDES + FPGA

The ispXPGA family couples an ispXP™ (ISP™ eXpanded Programmability) based FPGA with up to 20 SERDES channels. With ispXP technology, the ispXPGA family provides infinite reconfigurability through SRAM technology and the benefits of instant-on, security, and a single chip solution through E²CMOS® non-volatility.

ispGDX2 Block Diagram



ispGDX2 - Programmable Interconnect

Up to 16 x 850 Mbps SERDES + Interconnect

The ispGDX2 family provides cost effective SERDES solutions at less than \$2.00 per channel for high volume applications. These SERDES are coupled with a multiplexer-based programmable interconnect and switching fabric and flexible I/Os. Many designers use the ispGDX2 device as a universal parallel-to-serial converter.

sysHSI SERDES Enabled Devices

	High Performance SERDES				Cost Effective SERDES	
	ORT82G5 / 42G5	ORS082G5 / 42G5	ORT8850H	ORT8850L	ispXPGA	ispGDX2
Data Rate per Channel	3.7 – 0.6 Gbps	2.7 – 0.6 Gbps	850 – 126 Mbps	850 – 126 Mbps	850 – 400 Mbps	850 – 400 Mbps
# of Channels	8 / 4	8 / 4	8	8	4 – 20	4 – 16
SERDES I/O	CML	CML	LVDS	LVDS	LVDS	LVDS
TX Jitter	0.17UI	0.16UI	0.25UI	0.25UI	0.25UI	0.25UI
RX Jitter	0.75UI	0.79UI	0.6UI	0.6UI	0.4UI	0.4UI
On-Chip Termination	Yes	Yes	Yes	Yes	No	No
Pre-emphasis Settings	25, 12.5, 0%	25, 12.5, 0%	—	—	—	—
Power / Channel	225 mW	225 mW	50 mW	50 mW	65 mW	65 mW
Encoding Support	8b/10b	SONET	SONET	SONET	10b/12b 8b/10b*	10b/12b 8b/10b*
Standards Support	XAUI, Fibre Channel Gigabit Ethernet	SONET-based SERDES links	SONET-based SERDES links	SONET-based SERDES links	Proprietary SERDES links	Proprietary SERDES links
FPSC Functionality	8b/10b encoding XAUI & Fibre channel link state machines, multi-channel alignment	Pseudo-SONET Framing, TOH insertion/extraction multi-channel alignment, payload cell processor	Pseudo-SONET Framing, TOH insertion/extraction multi-channel alignment, pointer mover	Pseudo-SONET Framing, TOH insertion/extraction multi-channel alignment, pointer mover	—	—
Programmable Section	10,368 LUTS 643K Gates 372 / 204 I/O	10,368 LUTS 643K Gates 372 / 204 I/O	16,192 LUTS 899K Gates 297 I/O	4,992 LUTS 397K Gates 278 I/O	1.9K – 15.3K LUTS 125K – 1.2M Gates 176 – 496 I/O	ispGDX2 multiplexer and interconnect fabric
Typical Programmable Functions	Bridging, proprietary packet processing	Bridging, proprietary packet processing	Bridging, proprietary packet processing	Bridging, proprietary packet processing	PCI, SDRAM interface, Utopia interface	Multiplexer

* Bit alignment. 8b/10b encoding/decoding must be implemented outside of the sysHSI block.

Serial Standards Quick Reference

Specification	Fibre Channel	Infiniband	SFI-5	XAUI	Lattice ORT82G5
Baud Rate	1.0625 Gbps	2.5 Gbps	2.5 Gbps	3.125 Gbps	3.125 Gbps
TX Total Jitter	0.65UI	0.35UI	0.35UI	0.35UI	0.17UI
RX Jitter Tolerance	0.70UI	0.65UI	0.65UI	0.65UI	0.75UI

More Information on Lattice's sysHSI SERDES Technology

Lattice offers a wide range of SERDES related data sheets, technical notes, application notes, and the new SERDES Handbook. These technical documents are available from your local Lattice representative or you may download them from the Lattice website at www.latticesemi.com.



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