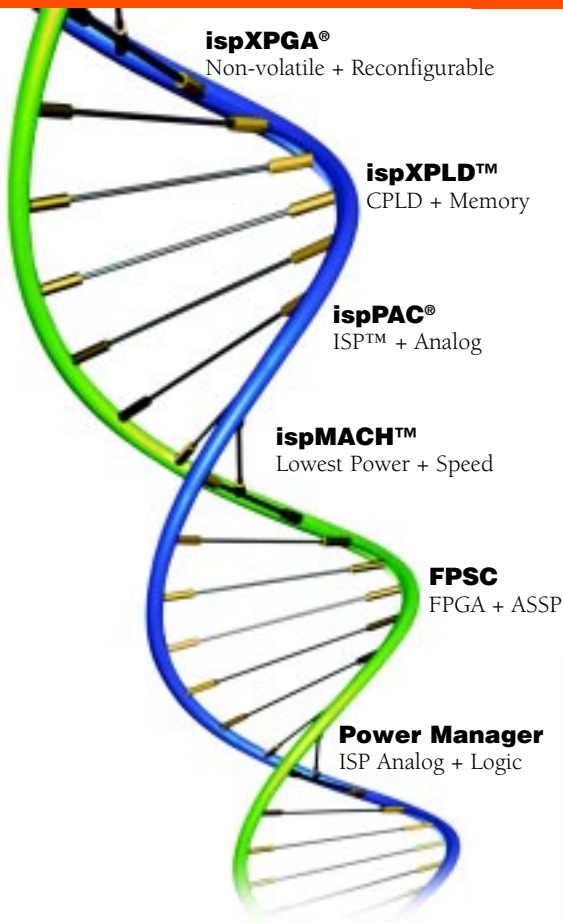


Bringing the Best Together **Lattice Solutions**



Bringing the Best Together



Today's leading-edge system designers have to satisfy multiple and often competing goals. Designers must balance speed, low power consumption, high functionality, board-space savings, cost, and fast time-to-market.

Lattice Semiconductor brings together a variety of technologies and features to provide innovative solutions that address the real needs of designers. This approach has been adopted across the range of products that Lattice supplies. In silicon products this spans logic, interface, and analog. In design tools it covers design entry, intellectual property and development tools.

Lattice's product portfolio includes the world's fastest programmable logic devices (2.3 ns pin-to-pin delay), the lowest power consumption (20 μ A max. static ICC), the world's only non-volatile, infinitely reconfigurable FPGAs (Field Programmable Gate Arrays), the fastest programmable SERDES (3.7 Gbps per channel), and programmable mixed signal devices.

Lattice consistently brings the best together to deliver innovative, high-performance, programmable solutions.

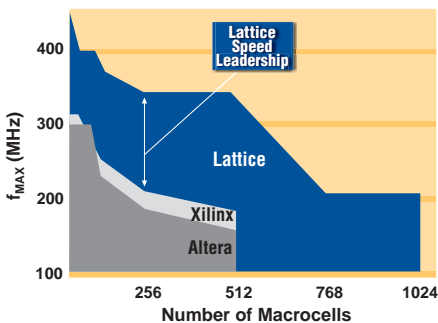
Lattice Exceeding Design Requirements

- ✓ Highest Speed Logic
- ✓ Highest Performance I/Os
- ✓ Complex Functions
- ✓ Lowest Power Dissipation
- ✓ Smallest Footprint
- ✓ Mixed Signal Capability
- ✓ Lower Cost
- ✓ Faster Time-to-Market

Performance Leadership

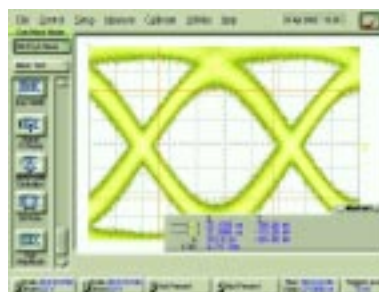
Lattice delivers the world's highest performance programmable logic devices.

- ispMACH 4000 – 2.5 ns / 400 MHz
- ispGAL®22V10 – 2.3 ns / 455 MHz



Superior SERDES Solutions

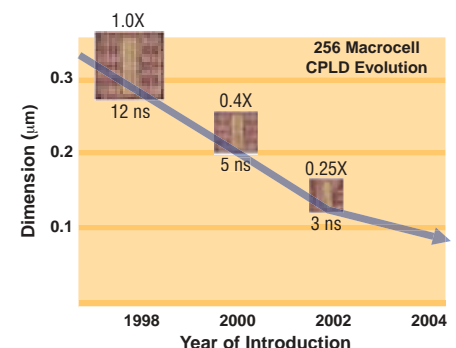
Lattice sysHSI™ (system high-speed interface) serializer/deserializer (SERDES) technology leads the programmable logic industry in terms of maximum bit rate and low jitter. The following actual eye diagram illustrates the outstanding characteristics of Lattice's sysHSI SERDES technology.



ORT82G5 RX Eye Diagram over 26 inches (65 centimeters) of FR4 at 3.7 Gbps

Technology Leadership

Through the development of products utilizing advanced manufacturing processes, Lattice delivers higher speed and lower cost solutions to the marketplace. Current developments are focused on 0.13 μ m and 90 nm technology.

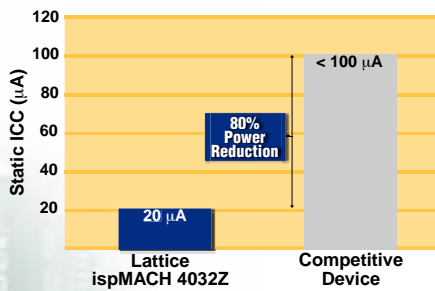




Ultra Low Power

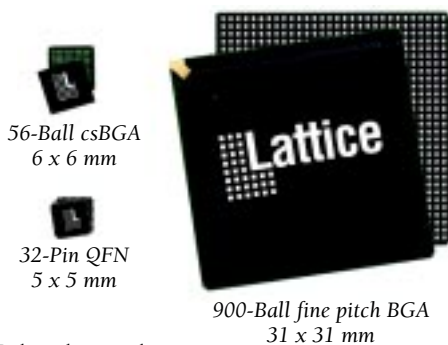
Lattice delivers the world's lowest power programmable logic devices.

- ispMACH 4000Z – 20 μ A (max.)
- ORCA® FPSC – 225 mW per SERDES Channel @ 3.125 Gbps



Advanced Packaging

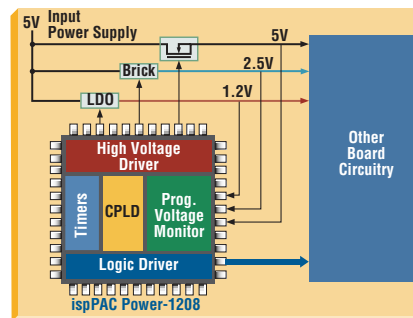
Lattice utilizes a variety of advanced packaging technologies that allow designers to increase functional density. Lattice offers TQFP, csBGA (0.5 mm) caBGA (0.8 mm), and fpBGA (1.0 mm) packaging – including thermally enhanced options. Current developments include packages ranging from the space-saving QFN to 1000+ ball BGA packages.



Packages shown actual size.

Programmable Analog

Today's system designs contain analog signals which must be monitored and processed. Lattice's innovative ispPAC family of programmable analog devices offers an excellent solution for signal conditioning, filtering and control loop applications. The ispPAC Power Manager combines programmable analog and digital providing an optimized power sequencing and monitoring solution.



Faster Time to Market

Programmable devices provide fast time-to-market. Lattice facilitates the design process by supporting users with easy-to-use ispLEVER® tools, IP cores, on-time delivery, a global network of field applications engineers, and over 20 years of experience in programmable products.



Lattice Products

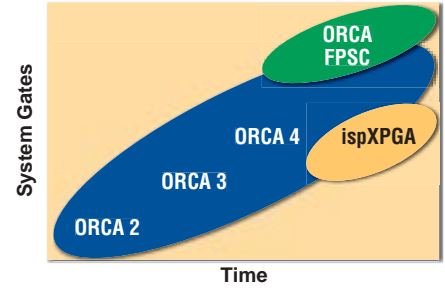
Logic Devices	Page
ORCA Series 4 SRAM-based FPGAs	4
ispXPGA Non-volatile, reconfigurable FPGAs	5
ispXPLD 5000MX High-density CPLD plus memory	8
ispMACH 4000 Highest speed, lowest power CPLDs	9
ispPAC Power Manager Programmable analog + logic	10
SERDES Interface Devices	
ORT82G5 8 x 3.7 Gbps SERDES + FPGA	6
ORT42G5 4 x 3.7 Gbps SERDES + FPGA	6
ORSO82G5 8 x 2.7 Gbps SERDES + SONET + FPGA	6
ORSO42G5 4 x 2.7 Gbps SERDES + SONET + FPGA	6
ORT8850H/L 8 x 850 Mbps SERDES + SONET + FPGA	6
ispGDX2™ Programmable SERDES + interconnect	7
Source Synchronous Interface Devices	
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FPGA Products

Lattice Field Programmable Gate Arrays

The ispXPGA (in system programmable eXpanded field Programmable Gate Array) family of devices allows the creation of high-performance logic designs that are both non-volatile and infinitely reconfigurable. Other FPGA solutions force a compromise, being either re-programmable, or reconfigurable, or non-volatile. Lattice's ispXPGA family offers all these capabilities with a mainstream architecture containing the features required for today's system-level design.



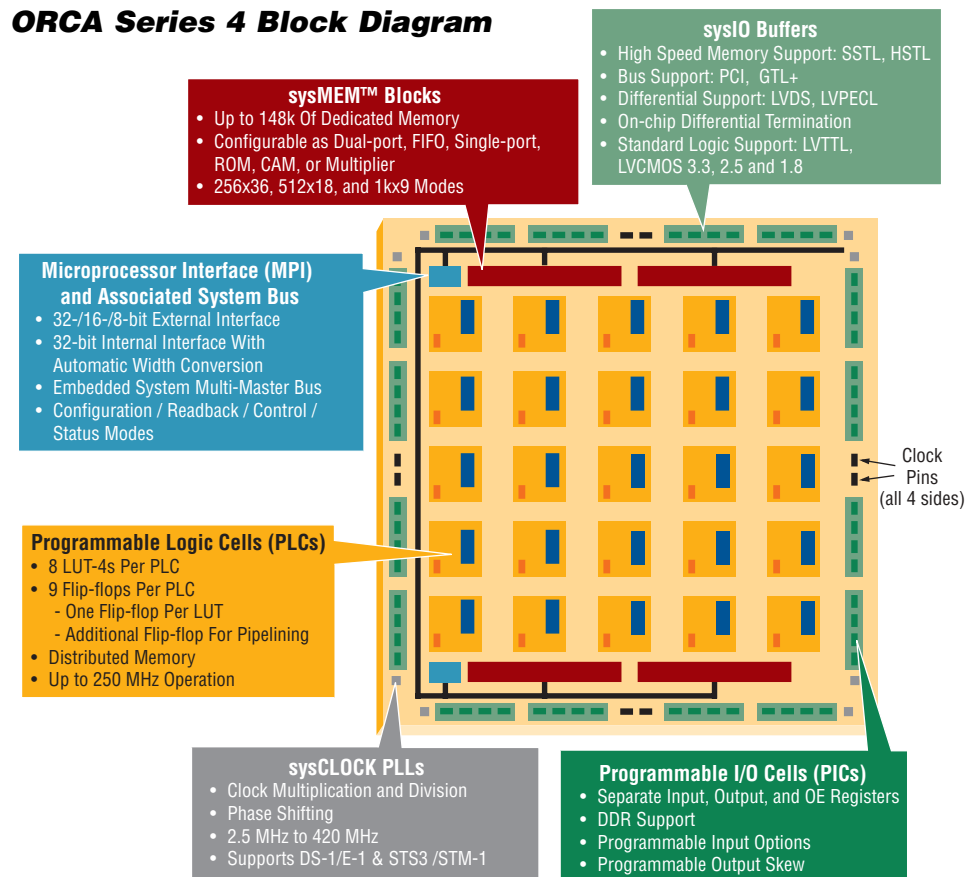
ORCA Series 4 FPGAs by Lattice Semiconductor are built on the familiar Optimized Reconfigurable Cell Array (ORCA) architecture. This FPGA device family offers many new features and architectural enhancements not available in any earlier FPGA generations. Bringing together highly flexible SRAM-based programmable logic, powerful system features, a rich hierarchy of routing and interconnect resources, and meeting multiple interface standards, the ORCA family of FPGAs accommodates the most complex and high-performance design challenges.



ORCA Series 4 Family

- High Performance FPGA
 - Up to 900k system gates
 - Up to 466 user I/Os
 - Up to 148k embedded memory
 - 250 MHz performance
- Flexible Programmable Logic Cells (PLCs)
- sysIO™ Capability for High Performance Interfacing
- Block and Distributed Memory
- sysCLOCK™ PLLs for Clock Management
 - 6 general purpose PLLs
 - 2 communication specific PLLs
- System-level Design Features
 - Embedded Microprocessor Interface (MPI)
 - Embedded system bus (ARM AHB bus)

ORCA Series 4 Block Diagram



ORCA Series 4 Family of FPGAs

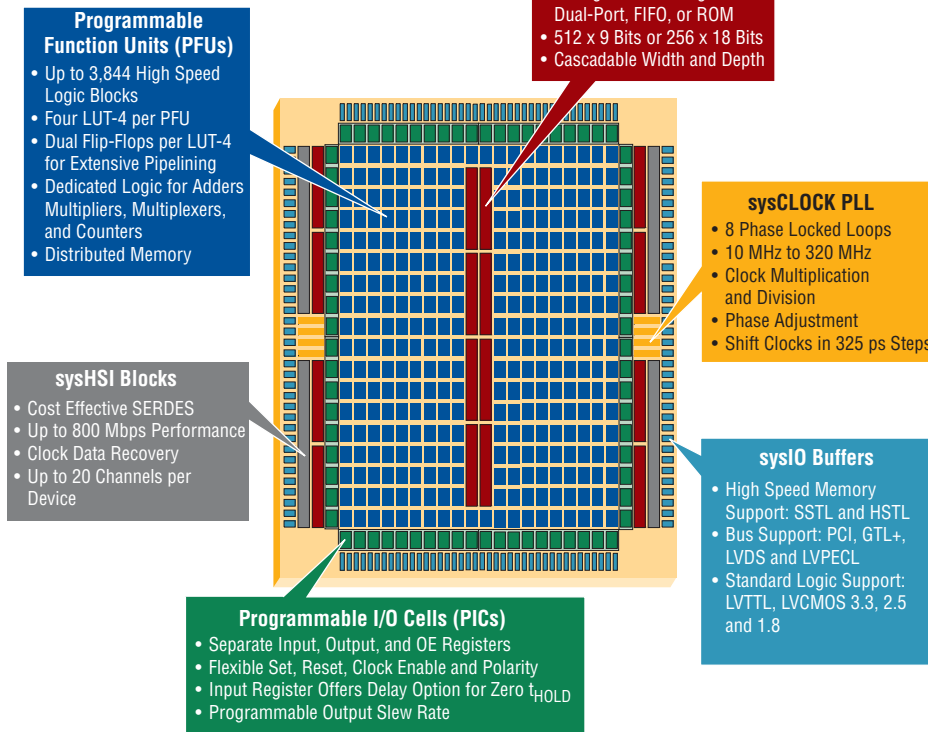
Device	System Gates	LUT-4	Total Registers	EBR RAM Blocks	EBR RAM Bits	Distributed RAM Bits	PLLs	User I/O
OR4E02	397k	5.0k	6.8k	8	74k	80k	8	405
OR4E04	643k	10.4k	13.4k	12	111k	166k	8	466
OR4E06	899k	16.2k	20.4k	16	148k	259k	8	466

ispXPGA Family

- ispXP™ Programming Technology Provides Non-volatility and Infinite Reconfigurability
 - Instant availability of logic at power-up
 - Single chip solution
 - Secure
- High-Performance FPGAs
 - Up to 1.25M system gates
 - Up to 496 I/Os
 - Up to 414k embedded memory
- High Performance Logic Blocks (PFUs)
- Block and Distributed Memory
- sysCLOCK PLLs for Clock Management
- sysIO Capability for High Performance Interfacing
 - Hot socketing support
 - Leave alone I/O – holds pin state during programming
- Two Options Available
 - High performance sysHSI (standard part number)
 - Low cost, no sysHSI (“E” series)
- sysHSI for 800 Mbps Serial Communication



ispXPGA Block Diagram



ispXP Offers Unique Set of Advantages

New ispXPGA and ispXPLD Families are Infinitely Reconfigurable and Non-volatile

Lattice offers an innovative new programming technology referred to as ispXP, for In-System Programmable eXpanded Programming. Previous programmable logic technologies have typically been either non-volatile EEPROM based or reconfigurable SRAM based. Because both these technologies provide unique benefits, Lattice decided to combine them in ispXP. This provides users, for the first time, with the benefits of non-volatility, including instant-on, single chip solutions, and high-security, with the infinite reconfigurability of SRAM technology.

- Single chip solution
- Instant-on – PLD logic available within microseconds of power-up (less than 200 μS)
- ispXP devices include security bits to prevent unauthorized readback
- No external bitstream



ispXPGA Family of FPGAs

Family Member	System Gates	LUT-4	Total Registers	EBR RAM Blocks	EBR RAM Bits	Distributed RAM Bits	SERDES Channels* (800Mbps)	PLLs	User I/O
ispXPGA 125/E	139k	1.9k	4.4k	20	92k	30k	4	8	176
ispXPGA 200/E	210k	2.7k	6.0k	24	111k	43k	8	8	208
ispXPGA 500/E	476k	7.0k	15.1k	40	184k	112k	12	8	336
ispXPGA 1200/E	1.25M	15.3k	32.2k	90	414k	246k	20	8	496

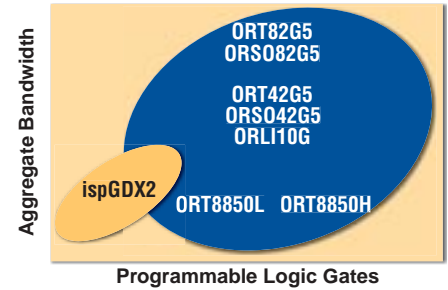
*"E" series does not support sysHSI.



Interface Products

Lattice Field Programmable System Chips and ispGDX2 Products

Lattice offers the world's fastest programmable interface products. Lattice Semiconductor pioneered the approach of putting ASIC macrocells and FPGA gates on the same silicon die. We call this a Field Programmable System Chip (FPSC). The embedded macrocells hold industry-standard Intellectual Property - bus interface, high-speed line interface, and high-speed transceiver cores. When these macrocells are combined with hundreds of thousands of programmable gates they can be used in a variety of advanced system designs.

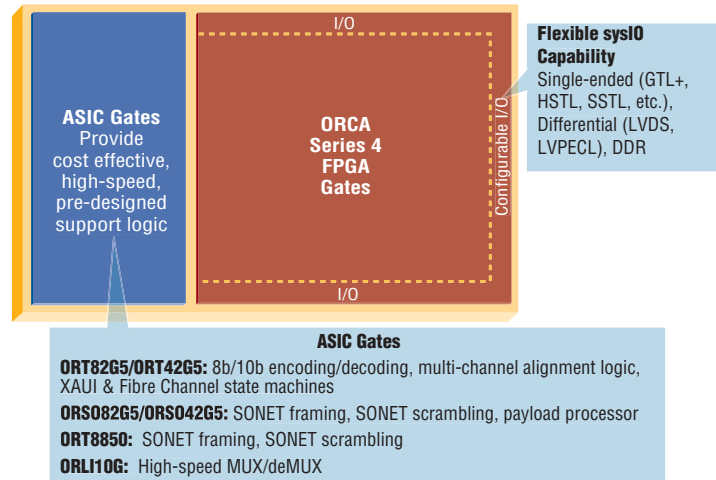


In addition to the innovative FPSC products, Lattice delivers the high-speed line of ispGDX2 (in-system programmable Generic Digital Crosspoint) bus switching and interface products. These flexible devices offer low-cost SERDES solutions and high-performance bus switching.

Lattice FPSC Families

- High Performance ORCA Series 4 based Field Programmable System Chips
- FPSC Functions
 - High-speed line interface
 - Programmable backplane transceiver
 - Serial backplane driver
 - SONET backplane transceiver
- sysCLOCK PLLs for Clock Management
- sysIO Capability for High Performance Interfacing
 - On-chip differential termination
- MPI and System Bus for Easy Connection to Microprocessor

FPSC Block Diagram

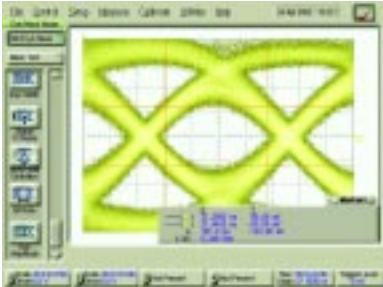


FPSC Interface Devices

FPSC Device	Data Rate per Channel	SERDES Channels	Encoding Support	Standards Support	FPSC Functionality	FPGA Core
ORT82G5 / ORT42G5	3.7 – 0.6 Gbps	8 / 4	8b/10b	XAUI Fibre Channel, Gigabit Ethernet	8b/10b encoding XAUI & Fibre channel link state machines, multi-channel alignment	10,368 LUTS 643K Gates 372 / 204 I/O
ORS082G5 / ORS042G5	2.7 – 0.6 Gbps	8 / 4	SONET	SONET-based SERDES Links	Pseudo-SONET framing, TOH insertion/extraction, multi-channel alignment, payload cell processor	10,368 LUTS 643K Gates 372 / 204 I/O
ORT8850H	850 – 126 Mbps	8	SONET	SONET-based SERDES Links	Pseudo-SONET framing, TOH insertion/extraction, multi-channel alignment, pointer mover	16,192 LUTS 899K Gates 297 I/O
ORT8850L	850 – 126 Mbps	8	SONET	SONET-based SERDES Links	Pseudo-SONET framing, TOH insertion/extraction, multi-channel alignment, pointer mover	4,992 LUTS 397K Gates 278 I/O
ORL10G	850 – 622 Mbps	–	–	OIF XSBI, OIF SFI-4	High speed MUX/deMUX	10,368 LUTS 643K Gates 316 I/O

Superior SERDES Performance

Lattice sysHSI SERDES technology leads the programmable logic industry in terms of maximum bit rate and low jitter. The following eye diagram illustrates the outstanding characteristics of Lattice's sysHSI SERDES technology.



ORT82G5 RX Eye Diagram over 40 inches (100 centimeters) of FR4 at 3.125 Gbps

Lattice FPSC Devices

ORT82G5 and ORT42G5

The ORT82G5 provides eight 3.7 Gbps SERDES. Standard compliance and on-chip link state machines make it ideal for implementing XAUI, 10 Gbps Ethernet and Fibre Channel links in chip-to-chip or backplane applications. The ORT42G5 offers four SERDES channels instead of eight.

ORT8850

The ORT8850 includes eight 850 Mbps SERDES channels plus on-chip SONET framing. The ORT8850 provides an alternative to Ethernet technology for implementing chip-to-chip or backplane applications.

ORSO82G5 and ORSO42G5

The ORSO82G5 includes eight 2.7 Gbps SERDES coupled with on-chip SONET framing. The ORSO82G5 provides an excellent SONET-based solution for chip-to-chip or backplane applications. The ORSO42G5 offers four SERDES channels instead of eight.

ORLI10G

The ORLI10G provides a high-speed line interface with a flexible FPGA logic core. The ORLI10G can be used as the interface in a variety of emerging networks, including 10 Gbps SONET/SDH (OC-192/STM-48), 10 Gbps optical transport networks (OTN) using digital wrapper and strong FEC, or 10 Gbps Ethernet.

ispGDX2 Family of Digital Cross Point Switches

ispGDX2 Features & Benefits

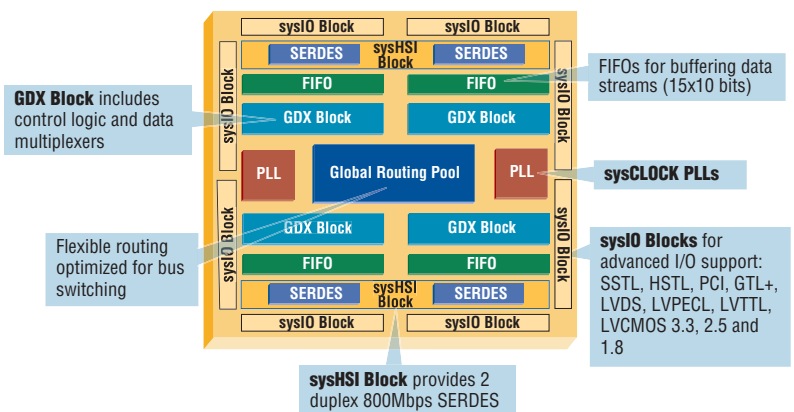
- **High Performance Bus Switching**
 - Up to 38 Gbps
 - Up to 16 (15x10) FIFOs for data buffering
 - I/O intensive: 64 to 256 I/Os
- **sysCLOCK PLLs for Clock Management**
 - Frequency synthesis and skew management
 - Clock shifting, multiply and divide capability
 - Jitter as low as 150 ps
- **sysIO Capability for High Performance Interfacing**
 - Hot socketing support
 - Leave alone I/O – holds pin state during programming
- **Up to 16 Channels of 800 Mbps sysHSI SERDES**
 - Serializer/de-serializer (SERDES) included
 - Built-in Clock Data Recovery (CDR)
 - 10b/12b and 8b/10b support
- **Flexible Programming & Testing**

* Bandwidth assumes 50% of I/Os are inputs and 50% are outputs.

ispGDX2 Families

Family Member	I/Os	GDX Blocks	Fmax	Bandwidth	Data Rate Per Channel	Bus LVDS (Pairs)	PLLs
ispGDX2-64	64	4	360 MHz	11 Gbps	400–800	32	2
ispGDX2-128	128	8	330 MHz	21 Gbps	400–800	64	2
ispGDX2-256	256	16	300 MHz	38 Gbps	400–800	128	4

ispGDX2 Block Diagram



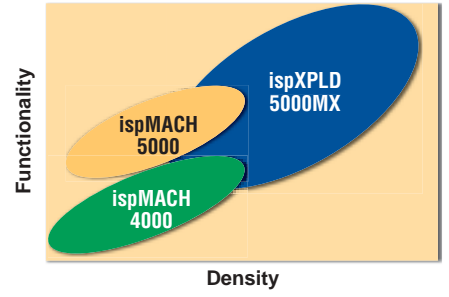


CPLD Products

Lattice ispXPLD and ispMACH CPLDs

Through its optimized portfolio of CPLDs, Lattice provides products a generation ahead of other CPLD solutions. These architectures are optimized to fit a variety of CPLD design challenges. This contrasts to the "one size fits all" approach of other CPLD vendors.

- SuperFAST™ Performance Leadership - Up to 400 MHz
- Zero Power CPLD - As low as 20 µA max. Standby Current
- SuperBIG™ Density Leadership - Up to 1024 macrocells
- SuperWIDE™ Logic - 68-input logic blocks
- Multi-Function Block (MFB) Architecture combines memory, CAM and FIFO with logic



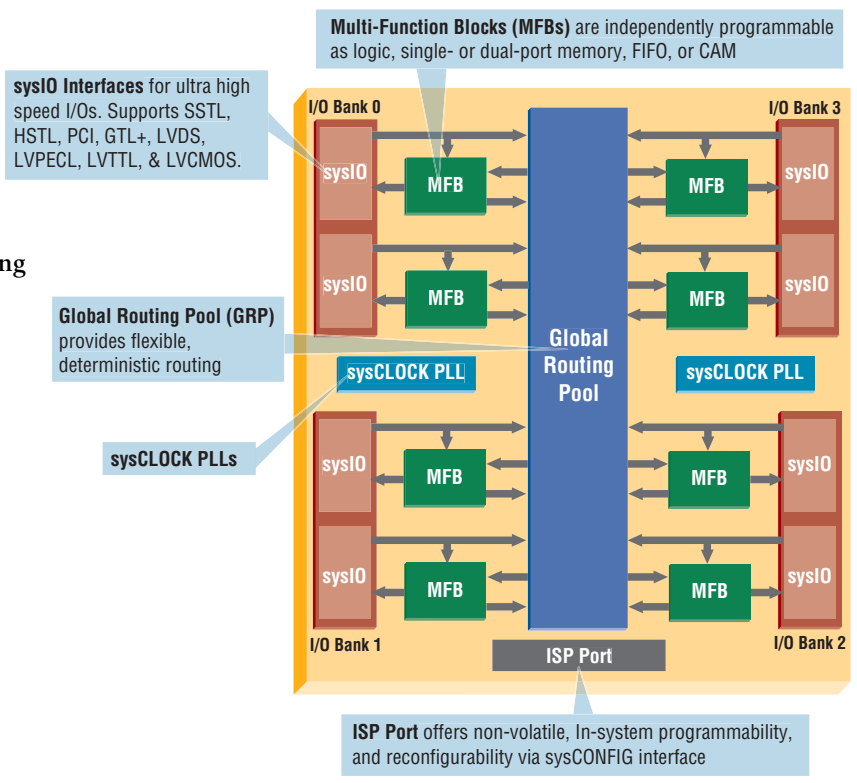
Lattice pioneered the ispMACH 5000 architecture delivering SuperWIDE performance with 68 logic inputs and easy implementation of complex logic functions in a single level of logic. The new ispXPLD 5000MX family combines memory with Lattice's SuperWIDE architecture and SuperBIG density. The ispXPLD 5000MX family represents a new class of devices called eXpanded Programmable Logic Devices (XPLDs). These devices are built around a new building block, the Multi-Function Block (MFB). MFBs can be individually configured as SuperWIDE (136-input) logic, single- or dual-port memory, FIFO, or CAM depending on the application. This architecture delivers the ultimate PLD flexibility through ispXP.

Lattice's ispMACH 4000 family is built on the industry's most advanced non-volatile CMOS process and delivers SuperFAST system performance for logic functions up to 36 inputs. The ispMACH 4000Z offers the industry's lowest power for handheld and other power-sensitive applications. Lattice's ispMACH 4000 family brings together high speed, low power and low cost to deliver the best solutions for a broad range of applications. Lattice's CPLD product portfolio offers commercial, industrial, automotive, and military grade devices.

ispXPLD 5000MX Features and Benefits

- Flexible MFB Architecture
 - SuperWIDE logic, SuperBIG density
 - Arithmetic support
 - Single- or Dual-Port RAM
 - Asynchronous FIFO
 - Ternary CAM
- sysCLOCK PLLs for Clock Management
- sysIO Capability for High Performance Interfacing
 - Leave alone I/O – holds pin state during programming
 - 5V tolerant inputs & I/Os
- In-system eXpanded Programming (ispXP)
 - Instant-on capability
 - Single chip convenience
 - ISP via IEEE 1532 Interface
 - Infinitely reconfigurable via IEEE 1532 or sysCONFIG™ interface
- High Performance
 - 4.0 ns t_{PD} pin-to-pin delays
 - 285 MHz f_{MAX}
- Low Power Consumption
 - Static power as low as 20 mA
- Ease of Design
 - 3.3, 2.5 and 1.8V power supply operation

ispXPLD 5000MX Block Diagram

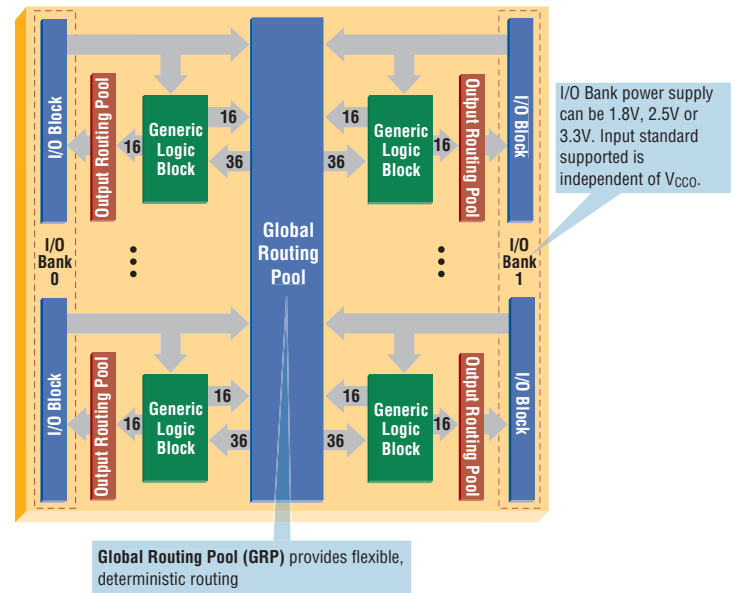


ispMACH 4000 Features and Benefits

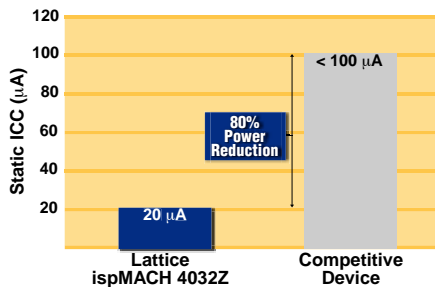
- **SuperFAST Performance**
 - 2.5 ns t_{PD} pin-to-pin delay
 - 400 MHz system performance
- **Industry's Lowest Power Consumption**
 - 1.8V core for low dynamic power
 - Low static current
 - 20 μ A max. (1.8V ispMACH 4000Z)
 - 1 - 3.5 mA (1.8V ispMACH 4000C)
- **Ease of Design**
 - In-system programmable
 - IEEE 1149.1, IEEE 1532 compliant
 - Flexible I/O support
 - 2 I/O banks with independent V_{CCO} and GND
 - Leave alone I/O – holds pin state during programming
 - LVTTTL, LVCMOS 1.8, 2.5, 3.3
 - 5V tolerant inputs and I/Os
 - Hot socketing support
- **Automotive Temperature Devices**
 - Broadest density range: 32 to 256 macrocells
 - Available for 3.3V (4000V) and 1.8V (4000Z) power supply
 - 7.5 ns t_{PD} pin-to-pin delay
 - 168 MHz system performance



ispMACH 4000 Block Diagram



Lattice Offers Ultra-Low Power Consumption



ispMACH 5000 Features and Benefits

- **SuperWIDE Performance**
 - 68 Inputs / 32 macrocells per logic block
 - 3.0 ns t_{PD} pin-to-pin delay
 - 275 MHz system performance
- **sysIO Capability for High Performance interfacing**
 - Leave alone I/O – holds pin state during programming
 - 5V tolerant inputs & I/Os
- **Ease of Design**
 - In-system programmable
 - IEEE 1149.1, IEEE 1532 compliant
 - 2.5V power supply operation
 - Hot socketing support

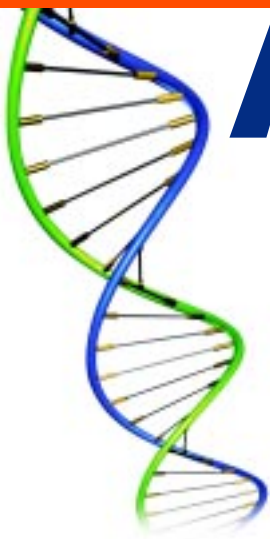
World's Fastest and Smallest PLD

Lattice's ispGAL22V10A device takes board-space savings and speed to a new level. This high performance device brings together the best features in one tiny package.

- 2.3 ns / 455 MHz Speed
- 150 μ A Standby Current
- 5 x 5 mm QFN Package
- In-System Programmable

XPLD and CPLD Device Families

Power Supply	Family	Macrocells	User I/O Options	t_{PD} (ns)	f_{MAX} (MHz)	Logic Block Inputs	Memory Kbits	Standby Current
1.8V	ispXPLD 5000MC	256 - 1024	141 - 381	4.0	300	68	128-512	12 mA
	ispMACH 4000C	32 - 512	30 - 208	2.5	400	36	—	1.8 mA
	ispMACH 4000Z	32 - 256	32 - 128	3.5	267	36	—	20 μ A (Max.)
2.5V	ispXPLD 5000MB	256 - 1024	141 - 381	4.0	300	68	128-512	16 mA
	ispMACH 5000B	128 - 512	92 - 256	3.0	275	68	—	83 mA
	ispMACH 4000B	32 - 512	30 - 208	2.5	400	36	—	11.3 mA
3.3V	ispXPLD 5000MV	256 - 1024	141 - 381	4.0	300	68	128-512	16 mA
	ispLSI 5000VE	128 - 512	72 - 256	5.0	180	68	—	100 mA
	ispMACH 4000V	32 - 512	30 - 208	2.5	400	36	—	11.3 mA
5V	ispMACH 4A5	32 - 256	32 - 128	5.0	182	36	—	20 mA



Analog Products

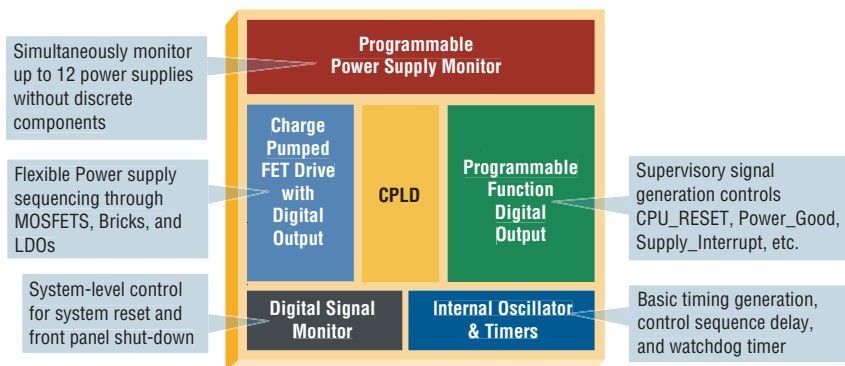
Programmable Analog & Mixed Signal Devices

Impossible was never so easy! Lattice delivers in-system programmable analog ICs (ispPAC) and the new Programmable Mixed Signal devices ... ispPAC Power Manager.



Bringing the Best Together: Integrating in-system programmable analog and digital components on a single chip, the ispPAC Power Manager devices provide complete monitoring and sequencing control of power supplies on your circuit board.

ispPAC Power Manager Block Diagram



ispPAC Design Tools

Lattice provides a complete set of tools for rapidly implementing analog and mixed signal designs.

- PAC-Designer Software Allows Intuitive Point & Click Design entry
 - Board power supply management
 - Adaptive analog front ends
 - Continuous-time filters from 5th order down
 - Flexible feedback control loops
- Simulation for Analog and Mixed Signal Designs
- Evaluation Boards for Rapid Prototyping



PAC-Designer software's easy-to-use GUI

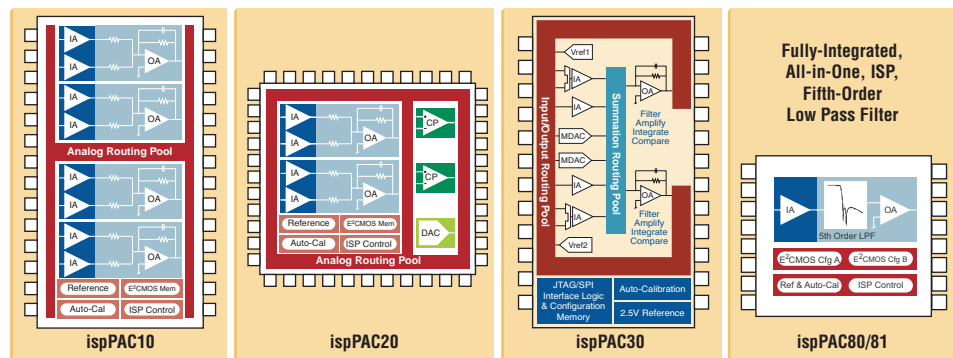


Power Manager and ispPAC Evaluation boards enable fast prototyping.

ispPAC Power Manager Devices

Device	Power Supply Sense Inputs	Supervisory Outputs	FET Drivers/Digital Outputs	Reprogrammable Timers	CPLD Macrocells
Power1208	12	4	4	4	16
Power604	6	4	—	2	8

ispPAC Device Block Diagrams



ispPAC Device Families

Device	Filters	Control Loop	Sensor Interface	Data Acquisition
ispPAC10	✓	—	✓	—
ispPAC20	✓	✓	✓	✓
ispPAC30	—	✓	✓	✓
ispPAC80/81	✓	—	—	✓

ispLEVER Design Tools

The Simple Machine for Complex Design

Lattice's ispLEVER® is an advanced programmable logic design tool equipped to provide a complete system for FPGA, FPSC, CPLD, XPLD, ispGDX®, and SPLD design. ispLEVER includes a fully integrated, push-button design environment, and advanced features for interactive design optimization and debug.

ispLEVER Design Tools Features

- Integrated ModelSim® RTL Simulator
- Integrated Mentor Graphics® and Synplicity® Synthesis
- VHDL, Verilog, and ABEL Language Support
- Module Generator / IP Manager
- Comprehensive Constraints / Pin Editor
- Floorplanner for FPGA / FPSC
- EPIC Chip Editor
- Integrated Timing and Functional Simulator
- HTML Reporting and Help
- TCL/Tk Scripting Tools
- ispTRACY™ Logic Analyzer (ispXPGA)
- Integrated ispVM® Programming Software
- PC and UNIX Versions



ispLEVER Design Tools

Package	Part Number	ispXPGA	ORCA	FPSC	CPLD			ModelSim Simulation
					GDX/2 SPLD	LeoSpec Synthesis	Synplify® Synthesis	
Starter	Downloadable	✓			✓	✓	✓	
Base	LS-HDL-BASE-PC-N	✓	✓		✓	✓	✓	✓
Advanced	LS-HDL-ADV-PC-N	✓	✓	✓	✓	✓	✓	✓
	LS-ADV-WS-F	✓	✓	✓	✓			
	LS-ADV-PC-F	✓	✓	✓	✓			

Intellectual Property

Lattice offers an expanding range of IP cores (ispLeverCORE™ IP modules) to support easy integration of commonly used complex functions for:

- **Communications**
 - UTOPIA
 - Fast 10/100 Ethernet MAC
 - Gigabit Ethernet MAC
 - 10 Gigabit PCS
- **Bus Interface**
 - PCI Master/Target
 - PCI Express
- **Memory Control**
 - DDR SDRAM Controller
 - Multi-channel DMA Controller
- **Digital Signal Processing**
 - Reed Solomon Encoder
 - Convolutional Encoder
 - FIR Filter

For a complete list of IP cores available from Lattice and our IP partners, see the Lattice website.

Evaluation and Programming Hardware

Evaluation boards are offered to allow users to evaluate, test, and perform design debug for a variety of Lattice devices and include:

- EV Board
- Download Cable
- Board Schematics
- Users Manual

Lattice also offers a wide range of programming cables, desktop programmers, and adapters for advanced packages:

- **ispDOWNLOAD® Cables**
 - Parallel (1 x 8, 2 x 5, Flywire)
 - USB (Flywire)
- **Model 300 Desktop Programmer and Adapters**



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