Lattice Semiconductor Corporation

Thermal Management

April 2008

Introduction to Thermal Management

Thermal management is recommended as part of any sound CPLD and FPGA design methodology. To properly assess the thermal characteristics of the system, Lattice Semiconductor specifies a maximum allowable junction temperature in all device data sheets. The system designer should always complete a thermal analysis of their specific design to ensure that the device and package does not exceed the junction temperature requirements.

The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. Table 1 specifies the generic package thermal resistance for legacy GAL, CPLD, FPGA and XPLD devices. Table 2 specifies the device/package specific thermal resistance for newer FPGA products. These values are based upon JEDEC standards. If specified, the device/package specific thermal value supercedes the generic package thermal data contained in Table 1.

In addition to the device and package, the thermal characteristics of a circuit depend on the operating temperature, device power consumption, and the ability of the system to dissipate heat. The maximum junction temperature of a device can be calculated as shown:

$T_J = T_A + \text{Power}*\theta_{JA}$

or

$T_J = T_A + \text{Power} *(\theta_{JC}+R_{CS}+R_{SA})$

Where :

T_J	=	Junction Temperature of the Device
T_A	=	Ambient Temperature
R_{CS}	=	Thermal resistance of thermal interface material
R_{SA}	=	Thermal resistance of heat sink
θ_{JA}	=	Junction-to-Ambient Thermal Resistance (see Tables 1 and 2 at the end of this section)
θ_{JC}	=	Junction-to-Case Thermal Resistance (see Tables 1 and 2 at the end of this section)
Power	=	$I_{CC} * V_{CC}$

I_{CC} may be estimated as shown in the “Power Consumption” section of the DC and Switching Characteristics section of each individual data sheet. The parameters in the I_{CC} equation may be found in the report file from the ispLEVER® compiler. For predicting power, the best resource is to use ispLEVER design tools. For additional information on power calculations and considerations please refer to the referenced technical note in the For Further Information section of each individual data sheet.

If the calculated T_J max exceeds the specified limits, refer to the following hints to reduce the overall power dissipation and package temperature.

Ways to Reduce Junction Temperature

1. Increase airflow in the system to reduce the case or ambient temperature.

2. Reduce power in one of the following ways:

   a. Reduce overall device utilization by combining common input functions. This is especially true when using wide input CPLD blocks. Even with the narrow FPGA logic blocks, careful partitioning of logic can reduce the overall net utilization.
   b. Trade off net utilization with reducing the number of high frequency switching nets. By careful use of different encoding schemes, the high frequency switching nodes can be reduced. For example, using one-hot encoding can reduce the high frequency switching nodes compared to a binary encoding while increasing the logic utilization.
   c. Reduce the frequency of operation. High-density architectures provide flexibility to control clock polarity to potentially reduce the overall clock speed.

3. Where possible, make use of the output slew rate control to reduce the output switching current of the device.

4. Make sure that programmable pull-ups are enabled to drive unused inputs to a proper logic level.

5. Select an appropriate heat sink and thermal interface material for the package.

***Table 1. Package Thermal Resistance*[1]**

Package	Dimension	Pin Count	θ_{JA} (0lfm)	θ_{JA} (200lfm)	θ_{JC}
PDIP	.300 wide	16	77	56	31
	.300 wide	20	67	49	30
	.300 wide	24	64	35	25
	.300 wide	28	56	33	23
PLCC	–	20	64	58	22
	–	28	56	49	18
	–	44	35	31	16
	–	68	34	30	13
	–	84	33	29	12
QFN	5x5mm	32	35	33	15 (Theta JB) [2]
SOIC	–	16	104	86	23
	–	20	85	69	18
	–	24	80	52	17
	–	28	74	50	15
SSOP	–	28	105	80	25
PQFP/MQFP	14x20 mm	100	35	34	12
	28x28 mm	120	32	26	12
	28x28 mm	128	32	26	11
	28x28 mm	160	30	24	9
	28x28 mm	208	25	23	8
	28x28 mm	208 HS	14	12	3
	32x32 mm	240	24	18	5
	32x32 mm	240 HS	13	11	3
	40x40 mm	304 HS	12	9	3

Table 1. Package Thermal Resistance[1]

Package	Dimension	Pin Count	θ_{JA} (0lfm)	θ_{JA} (200lfm)	θ_{JC}
TQFP (1.4 mm thick)	10x10 mm	44	42	36	17
	7x7 mm	48	48	44	19
	14x14 mm	100	35	29	10
	14x14 mm	128	35	29	10
	20x20 mm	144	33	27	9
	24x24 mm	176	33	27	8
TQFP (1.0 mm thick)	7x7 mm	48	49	45	19
	10x10 mm	44	43	37	17
caBGA/csBGA	5x5 mm	64	90	85	15
	6x6 mm	56	74	68	15
	7x7 mm	49	74	68	15
	7x7 mm	144	72	66	13
	8x8 mm	132	49	40	13
	10x10 mm	100	48	39	12
fpBGA	11x11 mm	100	40	32	11
	13x13 mm	144	29	25	11
	17x17 mm	208	24	20	10
	17x17 mm	256	20	16	10
	23x23 mm	388	18	15	6
	23x23 mm	484	18	15	6
	27x27 mm	416	17	14	5
	27x27 mm	672	16	13	5
	31x31 mm	516	14	12	4
	31x31 mm	516 HS	13	11	3
	31x31 mm	676	14	12	4
	31x31 mm	900	14	12	4
	31x31 mm	900 HS	13	11	3
	35x35 mm	680	14	12	3
	35x35 mm	680 HS	13	11	2.7
	35x35 mm	1156	13	11	3
	35x35 mm	1156 HS	12	9.9	2.7
PBGA	27x27 mm	272	20	17	6
	35x35 mm	388	16	13	3
	35x35 mm	492	16	13	3
fpSBGA	40x40 mm	680	11	10	0.65
	45x45 mm	1036	10	9	0.65
ftBGA	17x17 mm	256	29	23.5	10
fcBGA	15x15 mm	269	26	25	2

Table 1. Package Thermal Resistance[1]

Package	Dimension	Pin Count	θ_{JA} (0lfm)	θ_{JA} (200lfm)	θ_{JC}
SBGA	27x27 mm	256	15	12	0.65
	31x31 mm	320[3]	13	10	0.65
	35x35 mm	352	12	9	0.65
	40x40 mm	432[3]	11	8	0.65
	45x45 mm	600	10	7	0.65
CERDIP	–	20	62	52	10
	–	24	60	48	10
LCC	–	20	65	60	8
	–	28	62	49	7
JLCC	–	44	69	38	4
	–	68	52	30	3
CPGA	–	84	38	21	3
	–	133	26	21	2

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1. The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. This Table specifies the generic package thermal resistance for legacy GAL, CPLD, FPGA and XPLD devices. These values are based upon JEDEC standards. If specified in Table 2, the device/package specific thermal value supercedes the generic package thermal data contained in this Table.
2. _JB (_JB = Junction-to-Board Thermal Resistance). _JB value shown is only applicable when the package thermal pad is soldered directly onto user PCB.
3. The 320-ball BGA and 432-ball BGA packages junction temperature must not exceed 140˚C.

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimension	Pin Count	θ_{JA} (0lfm)	θ_{JA} (200lfm)	θ_{JA} (500lfm)	θ_{JC}
ECP/EC	LFEC1	TQFP	14x14 mm	100	36.9	33.0	30.4	12.4
	LFEC1	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LFEC1	PQFP	28x28 mm	208	40.2	37.0	34.2	18.5
	LFEC3	TQFP	14x14 mm	100	36.9	33.0	30.4	12.4
	LFEC3	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LFEC3	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFEC3	FPBGA	17x17 mm	256	28.4	24.3	21.8	5.2
	LFECP/EC6	TQFP	20x20 mm	144	27.8	25.0	23.1	7.2
	LFECP/EC6	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFECP/EC6	FPBGA	17x17 mm	256	25.9	22.0	19.5	4.0
	LFECP/EC6	FPBGA	23x23 mm	484	19.6	16.9	15.3	6.5
	LFECP/EC10	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFECP/EC10	FPBGA	17x17 mm	256	24.0	20.1	17.7	3.1
	LFECP/EC10	FPBGA	23x23 mm	484	18.0	15.4	13.7	5.0
	LFECP/EC15	FPBGA	17x17 mm	256	22.7	18.9	16.5	2.6
	LFECP/EC15	FPBGA	23x23 mm	484	17.1	14.6	12.8	4.2
	LFECP/EC20	FPBGA	23x23 mm	484	16.6	14.0	12.2	3.8
	LFECP/EC20	FPBGA	27x27 mm	672	15.2	12.8	11.0	3.2
	LFECP/EC33	FPBGA	23x23 mm	484	15.8	13.1	11.3	3.1
	LFECP/EC33	FPBGA	27x27 mm	672	14.0	11.8	10.1	2.6
ECP2	LFE2-6E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LFE2-6E	FPBGA	17x17 mm	256	29.1	25.0	22.5	5.7
	LFE2-12E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LFE2-12E	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFE2-12E	FPBGA	17x17 mm	256	26.7	22.7	20.2	4.3
	LFE2-12E	FPBGA	23x23 mm	484	20.0	17.4	15.8	7.0
	LFE2-20E	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFE2-20E	FPBGA	17x17 mm	256	24.9	21.0	18.5	3.5
	LFE2-20E	FPBGA	23x23 mm	484	18.7	16.1	14.4	5.6
	LFE2-20E	FPBGA	27x27 mm	672	17.4	15.1	13.0	4.8
	LFE2-35E	FPBGA	23x23 mm	484	17.7	15.2	13.4	4.7
	LFE2-35E	FPBGA	27x27 mm	672	16.4	14.0	12.1	4.0
	LFE2-50E	FPBGA	23x23 mm	484	16.7	14.2	12.3	3.9
	LFE2-50E	FPBGA	27x27 mm	672	15.3	13.0	11.2	3.3
	LFE2-70E	FPBGA	27x27 mm	672	14.3	12.0	10.3	2.7
	LFE2-70E	FPBGA	31x31 mm	900	12.6	10.5	9.2	2.0

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimension	Pin Count	θ_{JA} (0lfm)	θ_{JA} (200lfm)	θ_{JA} (500lfm)	θ_{JC}
ECP2M	LFE2M20E	FPBGA	17x17 mm	256	24.2	20.2	17.8	3.2
	LFE2M20E	FPBGA	23x23 mm	484	18.1	15.6	13.8	5.1
	LFE2M35E	FPBGA	17x17 mm	256	22.4	18.5	16.2	2.5
	LFE2M35E	FPBGA	23x23 mm	484	16.8	14.3	12.5	4.0
	LFE2M35E	FPBGA	27x27 mm	672	15.5	13.0	11.1	3.1
	LFE2M50E	FPBGA	23x23 mm	484	15.6	13.1	11.3	3.1
	LFE2M50E	FPBGA	27x27 mm	672	14.2	11.9	10.2	2.6
	LFE2M50E	FPBGA	31x31 mm	900	12.5	10.4	9.1	1.9
	LFE2M70E	FPBGA	31x31 mm	900	11.7	9.5	8.1	1.5
	LFE2M70E	FPBGA	35x35 mm	1152	13.7	12.0	11.0	2.2
	LFE2M100E	FPBGA	31x31 mm	900	10.8	8.6	7.1	1.2
	LFE2M100E	FPBGA	35x35 mm	1152	13.2	11.2	9.8	1.7
	LFE2M100E	FPBGA	35x35 mm	1156	13.2	11.2	9.8	1.7
SC/SCM	LFSC/SCM15	FPBGA	17x17 mm	256	21.1	17.4	15.1	2.1
	LFSC/SCM15	FPBGA	31x31 mm	900	12.9	10.8	9.6	2.1
	LFSC/SCM25	FPBGA	31x31 mm	900	11.5	9.3	7.9	1.5
	LFSC/SCM25	FFBGA	33x33 mm	1020	10.1	8.1	6.7	1.1
	LFSC/SCM40	FFBGA	33x33 mm	1020	10.1	8.1	6.7	1.1
	LFSC/SCM40	FCBGA	35x35 mm	1152	9.5	6.8	5.1	0.6
	LFSC/SCM80	FCBGA	35x35 mm	1152	7.9	5.7	4.2	0.5
	LFSC/SCM80	FFBGA	42.5x42.5 mm	1704	7.7	5.5	4.0	0.5
	LFSC/SCM115	FCBGA	35x35 mm	1152	7.9	5.7	4.2	0.5
	LFSC/SCM115	FFBGA	42.5x42.5 mm	1704	7.7	5.5	4.0	0.5
MachXO	LCMXO256C/E	CSBGA	8x8 mm	100	85.4	79.4	74.4	31.9
	LCMXO256C/E	TQFP	14x14 mm	100	36.9	33.0	30.4	12.4
	LCMXO640C/E	CSBGA	8x8 mm	100	75.1	69.5	65.9	18.5
	LCMXO640C/E	TQFP	14x14 mm	100	36.9	33.0	30.4	12.4
	LCMXO640C/E	CSBGA	8x8 mm	132	67.6	62.3	58.5	16.7
	LCMXO640C/E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LCMXO640C/E	FTBGA	17x17 mm	256	44.9	40.3	37.8	11.4
	LCMXO1200C/E	TQFP	14x14 mm	100	36.9	33.0	30.4	12.4
	LCMXO1200C/E	CSBGA	8x8 mm	132	55.7	51.0	48.0	9.7
	LCMXO1200C/E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LCMXO1200C/E	FTBGA	17x17 mm	256	41.8	36.9	34.3	7.7
	LCMXO2280C/E	TQFP	14x14 mm	100	36.9	33.0	30.4	12.4
	LCMXO2280C/E	CSBGA	8x8 mm	132	48.4	44.1	41.6	6.6
	LCMXO2280C/E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LCMXO2280C/E	FTBGA	17x17 mm	256	40.0	34.9	32.3	5.1
	LCMXO2280C/E	FTBGA	19x19 mm	324	37.3	31.2	29.5	6.2

Table 2. Device/Package Thermal Resistance[1]

Family	Device	Package	Dimension	Pin Count	θ_{JA} (0lfm)	θ_{JA} (200lfm)	θ_{JA} (500lfm)	θ_{JC}
XP	LFXP3C/E	TQFP	14x14 mm	100	31.0	27.1	24.6	8.1
	LFXP3C/E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LFXP3C/E	PQFP	28x28 mm	208	29.5	27.0	24.7	13.2
	LFXP6C/E	TQFP	20x20 mm	144	27.8	25.0	23.1	7.2
	LFXP6C/E	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFXP6C/E	FPBGA	17x17 mm	256	25.7	21.6	19.4	5.3
	LFXP10C/E	FPBGA	17x17 mm	256	23.4	19.5	17.2	2.9
	LFXP10C/E	FPBGA	23x23 mm	388	17.6	15.0	13.2	4.6
	LFXP15C/E	FPBGA	17x17 mm	256	21.6	18.1	15.6	1.5
	LFXP15C/E	FPBGA	23x23 mm	388	16.1	13.5	11.9	3.8
	LFXP15C/E	FPBGA	23x23 mm	484	16.3	14.0	12.0	3.7
	LFXP20C/E	FPBGA	17x17 mm	256	21.9	17.8	15.6	2.8
	LFXP20C/E	FPBGA	23x23 mm	388	16.2	13.7	11.8	3.5
	LFXP20C/E	FPBGA	23x23 mm	484	16.2	13.7	11.8	3.5
XP2	LFXP2-5E	CSBGA	8x8 mm	132	47.2	43.0	40.5	6.1
	LFXP2-5E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LFXP2-5E	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFXP2-5E	FTBGA	17x17 mm	256	39.1	34.1	31.4	6.1
	LFXP2-8E	CSBGA	8x8 mm	132	41.9	38.0	35.8	4.4
	LFXP2-8E	TQFP	20x20 mm	144	28.8	26.1	24.0	9.4
	LFXP2-8E	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFXP2-8E	FTBGA	17x17 mm	256	37.2	32.3	29.5	5.1
	LFXP2-17E	PQFP	28x28 mm	208	30.2	27.8	25.7	13.9
	LFXP2-17E	FTBGA	17x17 mm	256	33.9	29.1	26.2	4.3
	LFXP2-17E	FPBGA	23x23 mm	484	18.6	16.0	14.3	5.5
	LFXP2-30E	FTBGA	17x17 mm	256	32.0	27.1	24.2	3.0
	LFXP2-30E	FPBGA	23x23 mm	484	17.3	14.8	13.0	4.4
	LFXP2-30E	FPBGA	27x27 mm	672	16.0	13.6	11.7	3.7
	LFXP2-40E	FPBGA	23x23 mm	484	16.5	14.0	12.1	3.7
	LFXP2-40E	FPBGA	27x27 mm	672	15.1	12.7	10.9	3.1

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1. The data shown in this Thermal Management document is relative and actual values depend on a variety of factors such as: die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices and user applications. This Table specifies the device/package specific thermal resistance for newer FPGA products. These values are based upon JEDEC standards.

Revision History

Date	Version	Change Summary
–	–	Previous Lattice releases.
September 2007	01.0	Updated Table 1 and added Table 2: Device/Package Thermal Resistance.
January 2008	01.1	Updated Table 1 with information for ftBGA 256 packaging.
March 2008	01.2	Corrected equation on page 1.
April 2008	01.3	Added 64-ball csBGA and 144-ball csBGA packaging to Table 1.