

Introduction

The ispMACH™ 4000B/C families offer an ideal mix of both high speed and low power in the same device. With an advanced low-power electrically erasable non-volatile memory cell and a full CMOS logic design approach, the ispMACH 4000B/C families offer the fastest pin-to-pin propagation delays for designs requiring high speed, while consuming only milliamps of static current. The low standby and dynamic power is provided without needing any “turbo bits” or other power management schemes associated with traditional low power CPLD approaches.

1.8V Core E²CMOS® Technology

The ispMACH 4000B/C devices have an internal core voltage of 1.8V. For the ispMACH 4000B family, a built-in voltage regulator allows the user to interface to a 2.5V power supply with the core device voltage running at 1.8V. Because device I_{CC} is proportional to capacitance and switching voltage, the lower 1.8V internal voltage helps reduce the dynamic component of power consumption. The internal voltage regulator needs a bias current however, which leads to a higher static component on the 2.5V devices

Power Estimation

This section describes how to estimate the power consumption of the ispMACH 4000 devices. It is important to confirm these estimates with the actual design under the intended operating conditions.

Power consumption in the ispMACH 4000 family devices depends on three primary factors:

1. The operating clock frequency
2. The operating voltage
3. The power dissipated by the I/Os

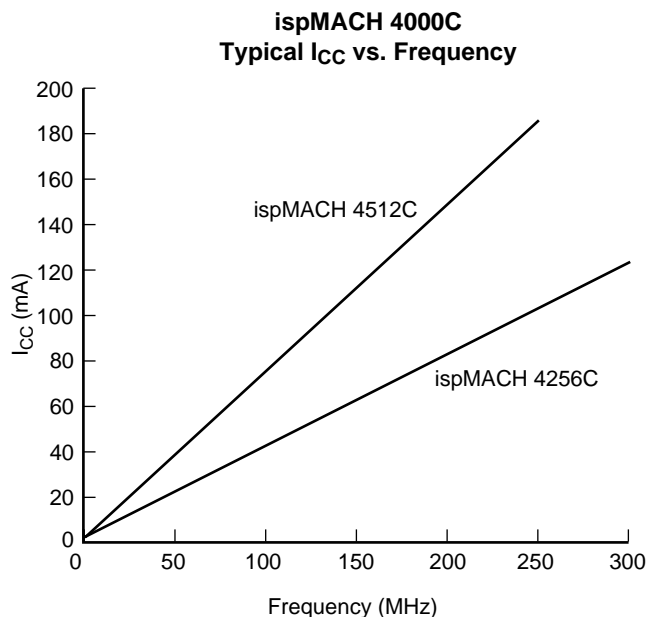
The current consumption for the ispMACH 4000 can be estimated using the following equation:

$$I_{CC} = A + B * N * F_{MAX} * SR + I_{CCIO}$$

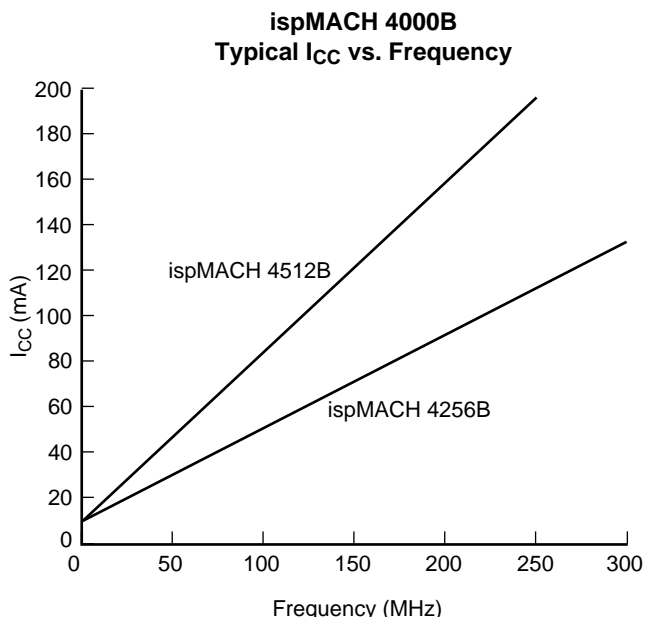
- I_{CC} = Current consumed by the ispMACH 4000 (mA)
- A = Static component, given in the device data sheet
- B = Dynamic coefficient, given in the device data sheet (mA/MHz/MC)
- N = Number of macrocells in the design
- f_{MAX} = Operating Clock Frequency
- SR = Switching Rate Factor of the design used
- I_{CCIO} = Current attributable to I/Os

In this case, a 16-bit counter pattern assumes a minimal I/O loading and Switching Rate factor (SR) of 0.125 is used to perform initial estimates. Figure 1 shows the relationship between I_{CC} and operating frequency for the ispMACH 4000B/C at typical operating voltage and room temperature. The selected pattern is a multiple 16-bit up-down counter that fills the device and exercises every macrocell at frequency

Figure 1. ispMACH 4000 Typical Device Power Consumption vs. F_{MAX}



Note: The devices are configured with maximum number of 16-bit counters, typical current at 1.8V, 25° C.



Note: The devices are configured with maximum number of 16-bit counters, typical current at 2.5V, 25° C.

Technical Support Assistance

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