

Users of the ORT82G5 often are interested in the SERDES receiver's performance during acquisition and re-acquisition (locking) on to the incoming high-speed serial data stream. However, this term can have many meanings. For this reason, this note seeks to describe the various components of the acquisition process and report the results of measurements of each component.

The ORT82G5 SERDES RX logic performs four levels of synchronization on the incoming serial data stream. Each level builds upon the previous, providing first bit, then byte (character), then channel (32-bit word), and finally multi-channel alignment. Each is described below.

Bit Alignment

Bit alignment is the task of the Clock/Data Recovery (CDR) block. This block utilizes a PLL that locks to the transitions in the incoming high-speed serial data stream, and outputs the extracted clock as well as the data. If the PLL is unable to lock to the serial data stream, it instead locks to REFCLK to stabilize the voltage-controlled oscillator (VCO), and periodically switches back to the serial data stream to again attempt synchronization. This process continues until a valid input data stream is detected and lock is achieved.

The CDR can maintain lock on data as long as the input data stream contains an adequate data "eye" (i.e., jitter is within specification), and maximum data stream run length is not exceeded.

Bit alignment times fall into two categories: alignment from a no-signal condition, and re-alignment when the input serial data stream experiences an abrupt phase change (as may occur when protection switching is performed between two paths having different delays).

Alignment from a no-signal condition has two components. First, there is the re-acquisition to the data's frequency and phase. The time required for re-acquisition to the data's frequency is minimized by logic that periodically switches the PLL to lock to the REFCLK when it fails to lock on the serial data stream, thus limiting the VCO's frequency wander. Second, there is the time spent while the PLL is locking to REFCLK, which can be from zero to a maximum value, depending on when the serial data stream becomes valid in relation to the PLL's switching to/from REFCLK. In the lab, this alignment has been observed to require no more than 4 microseconds when REFCLK = 156.125 MHz.

Re-alignment is very quick, since the PLL's VCO is already locked on frequency and only needs to adapt to the new phase. In the lab, this re-alignment has been observed to require no more than one microsecond when REFCLK = 156.125 MHz.

Byte Alignment

Byte alignment occurs once valid bit alignment is achieved. The byte aligner looks for a particular 7-bit sequence (either 0011111 or its complement, 1100000) that, in data that has been 8B/10B encoded per IEEE 802.3, only occurs in the comma (/K/) characters K28.1, K28.5 and K28.7. Byte alignment only occurs when the ENBYSYNC signal for that channel is active HI, and re-alignment occurs on each 7-bit sequence encountered. However, if ENBYSYNC is asserted active HI and no comma character is encountered, and then is brought inactive LO, the channel will still perform one byte alignment operation on the next comma character.

Byte alignment occurs immediately when an alignment sequence is detected, so lock time is only one clock period.

Word (32-bit) Alignment

Word (32-bit) alignment requires that the Fibre-Channel (XAUI_MODE = 0) or XAUI (XAUI_MODE = 1) state machine has achieved the synchronized state.

Fibre-Channel Mode: synchronization (WDSYNC = 1) will occur after three¹ ordered sets of data have been received, in the absence of any code violations. After this, the next comma character will cause the output data to be aligned such that the comma character is in the most significant byte. Thus, three¹ ordered sets plus a comma character must be detected after byte sync is achieved before 32-bit word alignment occurs. The time required is directly dependent on comma-character density. This has been verified in the lab.

Note: once word alignment is accomplished, no further alignment occurs unless and until WDSYNC goes to zero and back to one again. Comma characters that are not located in the most significant byte position will not trigger further re-alignment while WDSYNC is active. This behavior is as defined by the Fibre-Channel specification. But it means that, if the channel experiences an abrupt delay change (as could occur if an external MUX performs a protection switch between two links), and the delay change is close enough to a full character or characters that not enough code violations are generated to cause loss of WDSYNC, the channel could become misaligned and remain that way indefinitely. This behavior has been observed in the lab. As mentioned above, this is as defined by the Fibre-Channel specification.

XAUI Mode — The state diagram in the data sheet indicates that three error-free code-groups containing commas must be detected before synchronization is declared.

Multi (2, 4 or 8) Channel Alignment

Multi (2, 4 or 8) channel alignment does not occur until after 32-bit word alignment is complete. Alignment will not occur until the last (most delayed) channel has been received. The maximum skew between the earliest and latest channels cannot be greater than 18 cycles of the parallel receive data clock RWCK. At 78.125 MHz, this is 12.8 ns X 18 = 230.4 ns maximum.

Re-Lock After Loop Delay Change

Figures 1 and 2 display the performance of the ORT82G5 when the high-speed serial bit stream experiences an abrupt loop delay change in the serial link. Here, the delay change is caused by a switch into (Figure 1) or out of (Figure 2) internal loopback, where the non-loopback path is looped back externally. The transmitter is sending an idle ordered set every 32nd word. Code violations mark the beginning of the abrupt delay change. When the receiver re-establishes phase lock and a comma character is recognized, code violations cease. Four comma characters later (data taken using V2 silicon¹), word sync is re-established. Word alignment is performed on the next comma character, at which time the PRBS data checker implemented in the FPGA ceases to report errors.

Figure 1. Re-Lock After Positive Loop Delay Change

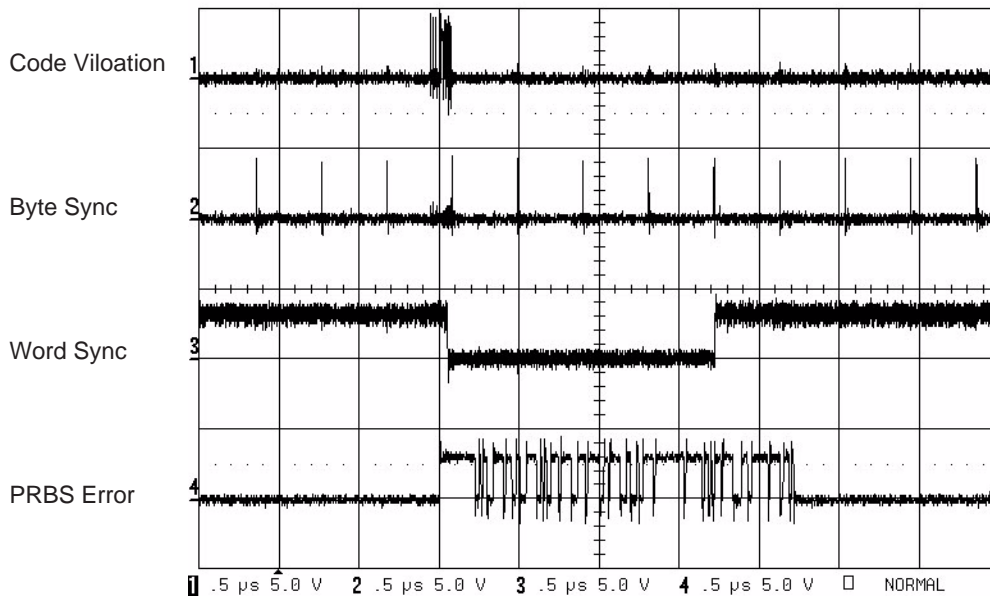
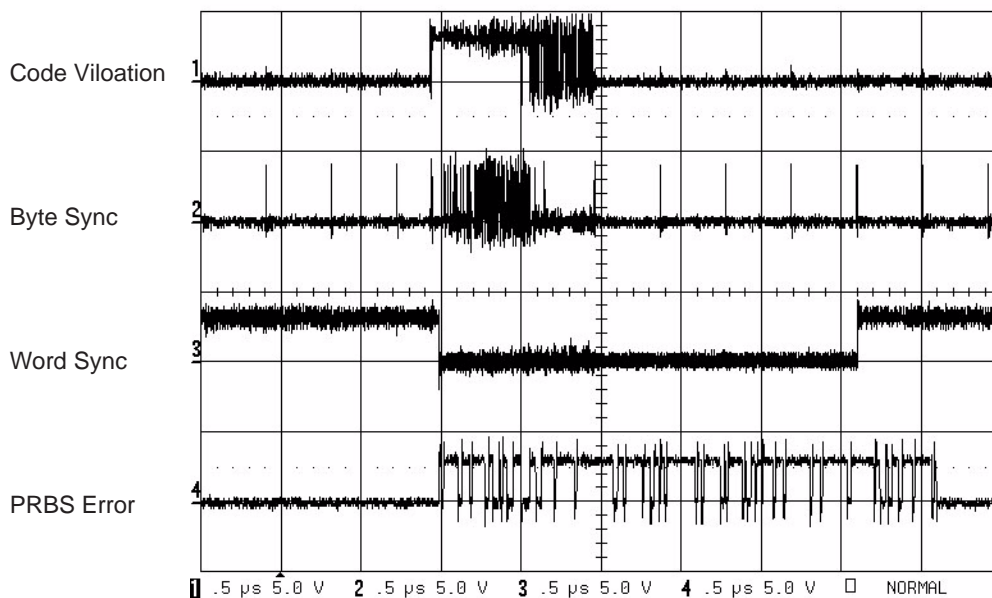


Figure 2. Re-Lock After Negative Loop Delay Change



Conclusion

In conclusion, the “lock time” can mean many things, but breaks down into the components outlined above: bit, byte, word and multi-channel alignment. Once the chip has recovered from reset and REFCLK is stable, the time required to lock onto a high-speed serial data stream is sub-microsecond. Further time required for byte synchronization, word synchronization, word alignment and multi-channel alignment depends on density of comma characters: one for byte sync, three¹ for word sync, and one for word alignment. Multi-channel alignment occurs shortly after the latest channel arrives.

¹ Note: ORT82G5 V2 and earlier silicon requires four ordered sets in order to achieve Fibre-Channel link synchronization (WDSYNC = 1), rather than the three required by V3 and later silicon. Figures 1 and 2 reflect data taken using V2 silicon.