

## Introduction

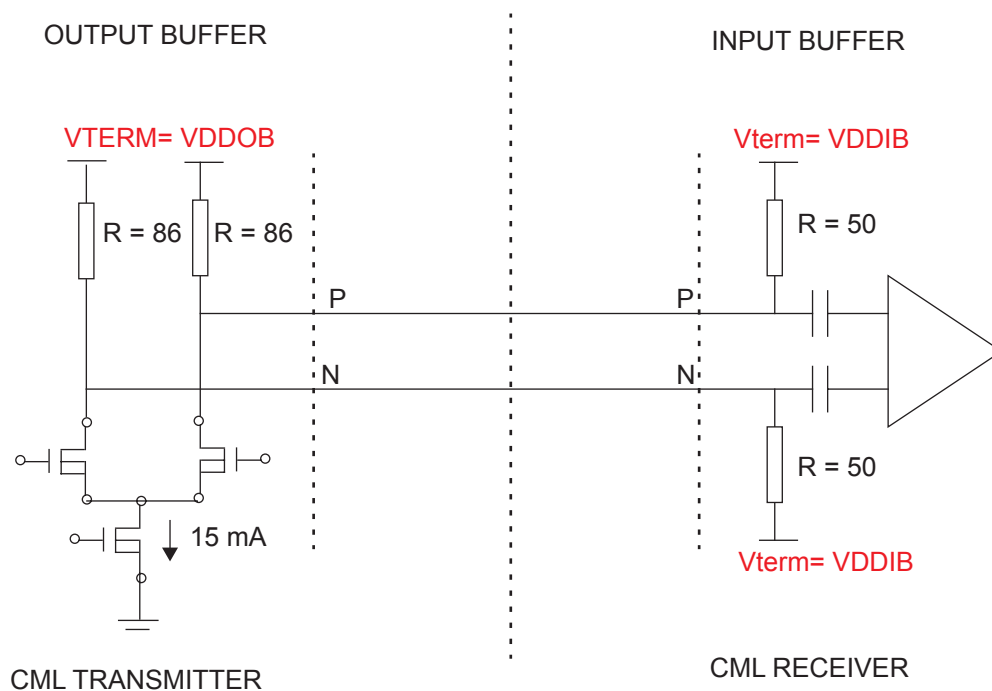
This document discusses the high-speed serial buffers provided in Lattice's ORT82G5 FPSC device. These current mode logic (CML) buffers are part of a second generation Quad SERDES macrocell design and provide the high-speed (1.0 to 3.7Gbps) serial data input and output ports. The data sheet description of this device can be found in Reference 1. Portions of this data sheet are included in this document. Off-chip signal interface design and characteristics are the focus of this document. Interfacing to external high-speed devices with LVDS and LVPECL ports is also discussed. Transmission line interconnections between devices are required because of the high data rates. Practical considerations related to printed circuit boards, cables and connectors that carry these signals are also touched on in this document.

## CML Buffer Description

The SERDES macro uses 0.16  $\mu\text{m}$  technology (0.16  $\mu\text{m}$  drawn, 0.135  $\mu\text{m}$  physical). Internal input and output terminations are provided to simplify board level interfacing for the user. A simplified schematic of the serial input and output buffers are shown below in Figure 1. The termination resistors and coupling capacitors are internal to the macro.

The SERDES macrocell provides separate Rx and Tx power input nodes VDDIB and VDDOB for each channel, allowing the receiver input termination and transmitter output termination to be biased at different level, independent of the core VDD voltage (1.5V).

**Figure 1. SERDES CML Buffer Schematic Diagram.**



## Interface Parameter Specification

The high operational speed of the SERDES serial I/O makes understanding the interface parameters especially important to the user. Proper interpretation of the parameters is needed for successful integration within a system. Signal interconnection performance, reliability and integrity are closely tied to these characteristics and their variational limits. This section attempts to summarize and discuss critical serial buffer interface parameters.

Correctly specifying the buffer I/O is a complex process. Methods used include extensive SPICE simulation and laboratory measurements. The official specification listing for the SERDES should be obtained from the Device data sheet (Reference 1). Revised issues of these documents will reflect updates and refinements in buffer specifications, as they are determined.

### Input Buffer

Table 1 describes input buffer parameters and characteristics that are needed for application interface to other printed wiring board devices.

**Table 1. Rx Input Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tj	Operating Junction Temperature		-40	-	125	°C
Ri	Internal Buffer Termination Resistance	Each input, to VDDIB	40	50	60	Ω
	Differential return loss	Package dependent	-	-	-	db
	Common-mode return loss	Package dependent	-	-	-	db
VDDIB	Input Termination Supply Voltage	Externally supplied	0	1.5 /1.8	1.9	V
Vi	Peak Input Voltage Limits		-0.3	-	VDD +0.3	V
	Common-mode Noise Tolerance	VDDIB bias dependent	TBD	-	-	V
	Internal Input ac-Coupling Time Constant		-	160	-	nS
	Clock and data recovery (CDR) closed loop bandwidth		-	3	-	MHz

Figure 2. Receive Data Eye-Diagram Template (Differential)

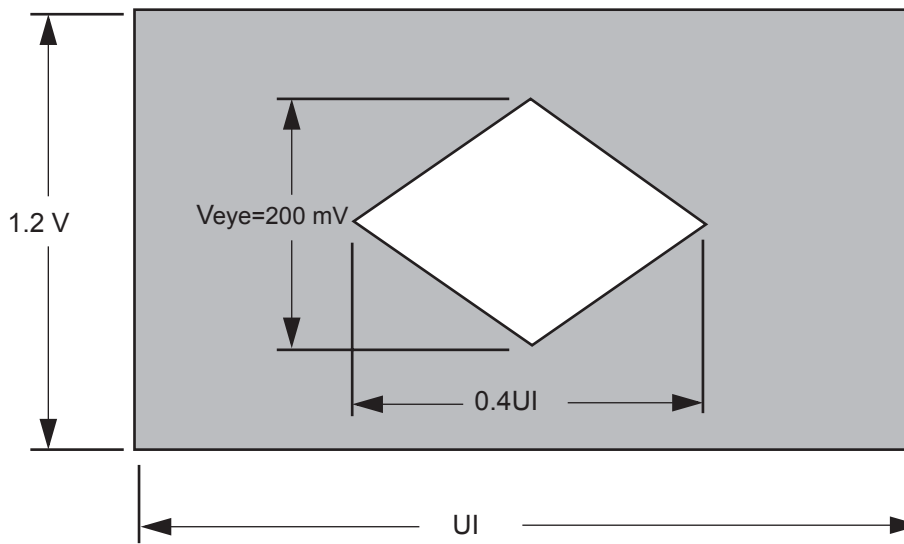


Figure 2 provides a graphical characterization of the SERDES receiver input requirements. It provides guidance on a number of input parameters including signal amplitude, rise time limits, noise and jitter limits, and P to N input skew tolerance.  $V_{eye}$  is specified as 200 mV. Incoming data patterns falling within the shaded region of the template will be received without error (BER < 1E-12), over all specified operating conditions.

Data pattern eye-opening at the receive end of a link is a good measure of received signal quality. Almost all detrimental characteristics of transmit signal and the interconnection link design result in eye closure. The eye-diagram template of Figure 2 represents the receiver's ability to function with signal eye-closure. In theory, eye-diagram measurements may be compared to eye-diagram templates to assess the ability of a data link, to transfer data error-free.

Signal jitter is of special interest to system designers. It is often the primary limiting characteristic of long digital links and of systems with high noise level environments. An interesting characteristic of the clock and data recovery (CDR) portion of the SERDES receiver is its ability to filter incoming signal jitter that is below the clock recovery PLL bandwidth (estimated to be about 3 MHz). For signals with high levels of low frequency jitter the receiver can correctly detect an incoming data stream, even with eye-openings significant less than that of Figure 2. This phenomenon has been observed in the laboratory.

Eye-diagram measurement and simulation are excellent tools of design. They are both highly recommended when designing serial link interconnections and evaluating system signal integrity.

## Output Buffer

Table 2 describes output buffer parameters and characteristics that are needed for application interface to other printed wiring board devices.

**Table 2. Tx Output Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T <sub>j</sub>	Operating Junction Temperature		-40	-	125	°C
VDDOB	Output Termination Supply Voltage	Externally supplied	1.3	1.5 / 1.8	1.9	V
R <sub>o</sub>	Internal Buffer Termination Resistance	Internally tied to VDDOB	69	86	103	Ω
R <sub>I</sub>	Preferred external load	Terminated to 1.5V/1.8V	-	50	-	W
	Differential peak-to-peak output	Full-amplitude mode Half-amplitude mode	0.8 0.4	1.0 0.5	1.2 0.6	V
V <sub>OH</sub>	Output voltage - High	VDDOB = 1.5V, 50Ω ext. load to 1.5V VDDOB = 1.8V, 50Ω ext. load to 1.8V	-	1.5 1.8	-	V
V <sub>OL</sub>	Output voltage - Low	VDDOB = 1.5V, 50Ω ext. load to 1.5V VDDOB = 1.8V, 50Ω ext. load to 1.8V	-	1.0 1.3	-	V
t <sub>r</sub> /t <sub>f</sub>	Rise and fall time (20% - 80%)	Preferred ext. load (R <sub>I</sub> )	50	-	110	pS
	Differential output skew	Preferred ext. load (R <sub>I</sub> )	-5	-	+5	pS
	Pre-Emphasis amplitude	Low mode High mode	-	+12.5 +25	-	%

The CML outputs are designed to avoid damage with inadvertent short-circuit connections to ground and VDD.

## External Interface

The SERDES high-speed serial buffers were optimized to interface externally to other similar buffers. Direct interconnection of Lattice SERDES buffers requires no external devices or components at the PCB level. Interconnection to other vendor's CML buffers is possible, but may require the addition of some passive components. CML buffers used in the Quad-SERDES macrocircuit provide internal ESD protection diodes which guarantee ESD to 2000V with Human Body Model testing and to 500V with Charged Device Model testing. The internal ESD diodes do place restrictions on allowable external voltage that can be safely applied to the high-speed I/O pins, as well as the I/O power supply inputs.

All interconnection circuits described in this section should use match length pairs of 50 ohm transmission line. Each will provide characteristic impedance termination of the line to provide maximum signal bandwidth. 50 ohms, an industry standard, provides maximum compatibility and suits present printed wiring board technology interconnections well, for circuit pack and backplane applications. It is also consistent with 100 ohm balanced transmission line interfaces which are becoming popular for high bandwidth shielded pair cable connections.

## LVDS Device Interface

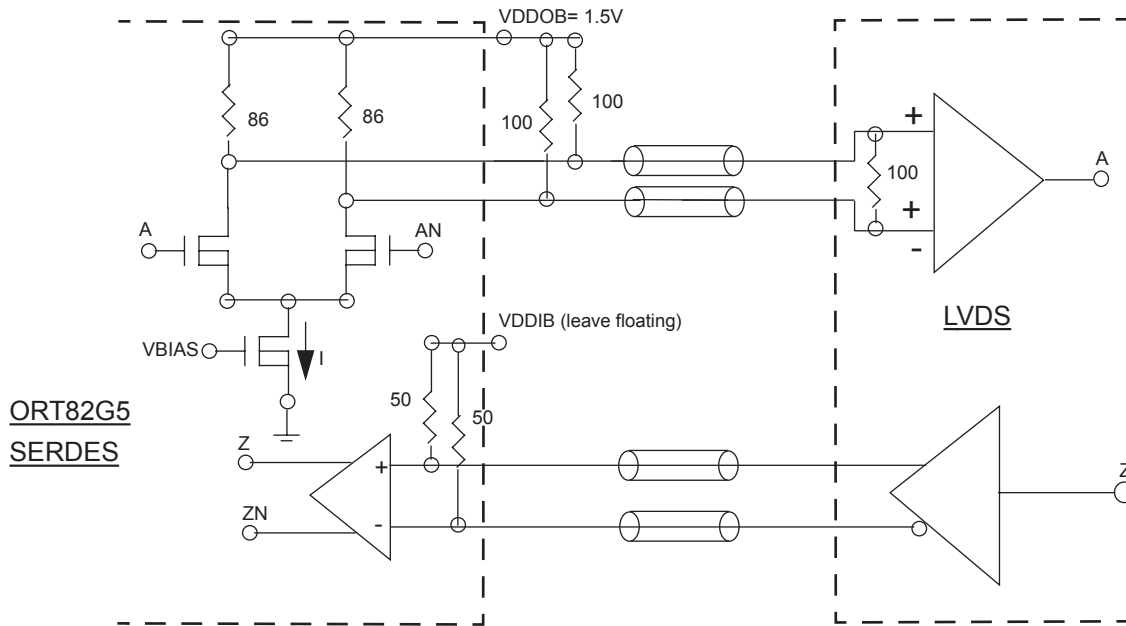
LVDS, like CML is intended for low-voltage differential signal point-to-point transmission (Reference 3). Many commercial LVDS devices provide internal 100 ohm input terminations. They are thus intended for use with 100 ohm characteristic impedance transmission line connections. Standard LVDS is specified with about 3 mA signal current which translates to a nominal signal voltage of 600 mVp-p (differential). Low power LVDS provides about 2 mA signal current. LVDS input and output parameters are shown in Table 3, as specified in the LVDS Standard.

**Table 3. LVDS Parameters**

Symbol	Parameter	Conditions	Min	Max	Units
Driver Specifications					
Voh	Output voltage high	Rload (dif)=100 ohm	-	1475	mV
Vol	Output voltage low	Rload (dif)=100 ohm	925	-	mV
Vod	Output differential voltage	Rload (dif)=100 ohm	250	400	mV
Ro	Output impedance, single ended	Vcm=1.0V to 1.4V	40	140	ohm
Receiver Specifications					
Vi	Input voltage range		0	2400	mV
Vidth	Input differential threshold		-100	+100	mV
Vhyst	Input differential hysteresis		25	-	mV
Rin	Receiver differential input impedance		90	110	ohm

Table 3 shows that LVDS devices have some degree of signal voltage range overlap with SERDES. Both use internal 100 ohm differential terminations at the receiver port. A direct interconnection of the two technologies, as shown in Figure 3, is therefore possible.

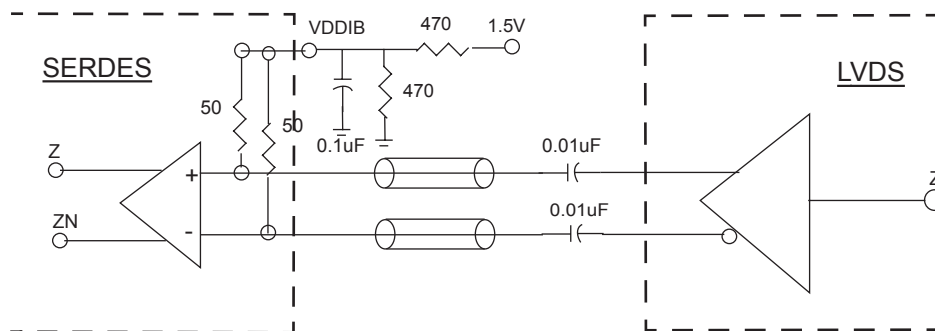
Figure 3. DC-Coupled SERDES CML to LVDS Interface



Within LVDS receivers, an internal input differential termination, of value 100 ohms, is typically provided. This termination resistor is usually floating with respect to ground. In the SERDES receiver the differential input termination resistor is center-tapped and biased to a voltage equal to 1.5V or 1.8V. This is required for proper operation of the output buffer. To properly drive the LVDS input from the SERDES output an external 100 ohm resistor to VDDOB is required on each output, as shown in Figure 3. Some LVDS devices provide a center-tapped input termination resistor, internally. If this center-tap is accessible, a capacitor to ground can be added to provide an additional level of immunity to system level common-mode noise.

In the LVDS to SERDES direction (lower portion of Figure 3), a floating input termination resistor may be provided by leaving the SERDES VDDIB pin floating. This provides a signal at the receiver input with a nominal common mode voltage of 1.2V. The maximum voltage swing at each input is +/- 200 mV. This is within the acceptable input voltage range of the receiver. A simple direct interface like this can be used in many applications. Higher common mode noise tolerance may be achieved with alternate ac-coupled LVDS driver to SERDES receiver connection, as shown in Figure 4.

Figure 4. AC Coupled LVDS to SERDES Scheme



The signal coupling capacitors and resistive voltage divider circuit is added to translate the LVDS output signal to the center of the SERDES input voltage range. This will increase the receiver tolerance to common-mode input noise voltage, and provide a higher tolerance range to common-mode and system and ground noise. Note that nominal resistor and capacitor values are shown in Figures 3 and 4. Optimum values will vary in each application.

Analog simulation of interface circuits can be a very useful part of the design process. As a simple example, the SERDES to LVDS interface portion of Figure is simulated, using the HSPICE models for the SERDES output buffer that is available from Lattice. Two 50 ohm ideal transmission lines of matched length were provided between the SERDES output and the LVDS input, representing PCB traces. Figure 5 shows the resulting signal voltage waveforms at the LVDS device input terminals, as predicted by simulation. Device package parasitic-elements were included. The P and N input common-mode (single-ended) and differential mode waveforms are shown. A random-digital signal pattern was used in the simulation to drive the SERDES buffer. Other parameters and conditions assumed were nominal IC processing parameters, nominal supply voltage and room temperature. Figure 5 shows a well behaved differential signal that should be an adequate LVDS input signal.

**Figure 5. SERDES to LVDS Signal Simulation - Nominal Case**

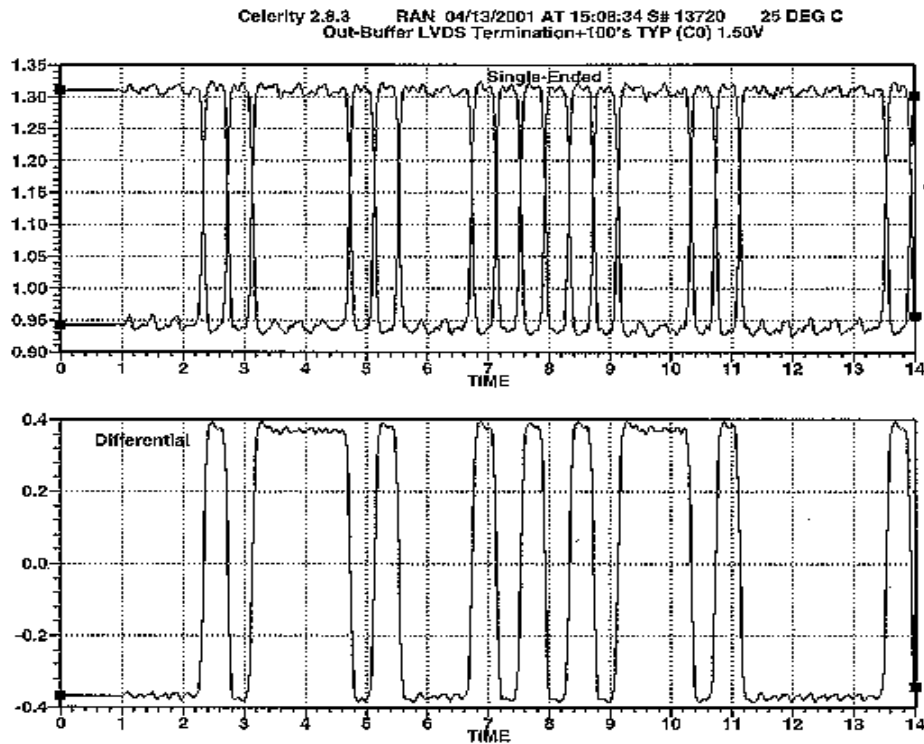
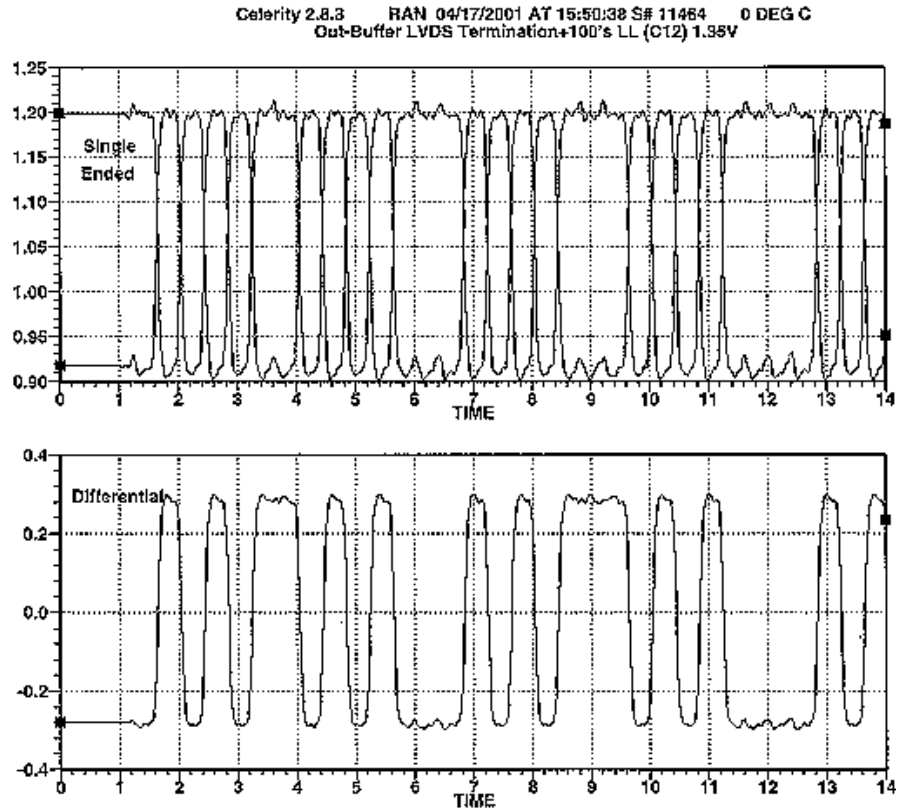


Figure 6 repeats the simulation of Figure 5, but under some worst case conditions. Extreme IC process parameters, low supply voltage, and 0 degree C temperature were assumed. The resulting waveforms in Figure 5 and 6 are well within the acceptable operating range of a typical LVDS device. One of the important functions of circuit simulation is to verify correct operation while varying parameters and operating conditions over the expected range of variation.

Figure 6. SERDES to LVDS Signal Simulation - Worst Case



## Low Voltage PECL Interface

Parameters for a typical LVPECL I/O device are listed in Table 4.

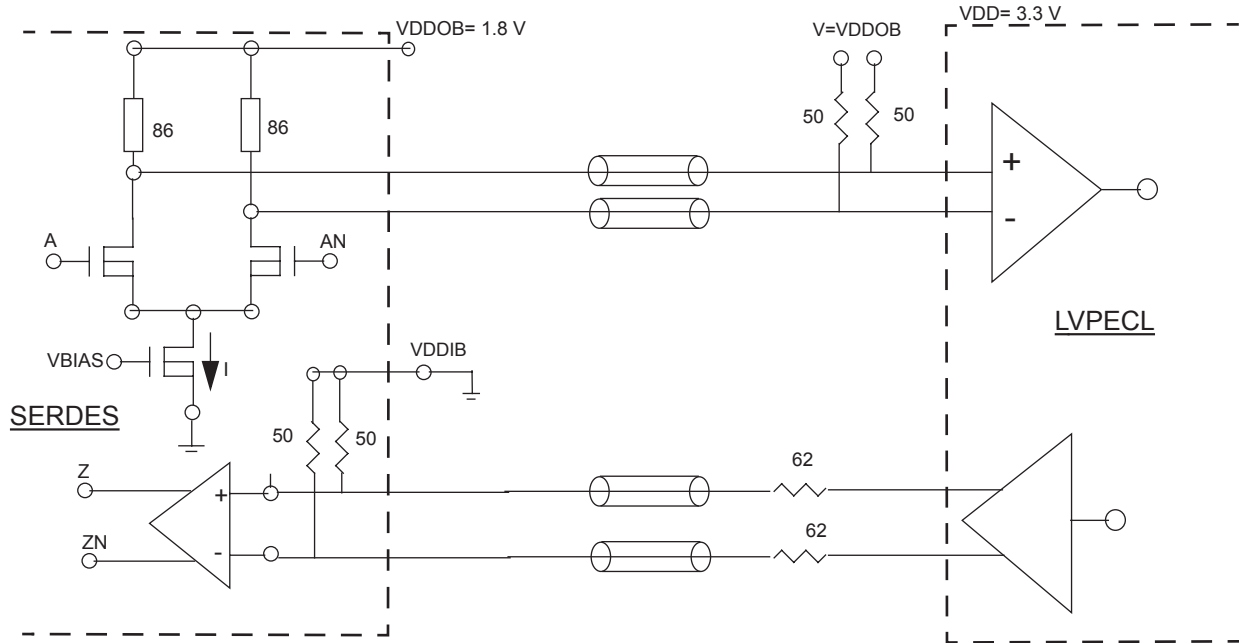
**Table 4. Typical LVPECL I/O Specifications**

Symbol	Parameter	Conditions	Min	Max	Units
Driver Specifications					
Voh	Output voltage high	Outputs terminated with 50 ohms to Vcc-2.0V	2215	2420	mV
Vol	Output voltage low	Outputs terminated with 50 ohms to Vcc-2.0V	1470	1680	mV
Vod	Output differential voltage	Outputs terminated with 50 ohms to Vcc-2.0V	535	950	mV
Ro	Output impedance, single ended	Vcm=1.0V to 1.4V	3	10	ohm
Receiver Specifications					
Vi	Input voltage range, common-mode	< 500mVp-p > 500mVp-p	1.1 1.3	3.1 3.1	V
Vin-diff.	Input voltage range, differential-mode		200	> 2000	mVp-p
Iih	Input HIGH current		-	150	uA
Iil	Input LOW current		-600	-	uA
Rin	Receiver differential input impedance	No internal termination resistor provided	>> 50	-	ohm

A comparison of Table 4 with Tables 1 and 2 will show that significant signal I/O voltage and termination differences exist between LVPECL and SERDES. In both signal directions there is almost zero overlap in signal voltage range. To interface these technologies, signal voltage offset must be provided by the interconnection circuit.

The proposed circuit for SERDES to LVPECL interconnection is shown in Figure 7.

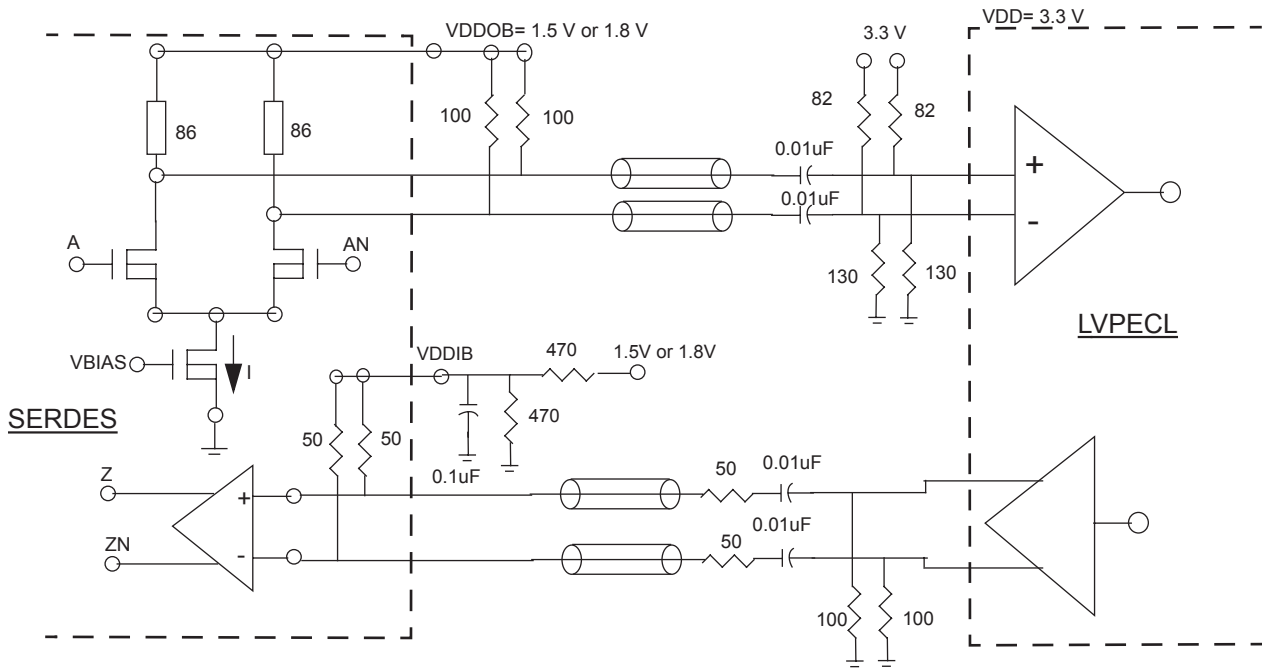
Figure 7. DC-Coupled LVPECL Interface



The circuit of Figure 7 minimizes external components and provides dc-signal coupling. The SERDES VDDOB supply is used at the LVPECL input to bias the two 50 ohm termination resistors, which characteristically terminate the transmission lines used for interconnection. The higher VDDOB value of 1.8V is preferred here to better align signal voltages. The LVPECL driver output bias current flows through the series 62 ohm resistors and the SERDES input internal 50 ohm termination resistors. This configuration provides the voltage offset and attenuation required for proper interface to the SERDES receiver. It also provides the matched transmission line termination for the interconnection.

Figure 8 shows an ac-coupled SERDES/ECL interface

Figure 8. AC-Coupled LVPECL Interface.



This interface circuit requires a higher number of external components than the dc-coupled method, but will provide tolerance to higher levels of common-mode system and ground noise. This is achieved by biasing the signal common-mode voltage level near the center of the input range, at each receiver. This method offers flexible signal offset capability and can be adapted for use with 5V PECL and -5V ECL interface applications. For these cases, bias voltage and resistor value modifications are required.

Note that nominal resistor and capacitor values are shown in Figure 7 and Figure 8. Optimum values may vary in each application.

## PCB, Connector and Cable Considerations

The sub-nanosecond rise time of the SERDES signals require very careful interconnection design techniques be used at the PCB level. The key to successful interconnection is using consistent transmission line paths with minimal discontinuities and true characteristic-impedance termination at the receive end of the line. Multi-layer laminated PCB backplanes and daughter cards are recommended, for best results. Use of controlled impedance connectors, PCB lines and cables provide the best result. Extensive test results for the ORT82G5 driving through a real backplane system, can be found in Reference 3. A good discussion of high-frequency PCB design considerations can be found in Reference 4.

## Conclusions

Lattice SERDES serial I/O can be interfaced to LVDS, LVPECL, PECL and ECL technologies, as was described in this document. As with any high-speed electrical interface, success depends on very careful design at all levels, including the device package and printed wiring board design. Designers should follow good high-frequency PCB design practices, as described in Reference 4.

HSPICE models of the SERDES input and output buffers can be obtained through Lattice Sales personnel. It is highly recommended that they be used to verify the performance of SERDES interface circuits, in all applications. High-frequency HSPICE models are available for many passive and active commercial components. Including these will increase the accuracy of the simulation results and provide higher confidence in the design integrity.

## References

1. **ORCA ORT82G5 SERDES Backplane Interface FPSC**, Lattice Data Sheet, April 2002
2. **IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)**, IEEE Std 1596.3-1996
3. **ORT82G5 FPSC High-speed Backplane Measurements**, Lattice Technical Note 1027
4. **High-speed PCB Design Considerations**, Lattice Technical Note