

Introduction

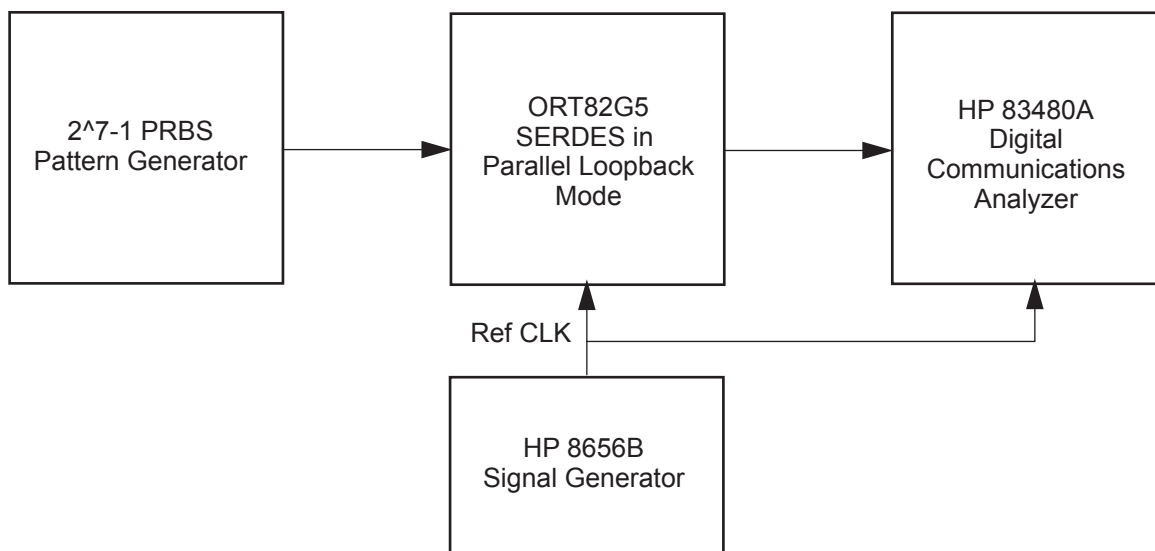
The ORT82G5 Field Programmable System Chip (FPSC)¹ contains two quad SERDES backplane interface blocks. The two quad SERDES provide eight high-speed serial channel interfaces that are capable of data rates up to 3.7 Gbits/s. Each channel can transmit and receive simultaneously and provides full clock and data recovery. At high data rates, jitter becomes a critical characteristic for error-free data transfer. This document discusses the device jitter performance and presents laboratory test results showing SERDES transmit and receive jitter characteristics. The test data was taken using a test chip that contained one quad macrocell, identical to the two quad macrocells on the ORT82G5.

Transmit Jitter

Total Jitter Measurement

The laboratory test setup used to measure total SERDES transmit jitter, is shown in Figure 1.

Figure 1. Transmit (Total) Jitter Measurement Setup



The serial data rate for this test is 3.125 Gbits/s. A pseudo random bit stream test data pattern is applied to a SERDES channel, configured in parallel loop-back mode. The transmitter output waveform is observed in eye-diagram form with a HP83480A sampling digital communications analyzer. Peak-to-peak and RMS time-jitter at the 50 percent crossing level are calculated by the analyzer. The automated measurement process followed by the DCA includes digitizing waveform segments of the incoming data signal into 1350 data point sets, and acquiring 3000 of these waveform segments to calculate the jitter statistical parameters.

Test results are shown in Table 1. Three different devices with intentionally varied manufacturing process parameters, were used in this experiment. The designations Fast, Nominal and Slow are used in Table 1 to indicate the direction of each device bias. The purpose was to broaden device population that was represented in the experiment. Temperature and supply voltage variations were also included in the experiment.

Table 1. Transmit Jitter Measurement Result

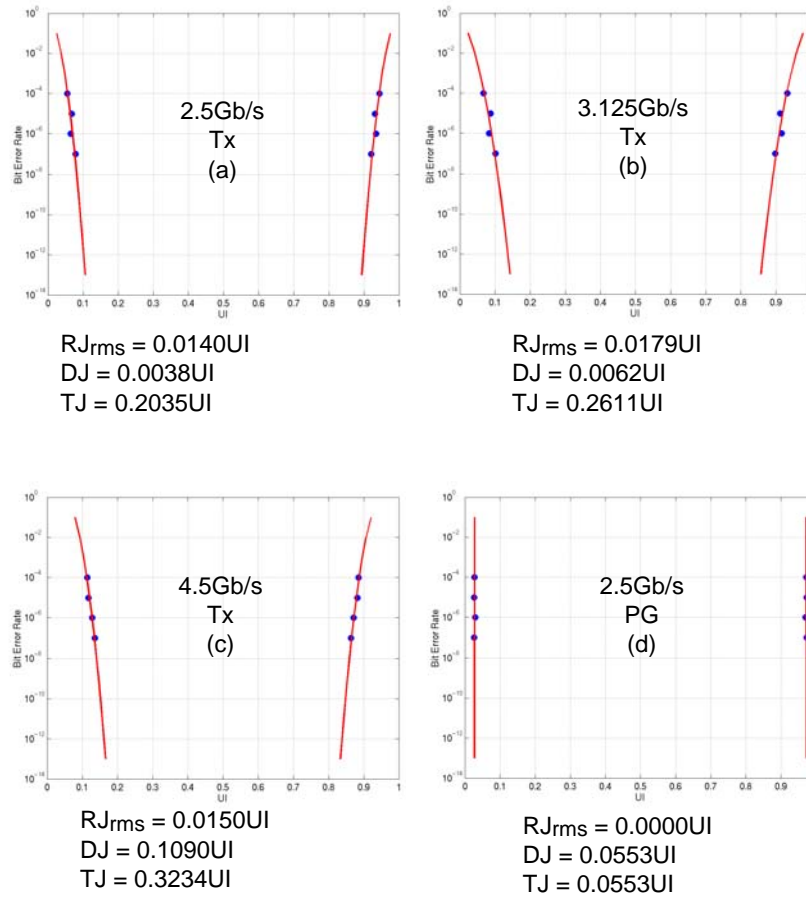
Device	Ambient Temperature	Voltage (V)	Tx Jitter pS RMS	Tx Jitter pS p-p	Tx Jitter (UI)
Nominal	0°C	1.5	6.0	40.0	0.125
Nominal	25°C	1.5	6.1	46.7	0.146
Nominal	85°C	1.5	6.2	44.4	0.139
Slow	0°C	1.5	6.5	46.7	0.146
Slow	25°C	1.5	6.6	44.4	0.139
Slow	85°C	1.5	7.2	48.9	0.153
Slow	85°C	1.575	7.2	51.1	0.160
Fast	0°C	1.5	5.7	42.2	0.132
Fast	25°C	1.5	6.8	46.7	0.146
Fast	85°C	1.5	7.9	55.6	0.174
Fast	0°C	1.575	5.5	42.2	0.132
Fast	0°C	1.425	8.3	53.3	0.167

The worst-case measurement seen in Table 1 shows a RMS jitter value of 8.3 pS and peak-to-peak value of 0.174 UI. All values in Table 1 are within the acceptable total jitter range for XAU1³, Fibre Channel⁴, and Infiniband⁵ standards, although the test pattern used may not be the specific type specified in each standard.

Jitter Component Measurement

Emerging high-speed interface standards are requiring that the different jitter components be identified in measurements, and that each conform to specified limits. Appropriate measurement methods are still being devised and debated. One common measurement method for decomposing the total jitter (TJ) into a random component (RJ) and a deterministic component (DJ) is described in Reference 2. It uses a Bit-Error Rate Tester (BERT) combined with a Time Interval Analyzer (TIA) to generate transmit jitter bathtub-curve characterization. This is also discussed in Reference 2. Preliminary bathtub-curve testing of the ORT82G5 SERDES has been performed. Resulting bathtub-curves and the corresponding jitter component levels are shown in Figure 2. Curves measured at several different transmit data rates are shown, along with resulting jitter component breakdown for each curve.

Figure 2. Preliminary Bathtub-Curve Measurement Results



RJ = Random Jitter
 DJ = Deterministic Jitter
 TJ = Total Jitter

Receive Jitter Tolerance

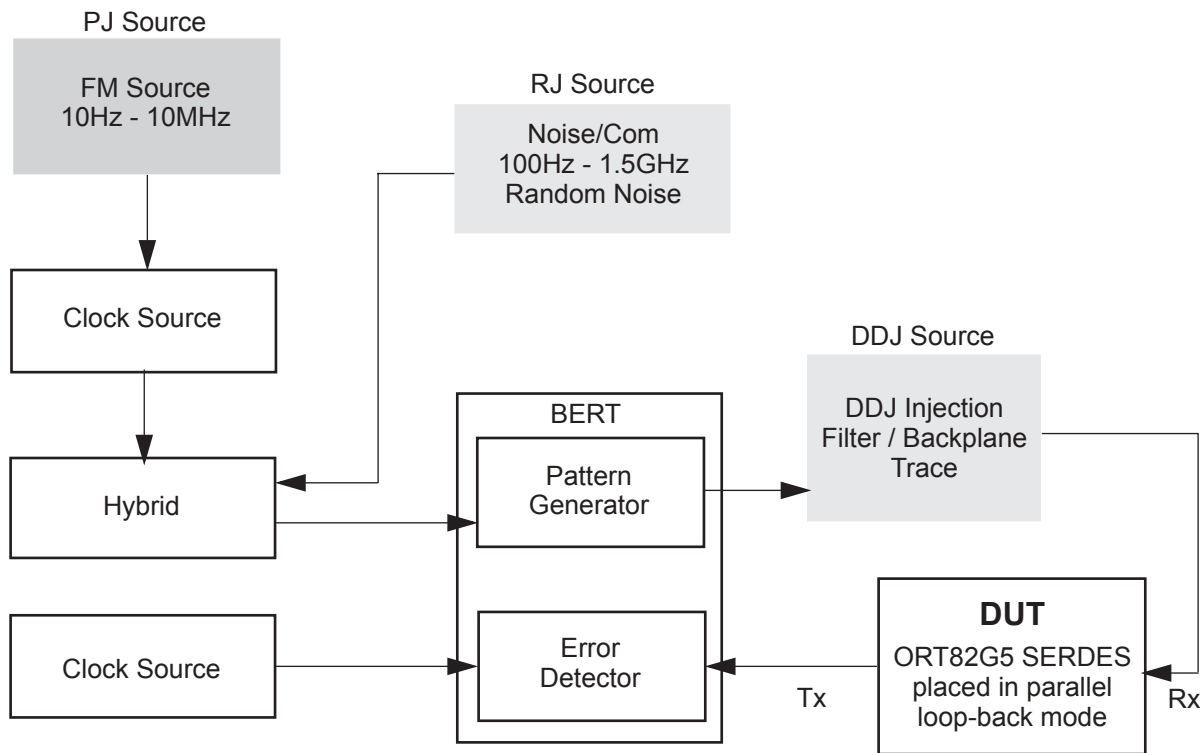
Receive jitter tolerance is a critical system interface parameter. It indicates the ability of the SERDES receiver to recover incoming serial data in the presence of transit signal jitter and path generated jitter that is generally additive. Such jitter will be present in all applications, in varying degrees, but must be kept within the limits of the receiver.

A receiver's ability to tolerate incoming signal jitter is very dependent on jitter type. High-speed serial interface standards have recognized this fact and have recently modified specifications to indicate tolerance levels for the different jitter types (such as those described in Section 2).

Jitter Tolerance Measurement

As with transmit jitter measurement methods, receive jitter tolerance measurement methods have not been firmly established. Preliminary test efforts have defined one test method which provides jitter components and levels as defined for the 10G Ethernet XAU1 standard³. The test setup for this method is shown in Figure 3.

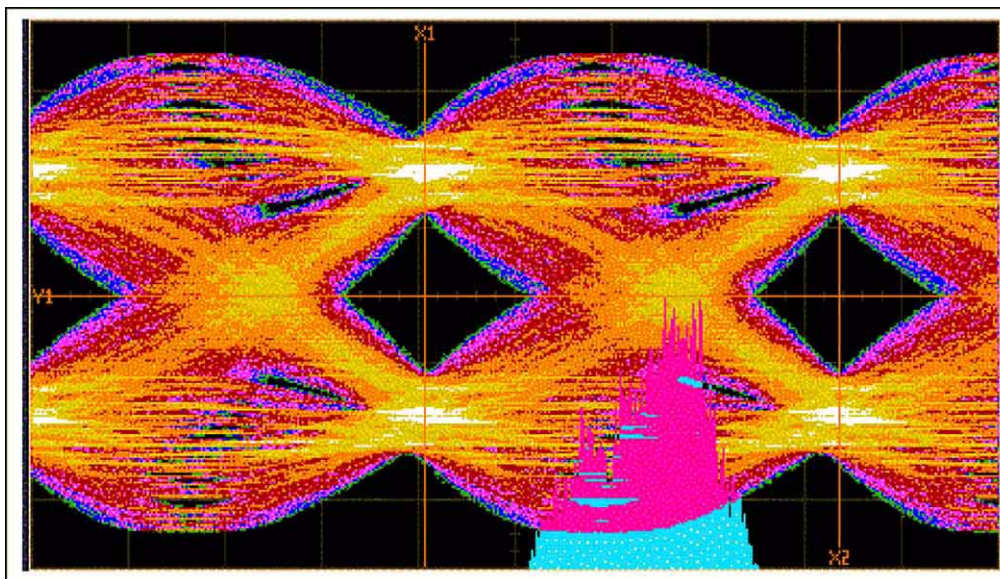
Figure 3. XAUI Receiver Jitter Tolerance Test Setup



PJ = sinusoidal periodic jitter
 RJ = random jitter
 DDJ = data dependent jitter

A detailed discussion of the test setup and procedure may be found in Reference 2. The measured eye-diagram of the incoming signal to the DUT in Figure 3, is shown in Figure 4.

Figure 4. Eye-Diagram for Receive Jitter Tolerance Test of Figure 3



Note that Figure 4 also shows a density function of the waveform level transition crossings through the center (horizontal) axis, between the second and third eye openings.

Jitter Tolerance Results

A pass/fail test was performed. Each jitter source component in the setup was adjusted to XAUI specified levels³. The same SERDES devices tested in Section 2 (and listed in Table 1) were used in this experiment. All temperature and supply voltage parameter levels, as specified in Table 1, were included in this testing. A CJT test data pattern was used. All testing performed passed the test criteria with measured bit error-rates of less than 1E-12.

Conclusion

Lattice FPSC SERDES transmit jitter generation and receive jitter tolerance have been measured and the results described. The results to date indicate excellent device performance in both of these areas. A summary of jitter requirements is shown in Table 2.

Table 2. Summary of Standards Jitter Requirements

Standard	Tx-Total Jitter	Rx-Jitter Tolerance
XAUI	0.35 UI	0.65 UI
Fibre Channel	0.65 UI*	0.70 UI*
Infiniband	0.35 UI	0.65 UI

*This standard is presently only specified at 1.065 Gbits/s rate

For the limited device test group used, all the transmit total-jitter measurement results were well within the limits of all three standards listed in Table 2. The XAUI receive jitter-tolerance tests showed standard limit compliance for the entire test group.

As system designers realize the importance of device jitter performance, standards and measurement methods are evolving and becoming more sophisticated. Additional device characterization is anticipated as the high-speed serial data interface standards mature.

References

1. Lattice ORT82G5 Field Programmable System Chip, Data Sheet
2. Jitter Testing for Multi-Gigabit Backplane SERDES, IEEE 2002 International Test Conference, Proceedings draft
3. IEEE Draft P802.3ae/D3.3, XGMII/XGMS/XAUI section, October 2001
4. FIBRE CHANNEL 10 Gigabit (10GFC), T11/Project 1413-D/Rev 1.1, May 11, 2001
5. InfiniBand Architecture Specification Volume 2, Release 1.0-a, June 19, 2001