

Introduction

The ispGDX2™ V/B/C devices are built from the latest 1.8V core E²CMOS[®] technology. The ispGDX2V/B device family uses an internal voltage regulator to interface with the 3.3V/2.5V power supply. As a result, a given ispGDX2V/B device will have a higher static power component compared to the similar density 1.8V core ispGDX2C device. The design of each of these device families is based on the advanced low-power electrically erasable non-volatile memory cell with a full CMOS logic design approach.

Power Calculation

This technical note explains how to estimate power consumption of the ispGDX2 device based on the device utilization. It is assumed that user has knowledge of the ispGDX2 architecture. The information for device utilization is generated by the ispGDX2 Compiler report file.

Power consumption in the ispGDX2 family is the sum of three components:

$$\begin{aligned}
 I_{CC} &= I_{CORE} + I_{PLL} + I_{HSI} \\
 I_{CORE} &= I_{DC} + I_{REF} + I_{IN} \\
 I_{DC} &= \text{Blank chip background current including power regulator current} \\
 I_{REF} &= K_{REF} * \text{Number of banks with } V_{REF} \text{ active} \\
 I_{IN} &= (K_{IN} * \text{Number of inputs} + K_{CORE}) * \text{Average input switching frequency (MHz)} \\
 I_{PLL} &= I_{PLLACTIVE} + I_{PLLSTBY} \\
 &= (K_{PLL} * F_{VCO} + K_{PLLSTBY}) * \text{Number of PLLs used} \\
 I_{HSI} &= I_{HSIACTIVE} + I_{HSISTBY} \\
 &= (K_{HSI} * \text{Mbps} + K_{HSISTBY}) * \text{Number of sysHSI}^{\text{TM}} \text{ Blocks used}
 \end{aligned}$$

Where

K_{REF} :	Reference voltage circuit current per bank
K_{IN} :	I/O current per input per MHz
K_{CORE} :	Core current per MHz with GRP fanout of 1
K_{PLL} :	PLL current per MHz per PLL
$K_{PLLSTBY}$:	PLL standby current per PLL
F_{VCO} :	VCO frequency
K_{HSI} :	HSI current per Mbps per sysHSI Block
$K_{HSISTBY}$:	HSI standby current per sysHSI Block

I_{CC} Calculation Example

Assume the following operational conditions:

- Room temperature
- V_{CC} = 1.8V
- 64 inputs are used at average switching frequency of 20 MHz
- Four sysHSI Blocks are configured at 622 Mbps
- Two sysCLOCK™ PLLs are used
- sysCLOCK PLL Input Freq (F_{IN}) = 100 MHz and N (Multiplier) / M (Divider) = 4:
- F_{VCO} = 400 MHz
- One GRP fanout per input
- All eight banks use V_{REF}

$$\begin{aligned}
 I_{CC} &= I_{CORE} + I_{PLL} + I_{HSI} \\
 &= I_{DC} + I_{REF} + I_{IN} + I_{PLLACTIVE} + I_{PLLSTBY} + I_{HSIACTIVE} + I_{HSISTBY} \\
 &= I_{DC} + K_{REF} * \text{Number of Banks} \\
 &\quad + (K_{IN} * \text{Number of inputs} + K_{CORE}) * \text{Average input switching frequency (MHz)} \\
 &\quad + (K_{PLL} * F_{VCO} + K_{PLLSTBY}) * \text{Number of PLLs used} \\
 &\quad + (K_{HSI} * \text{Mbps} + K_{HSISTBY}) * \text{Number of sysHSI Blocks used} \\
 &= 23.2 + 1.334 * 8 \\
 &\quad + (0.0213 * 64 + 0.239) * 20 \\
 &\quad + (0.064 * 400 + 5.5) * 2 \\
 &\quad + (0.091 * 622 + 3) * 4 \\
 &= 367 \text{ mA}
 \end{aligned}$$

I_{CC} estimates are based on typical conditions (V_{CC} = 1.8V, room temperature). These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
 1-408-826-6002 (International)
 e-mail: techsupport@latticesemi.com