

## Introduction

This technical note provides general guidelines for a solder reflow and rework process for Lattice surface mount products. The data used in this document is based on IPC/JEDEC standards. Each board has its own profile which depends upon the reflow equipment used and the board design. The PCB must be individually characterized to find the reliable profile. This document covers both the SnPb Eutectic process and the Pb-Free process.

## Reflow

- Use caution when profiling to insure the maximum temperature difference between components is less than 10°C (7°C within an individual component).
- Forced convection reflow with nitrogen is preferred (with maximum oxygen content of 50-75 PPM).

## Inspection

- Pre-reflow: Use visual inspection to verify solder paste dispense location and quantity.
- Pick and Place: Use machine vision as necessary to ensure proper component placement.
- Post reflow: Use electrical testing to verify solder joint formation (100% post-reflow visual inspection is not recommended).

## Cleaning Recommendations

- After solder reflow, printed circuit boards should be thoroughly cleaned and dried using standard cleaning equipment.
- Final rinse should be warm DI water (50° to 75°C) with resistivity of 0.2 Meg Ohms/cm or greater.
- After cleaning, boards should be baked for a minimum of 1 hour at 125°C to evaporate residual moisture.

## Rework Recommendations

Removal and replacement of SMT packages on printed circuit boards is fairly straightforward. However, reattachment or touch-up of SMT packages that have already been soldered to the board is not practical in most cases.

A few important criteria should be considered when choosing a rework system:

- Minimize the change in temperature across the solder joint array to promote good solder joint formation, minimize intermetallic growth, improve solderability and minimize component warpage.
- Minimize die temperature to prevent die delamination and wire bond failure.
- Minimize board temperature adjacent to the rework site to reduce intermetallic growth, prevent secondary reflow, and prevent possible component delamination.
- For boards with no internal ground plane, apply localized heat to the SMT package. When the solder is molten, remove package using appropriate vacuum tool.
- While the board is still hot, remove excess solder from the site using a vacuum desoldering system or a soldering iron and solder wicking material. Use care to avoid damaging the solder pads or the surrounding solder mask.
- For PCBs with internal ground plane(s), preheat the entire board to at least 80°C before removing the SMT packages.
- Use alcohol to remove residual flux, then wash the entire board using the standard board cleaning process before attempting to replace SMT components.

## BGA Reballing

BGA reballing is not recommended. Reballled BGA packages will void the original Lattice specifications.

## Pb-Free/RoHS-Compliant Products

All Lattice Pb-Free products are also fully RoHS compliant. Lattice offers a broad range of Pb-Free/RoHS-compliant products in a variety of package configurations. These packages include the Thin Quad Flat Pack (TQFP), Quad Flat Pack (QFN), Fine Pitch BGA (fpBGA), Fine Pitch Super BGA (fpSBGA) and Chip-Scale BGA (csBGA).

Lattice Pb-Free packages are qualified to a Level 3 moisture resistance (or better) with peak reflow temperatures of 245°C (large sized packages), 250°C (medium sized packages) or 260°C (small sized packages), consistent with IPC/JEDEC J-STD-020C, *Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices*. See Table 1 for specific reflow temperature by package. Reliability tests include high temperature operating life (HTOL), surface mount preconditioning testing, temperature cycling, moisture resistance testing, biased highly accelerated stress test (HAST) and unbiased HAST. Data for these tests are available upon request.

## Peak Reflow Temperature ( $T_P$ ) by Package Size

Table 1 illustrates the peak reflow temperatures by package size. Refer to the *Package Diagrams* document on the Lattice web site at [www.latticesemi.com](http://www.latticesemi.com). Use maximum package dimensions to determine package thickness and volume.

**Table 1. Peak Reflow Temperature ( $T_P$ )**

Classification	Package Thickness	Volume < 350 mm <sup>3</sup>	Volume = 350 - 2000 mm <sup>3</sup>	Volume > 2000 mm <sup>3</sup>
SnPb Eutectic Package	< 2.5 mm	240 + 0/-5°C	225 + 0/-5°C	
	≥ 2.5 mm	225 + 0/-5°C		
Pb-Free Package	< 1.6 mm	260 + 0/-5°C		
	1.6 mm to < 2.5 mm	260 + 0/-5°C	250 + 0/-5°C	245 + 0/-5°C
	≥ 2.5 mm	250 + 0/-5°C	245 + 0/-5°C	

Note: Package volume excludes external terminals (balls, bumps, lands, leads) and non-integral heat sinks.

Table 2 shows the peak reflow temperature for Lattice devices by package type and size.

**Table 2. Peak Reflow Temperature ( $T_P$ ) by Package Type and Size**

Package Type	Number of Pins/Balls	Peak Reflow Temperature (+0/-5°C)	
		SnPb	Pb-Free <sup>1</sup>
DIP (Ceramic 300mil)	20	225	N/A
	24	225	N/A
DIP (Plastic)	16	225	245
	20	225	245
	24	225	245
	28	225	245
BGA	272	225	250
	388	225	250
	492	225	250
caBGA	49	240	260
	100	240	260

Table 2. Peak Reflow Temperature ( $T_P$ ) by Package Type and Size (Continued)

Package Type	Number of Pins/Balls	Peak Reflow Temperature (+0/-5°C)	
		SnPb	Pb-Free <sup>1</sup>
CPGA	84	225	N/A
	133	225	N/A
csBGA	56	240	260
	132	240	260
fpBGA	100	240	260
	144 <sup>2</sup>	225	250
	208	225	250
	256	225	250
	388	225	250
	416	225	250
	484	225	250
	516	225	250
	672	225	250
	676	225	250
	680	225	250
	900	225	250
fpSBGA	680	225	245
	1036	225	N/A
JLCC	44	225	N/A
	68	225	N/A
LCC	20	240	N/A
	28	240	N/A
MQFP	240	225	N/A
	304	225	N/A
PLCC	20	225	250
	28	225	245
	44	225	245
	68	225	245
	84	225	245
PQFP	100	225	245
	120	225	245
	128	225	245
	144	225	245
	160	225	245
	208	225	245
	240	225	N/A
	304	225	N/A
QFN	32	240	260
ftBGA	256	240	260
	324	240	260

Table 2. Peak Reflow Temperature ( $T_P$ ) by Package Type and Size (Continued)

Package Type	Number of Pins/Balls	Peak Reflow Temperature (+0/-5°C)	
		SnPb	Pb-Free <sup>1</sup>
SBGA <sup>2</sup>	256	225	250
	320	225	250
	352	225	250
	432	225	250
	600	225	N/A
SOIC <sup>2</sup>	16	225	N/A
	20	225	N/A
	24	225	N/A
	28	225	N/A
SSOP	28	225	N/A
TQFP (thickness: 1.0mm)	44	240	260
	48	240	260
TQFP (thickness: 1.4mm)	44	240	260
	48	240	260
	100	240	260
	128	240	260
	144	225	260
	176	225	260

1. Not all device/package combinations are offered in the Pb-Free configuration.

2.  $T_P$  for these packages are qualified at a lower temperature than the JEDEC standard and are subject to change in the future.

## Reflow Profile for SMT Packages

The typical reflow process includes four phases.

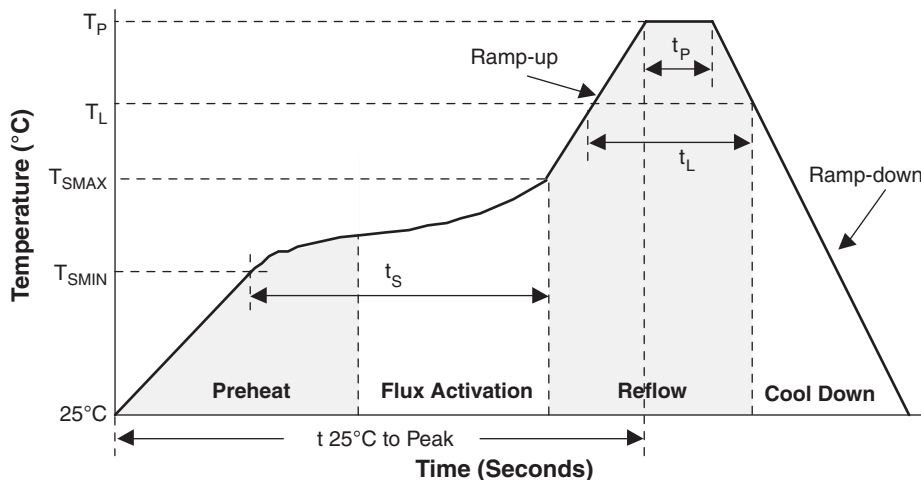
- Preheat** – Brings the assembly from 25°C to  $T_S$ . During this phase the solvent evaporates from the solder paste. Preheat temperature ramp rate should be less than 2°C/second to avoid solder ball spattering and bridging.
  - Solder Ball Spattering – The most common solder balling defect is spattering which is caused by explosive evaporation of solvents. It can be eliminated by a slower temperature rise in the preheat phase.
  - Bridging – Often seen on fine pitch components and usually caused by inaccurate or splashy screen printing. But it can also be a result of solder paste slumping caused by rapid temperature rise in the preheat phase.
- Flux Activation** – The temperature rises slowly and reaches a point at which the flux completely wets the surfaces to be soldered.
- Reflow** – In this phase, the temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
- Cool Down** – Ramp down rate should be as fast as possible in order to control grain size, but should not exceed 6°C/second.

Table 3 and Figure 1 describe the reflow profile.

Table 3. Reflow Profiles

Parameter	Description	Sn-Pb Eutectic Package	Pb-Free Package
Ramp-Up	Average Ramp-Up Rate ( $T_{SMAX}$ to $T_P$ )	3°C/second max.	3°C/second max.
$T_{SMIN}$	Preheat Peak Min. Temperature	100°C	150°C
$T_{SMAX}$	Preheat Peak Max. Temperature	150°C	200°C
$t_S$	Time between $T_{SMIN}$ and $T_{SMAX}$	60-120 seconds	60-180 seconds
$T_L$	Solar Melting Point	183°C	217°C
$t_L$	Time Maintained above $T_L$	60-150 seconds	60-150 seconds
$t_P$	Time within 5°C of Peak Temperature	10-30 seconds	20-40 seconds
Ramp_Down	Ramp-down Rate	6°C/second max.	6°C/second max.
$t_{25°C\ to\ T_P}$	Time from 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Figure 1. Thermal Reflow Profile



### Technical Support Assistance

Hotline: 1-800-LATTICE (North America)  
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