

Introduction

In order to optimize speed in Lattice devices such as the ispMACH™ 4000 and MachXO™, device inputs are configurable with internal pull-up, pull-down, bus-hold latch or no bus maintenance. Typically, inputs can tolerate rise and fall times in the 50ns to 100ns range. When interfacing to slow input signals with input rise and fall time in hundreds of nanoseconds, external board design techniques are necessary to make the slow input signals immune to input noise that may be injected. This technical note suggests a few such techniques.

Input Circuit Techniques

Simple external circuitry along with the internal bus maintenance circuit can significantly improve slow rising and falling input noise immunity. Three common methods are described below.

Figure 1. Method 1: Input Series Resistor

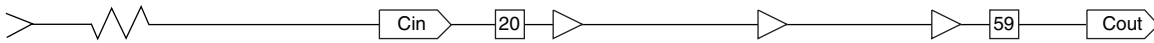


Figure 2. Method 2: Input and Feedback Resistor

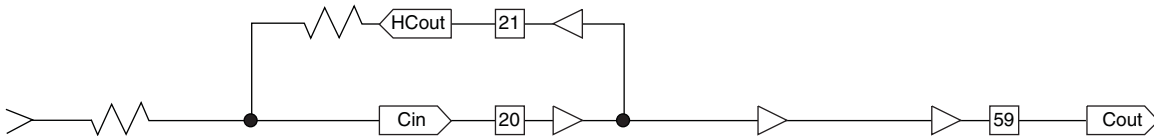
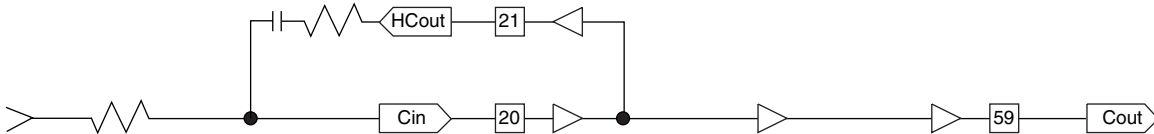


Figure 3. Method 3: Input Resistor and Feedback Capacitor



The following experimental data was collected to demonstrate the improvement that can be achieved with the different methods as compared to inputs without any external circuitry. The tables below highlight the maximum input rise (t_{RISE}) and fall (t_{FALL}) time of the results.

Test Device: MachXO
I/O Standard: LVCMOS 3.3V with input bus-hold latch turned on
Temperature: Room temperature

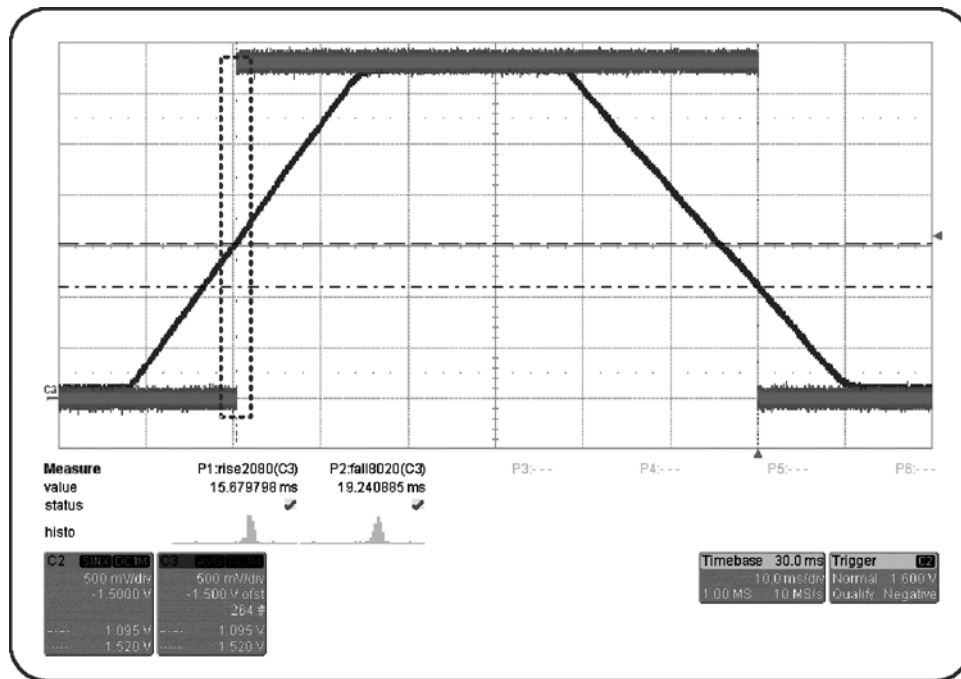
External Input Circuit	Input Series Resistor	t_{RISE}	t_{FALL}
None	—	<54ns	<56ns
Method 1	100Ω	65ns	63ns
	470Ω	500s	470μs
	680Ω	>15ms	>15ms

Test Device: ispMACH 4128V
I/O Standard: LVCMOS 3.3V with input bus-hold latch turned on
Temperature: Room temperature

External Input Circuit	Input Series Resistor	Feedback Resistor or Capacitor	t _{RISE}	t _{FALL}
None	—	—	<100ns	<100ns
Method 1	100Ω	—	220ns	155ns
	1KΩ	—	2μs	1.5μs
	4.7KΩ	—	6μs	7μs
Method 2	100Ω	1KΩ	800ns	300ns
		560Ω	700ns	350ns
	1KΩ	10KΩ	5μs	1.9μs
Method 3	100Ω	33pF	700ns	350ns
		100pF	2μs	600ns
	1KΩ	33pF	5μs	1.5μs

The plots below are measured with the ispMACH 4000. A 4.7 KOhm resistor is used in Method 1. The I/Os are configured as 'bus-hold'.

Figure 4. Normal View (Input Measured Before Series Resistor)



— Input
 ■ Output

Figure 5. Figure 1 Input Area (Zoomed View)

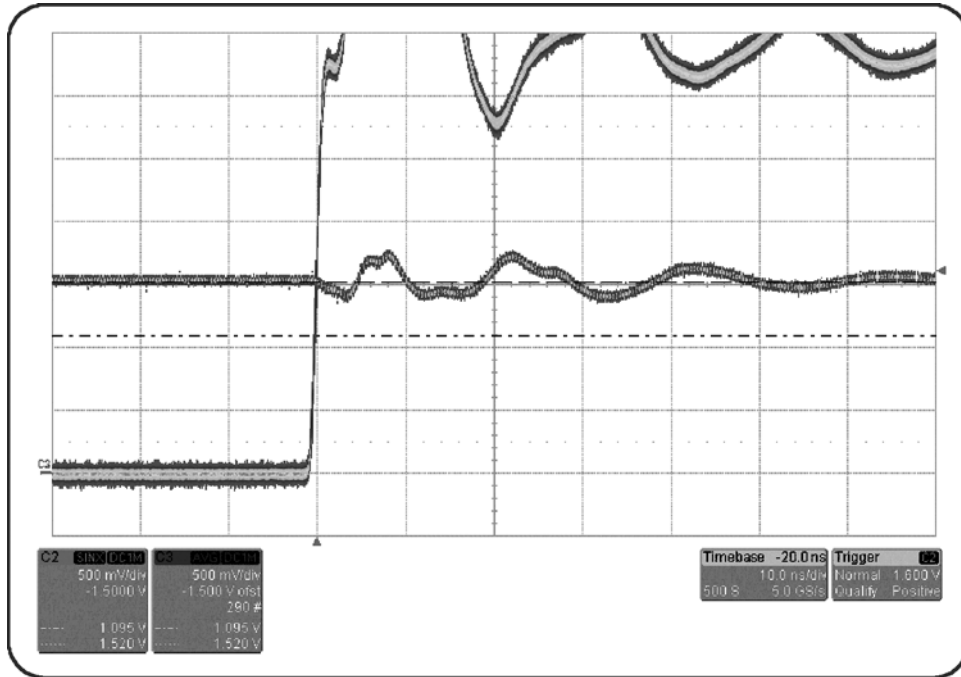
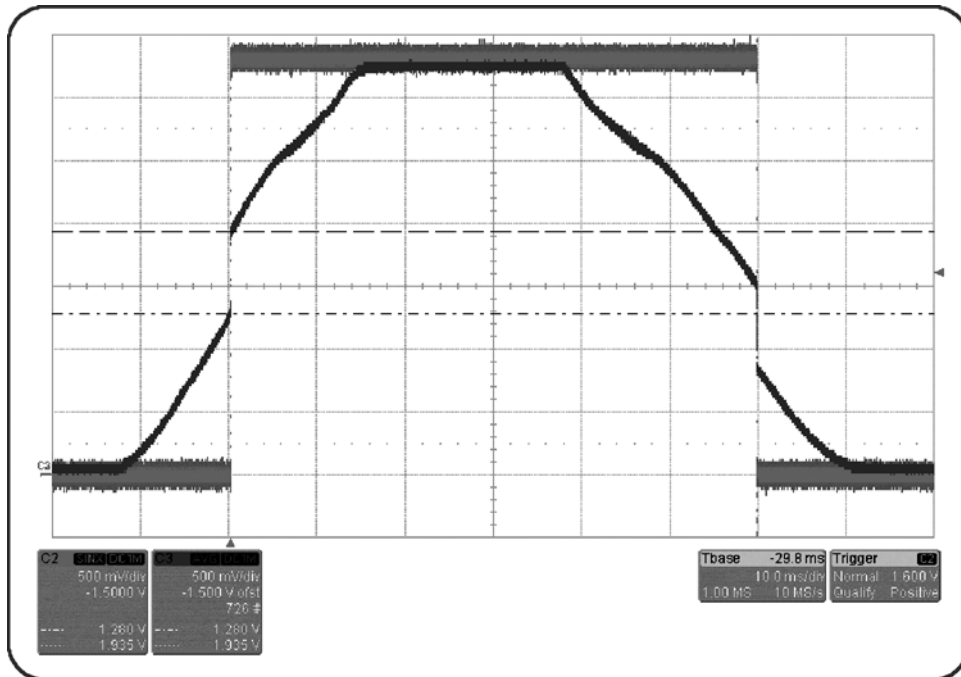


Figure 6. Input Measured After Series Resistor



Summary

As the data indicate, even with the very simple input series resistor used in Method 1 and the CPLD internal input bus-hold latch, maximum input rise and fall times will extend to hundreds of nanoseconds to microseconds.

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