

LatticeXP2 Family

flexiFLASH: Instant-On, Secure, Single-Chip FPGA

LatticeXP2™ devices combine a Look-up Table (LUT) based FPGA fabric with Flash non-volatile cells in an architecture referred to as flexiFLASH™.

The flexiFLASH approach provides a single chip solution with benefits such as instant-on operation, on-chip storage featuring FlashBAK™ embedded block RAM backup, access to general-purpose Serial TAG memory and inherent design security. LatticeXP2 devices also support Live Update field reconfiguration with TransFR™, 128-bit AES bitstream encryption and Dual Boot technologies.

The LatticeXP2 FPGA fabric utilizes an underlying LatticeECP2™ architecture that was optimized from the outset with high performance and low cost in mind. LatticeXP2 devices support 4-input LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O and enhanced sysDSP™ blocks.

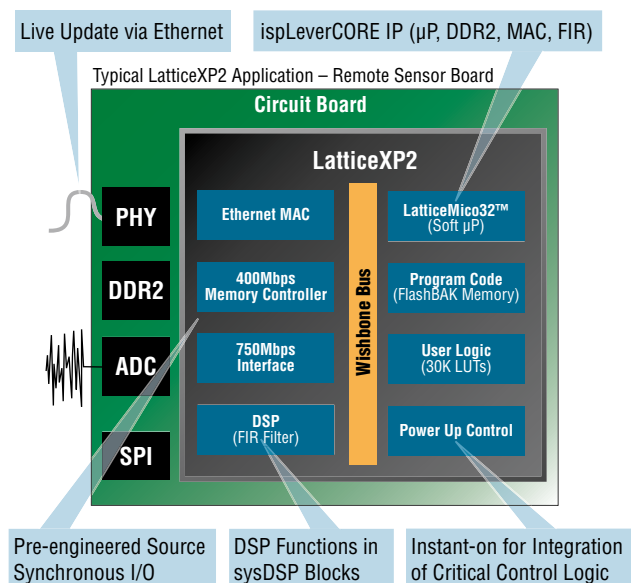
Lattice's ispLEVER® design tool allows complex designs to be efficiently implemented using the LatticeXP2 family of FPGAs. The ispLEVER tool is complemented by pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeXP2 family. By using these standardized IP blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.



Key Features and Benefits

- **flexiFLASH Architecture**
 - Instant-on (1mS), single chip integration
 - FlashBAK™ technology
 - General-purpose Serial TAG memory
 - Design security
- **Live Update Technology**
 - TransFR™ technology – update logic configuration while equipment continues to operate
 - Dual Boot with external SPI Flash improves reliability
 - Secure updates with 128 bit AES bitstream encryption
- **Optimized FPGA Architecture**
 - Densities from 5K to 40K 4-input Look-up Tables (LUTs)
 - Up to 885 Kbits sysMEM™ block RAM
 - Up to 83 Kbits distributed RAM
 - Low cost TQFP, PQFP and BGA packaging
- **High Performance sysDSP™ Block**
 - Three to eight blocks with multiply and accumulate
 - 12 to 32 18x18 multipliers
- **Flexible sysIO™ Buffer Supports:**
 - LVCMOS 3.3/2.5/1.8/1.5/1.2; LVTTTL
 - SSTL 18 class I, II; SSTL 3/2 class I, II
 - HSTL15 class I; HSTL18 class I, II
 - PCI
 - LVDS, Bus-LVDS, LVPECL
- **Pre-engineered Source Synchronous Interfaces**
 - DDR / DDR2 up to 200MHz/400Mbps
 - 7:1 LVDS up to 600Mbps
 - Generic up to 750Mbps
- **Up to 4 sysCLOCK™ PLLs**
- **Standby Power Reduced by 33%**
- **System Level Support**
 - SPI/JTAG interface for device programming
 - IEEE Standard 1149.1 Boundary Scan
 - Onboard oscillator for initialization & general use
 - Soft Error Detect (SED) logic
 - 1.2V power supply core voltage

Complete Non-Volatile System-on-Chip



LatticeXP2 Architecture

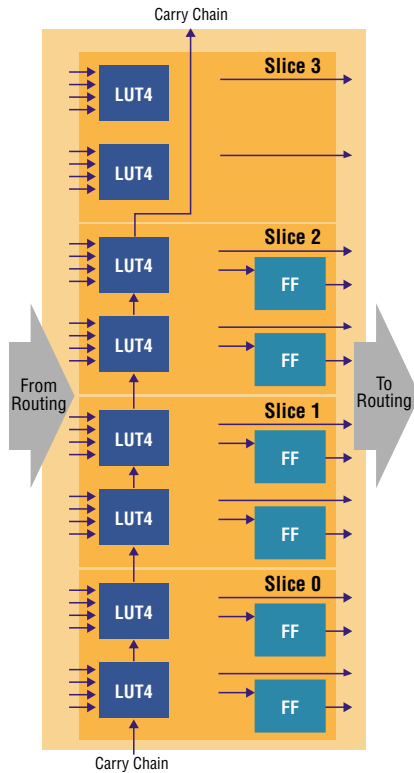
Architecture Overview

LatticeXP2 FPGAs combine on-chip Flash memory with SRAM programmable LUTs and interconnect to provide an optimized low cost architecture that delivers high performance sysMEM embedded RAM blocks, distributed memory, sysCLOCK PLLs, DDR memory interface, sysIO buffers, and more.

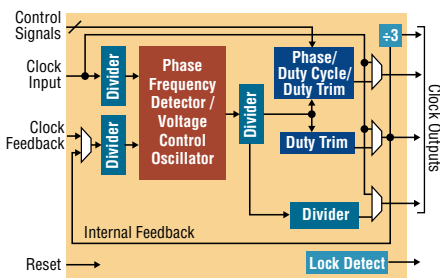


LatticeXP2 FPGAs offer the best of both worlds, with the instant-on, non-volatility of Flash and the reconfigurability of SRAM – all in one chip.

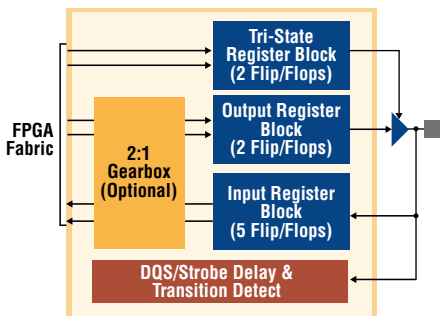
PFU BLOCK DIAGRAM



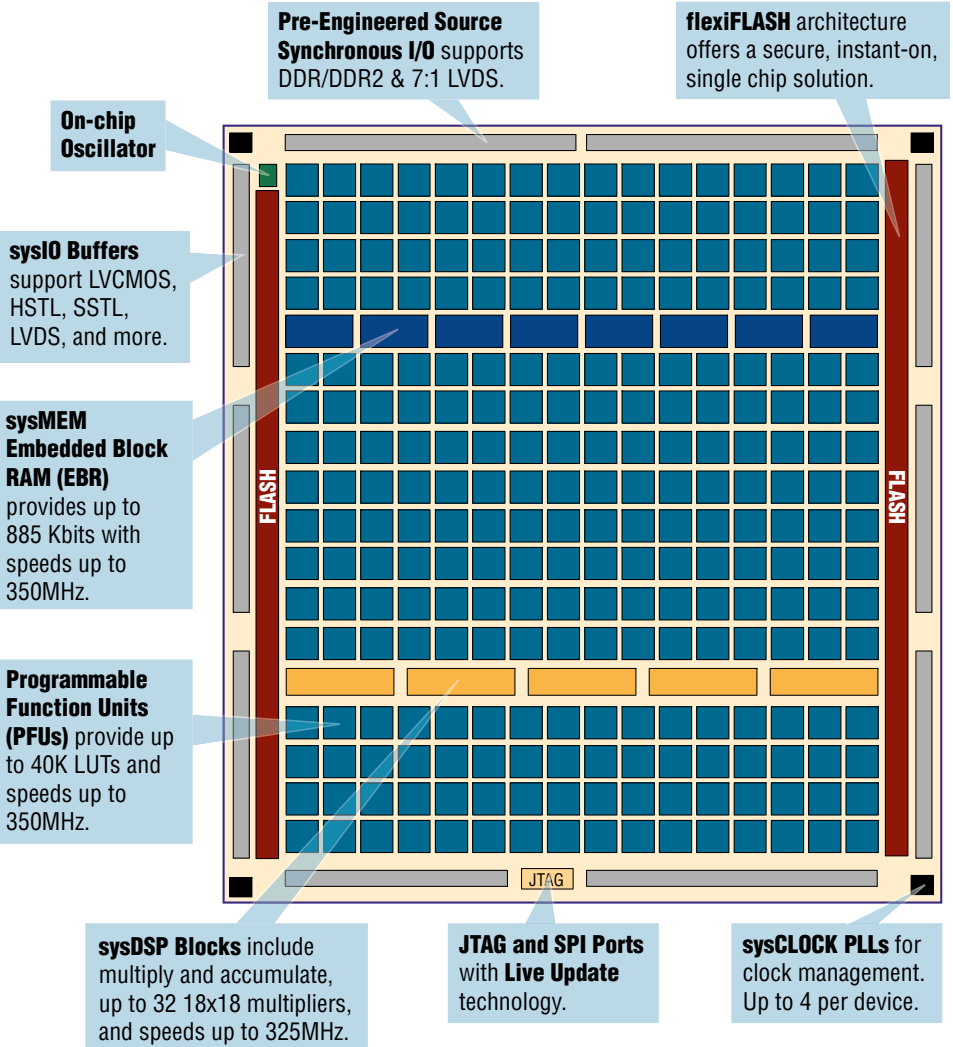
sysCLOCK PLL BLOCK DIAGRAM



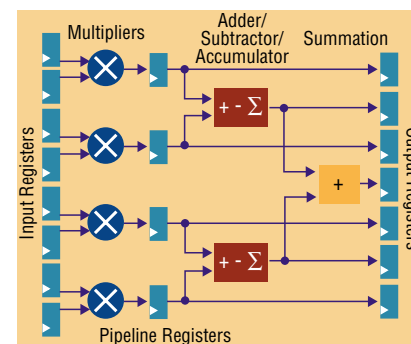
sysIO BLOCK DIAGRAM



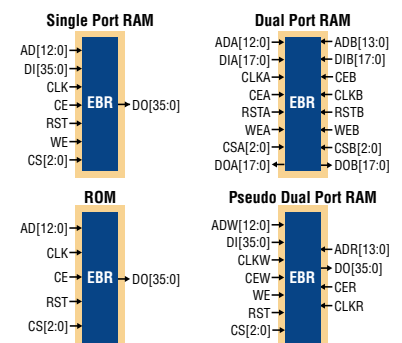
LatticeXP2 Block Diagram



sysDSP BLOCK DIAGRAM

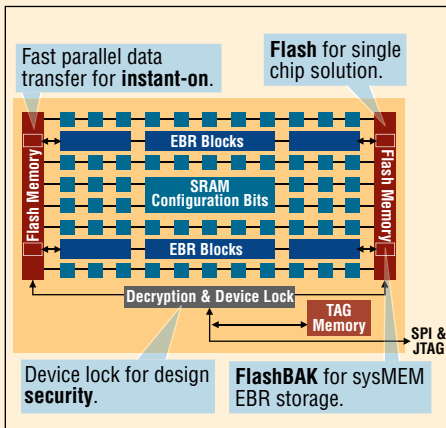


sysMEM EBR PRIMITIVES



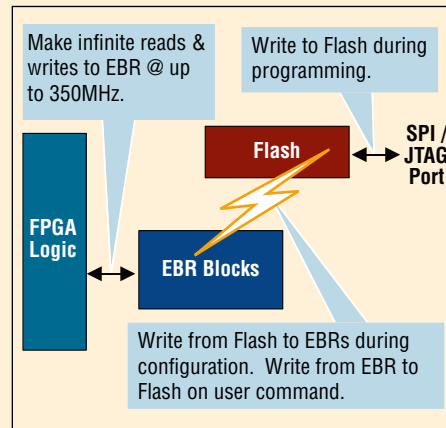
flexiFLASH Overview

flexiFLASH Architecture



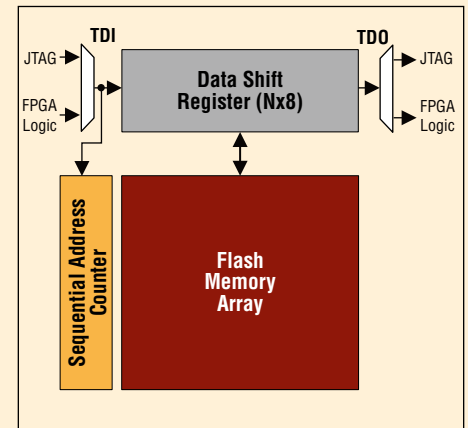
This approach provides a single chip solution, instant-on (1mS), FlashBAK EBR, TAG memory and design security.

FlashBAK Technology



FlashBAK technology allows storage of multiple data types: error codes, data tables, and microprocessor code.

Serial TAG Memory



Use Serial TAG Memory to store items such as Board ID, calibration data, and manufacturing information.

Live Update - Flexible, Reliable and Secure Updates

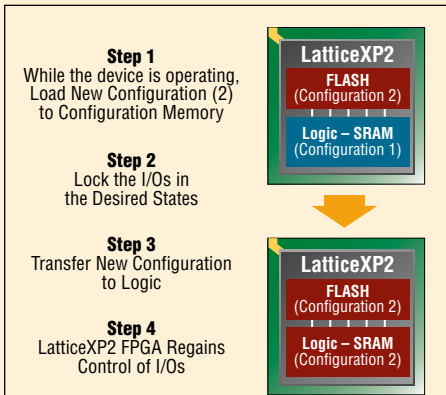
Live Update Technology

Field logic update continues to increase in importance in a wide variety of applications due to the unprecedented flexibility that it provides designers to fix bugs, respond to changing standards, upgrade equipment and add additional services. Lattice's Live Update technology allows logic to be reliably updated in the field without interrupting system operation.

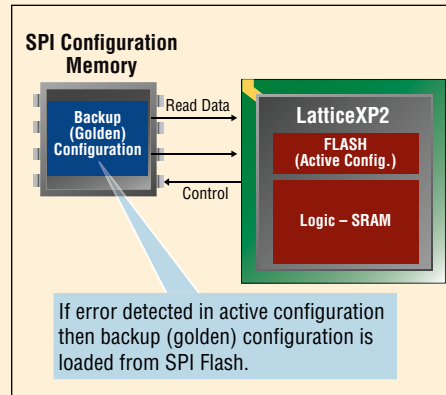


- ✓ Minimize Field Calls
- ✓ Add Services and Features
- ✓ Respond to Changing Standards

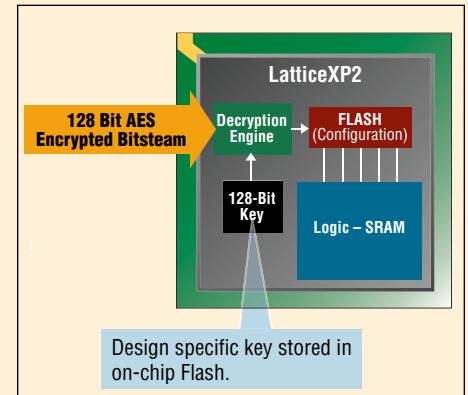
TransFR Technology



Dual Boot for Reliable Updates



128-Bit AES Bitstream Encryption



ispLEVER Design Tools

Lattice's ispLEVER® software is a comprehensive design environment for the LatticeXP2 architectures. The ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floor-planning, simulation, project management, device programming and more



Synthesis and simulation tools from industry leaders Mentor Graphics and Synplicity are included with ispLEVER software.

ispLeverCORE™ Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used functions, including:

- PCI Master/Target and Target 64-bit and 32-bit
- DDR/DDR2 Memory Controllers
- FFT Compiler
- FIR Compiler
- LatticeMico32 Microprocessor
- Gigabit Ethernet MAC
- Viterbi Decoder OFDM
- Correlator
- Interleaver / De-interleaver
- Turbo Encoder / Decoder
- 7:1 LVDS / Color Space



For additional IP cores, go to www.latticesemi.com/ip. Lattice's ispLeverCORE Connections partners also offer a wide range of IP for the LatticeXP2 family.

LatticeXP2 Development Boards

Lattice offers a choice of two development boards to support LatticeXP2 designs. The LatticeXP2 Standard evaluation board and the LatticeXP2 Advanced evaluation board offer platforms to fully evaluate the benefits of the LatticeXP2 devices capabilities in a lab setting.

The LatticeXP2 Advanced Evaluation Board provides a platform to fully evaluate the benefits of the LatticeXP2 family of FPGAs.



The LatticeXP2 Standard Evaluation Board delivers a low-cost option for fast evaluation of LatticeXP2 devices.

Device Selection Guide (Advance Information)

Parameter	LFXP2-5	LFXP2-8	LFXP2-17	LFXP2-30	LFXP2-40
LUTs (K)	5	8	17	29	40
sysMEM EBR RAM Blocks	9	12	15	21	48
Embedded Memory (Kbits)	166	221	276	387	885
Distributed Memory (Kbits)	10	18	35	56	83
sysDSP Blocks	3	4	5	7	8
Number of 18x18 Multipliers	12	16	20	28	32
Number of PLLs	2	2	4	4	4
Vcc Voltage (V)	1.2	1.2	1.2	1.2	1.2
Packages & I/O Combinations					
132-ball csBGA (8 x 8 mm)	86	86			
144-pin TQFP (20 x 20 mm)	100	100			
208-pin PQFP (28 x 28 mm)	146	146	146		
256-ball ftBGA (17 x 17 mm)	172	201	201	201	
484-ball fpBGA (23 x 23 mm)			358	363	363
672-ball fpBGA (27 x 27 mm)				472	540

Applications Support

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