



MWT2 Rel. G

Single Board Computer based on Hyperstone® 32-Bit RISC/DSP CPU



1. Technical Features

- Processor : Hyperstone® E1-L16XSR, 32-Bit RISC/DSP Architecture
- Clock : 118 MHz (Cycle-Time: 8ns to 16KByte internal SRAM)
- SDRAM : 16 MByte, 16-Bit
- Flash : 4 MByte, 16-Bit
- Ethernet : 10/100 MBit/s, Transformer on board,
- 2 x UART : up to 1 MBaud, all RS232 handshake signals
- Power : < 1W at 3.3V
- Connectors : 2 x 20 pin header, 1.27mm, on both sides
- ROHS : compliant
- Temp. Range : industrial (-40 to +85 °C)

2. Compatibility - Replacement Table

The Firmware compatibility with the HyNetOS® Operating System is given in any case. Application code written for any of the older MWT2 modules can easily be ported onto the MWT2-G platform (normally, only a recompilation required).

MWT2-G as replacement for	Connector Pinout, Socket Compatibility	Firmware compatibility	Other differences
MWT2-B	Compatible, but double row connectors on both sides	Needs other Firmware	Different CPU clock More memory
MWT2-C1	100% Compatible	Needs other Firmware	More memory
MWT2-C1PIC	100% Compatible	Needs other Firmware	More memory
MWT2-CIND	100% Compatible	Needs other Firmware	More memory
MWT2-D	100% Compatible	100% Compatible	-
MWT2-E	Compatible, but double row connectors on both sides	Needs other Firmware	Different CPU clock
MWT2-F	Compatible, but double row connectors on both sides	Needs other Firmware	Different CPU clock More memory



3. Pin Description

Name	Pin	Type	Description
VCC	A2, B2	Power	3.3V
GND	A1, A14, B1, C1, C14	Power	Ground
RES#	A3	Open Drain	Hardware reset, driven by internal supervisor
PRES	C3	Output	Peripheral reset, active high
FIO[0..1]	A[4..5]	I/O	Fast general purpose IO, 5V tolerant, max. 20mA, in I2C mode: FIO0 -> SCL, FIO1 -> SDA
FIO3	A7	I/O	Fast general purpose IO, 5V tolerant, max. 20mA, default use: IP-Switch Input
A[0..17]	B[11..28]	Output	Processor bus: address out
D[0..7]	B[3..10]	I/O	Processor bus: data
IORD#	B32	Output	Processor bus: IO read enable
IOWR#	B30	Output	Processor bus: IO write enable
CSIO[1..4]#	B34, B36, B38, B40	Output	Processor bus: IO chip selects
INT[2..4]	B35, B37, B39	Input	Processor bus: Interrupts INT3 is overlapped with WAIT#-Signal
CS2#	B29	Output	Processor bus: MEM chip select
OE#	B31	Output	Processor bus: MEM output enable
WE1#	B33	Output	Processor bus: MEM write enable
TX[0..1]	A13, C13	Output	UART[0..1]: TX
RX[0..1]	A12, C12	Input	UART[0..1]: RX
RTS#[0..1]	A11, C11	Output	UART[0..1]: RTS#
CTS#[0..1]	A10, C10	Input	UART[0..1]: CTS#
DTR#[0..1]	A9, C9	Output	UART[0..1]: DTR#
DSR#[0..1]	A8, C8	Input	UART[0..1]: DSR#
DCD#[0..1]	C7, C5	Input	UART[0..1]: DCD#
RI#[0..1]	C6, C4	Input	UART[0..1]: RI#
TD+	A20	Input	Ethernet: TD+ (connect to RJ45-Pin1)
TD-	A19	Input	Ethernet: TD- (connect to RJ45-Pin2)
RD+	A18	Input	Ethernet: RD+ (connect to RJ45-Pin3)
RD-	A17	Input	Ethernet: RD- (connect to RJ45-Pin6)
LEDA	A16	OpenDrain	Ethernet: Activity-LED
LEDB	A15	OpenDrain	Ethernet: LINK-LED

