Pb free packages

PPAP Submission

Atmel Germany GmbH Part No: all Pb free packages

All hereafter mentioned packages are lead free produced and qualified.

The lead free identification is also part of packing labeling.

Date: January, 28st 2005

Supplier: Atmel Germany GmbH

Adress: Atmel Germany GmbH
Theresienstrasse 2
POB 3535
D-74025 Heilbronn
Tel: (49) 7131 67-0
Fax: (49) 7131 67-2340

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1 Design Records, General Product Information

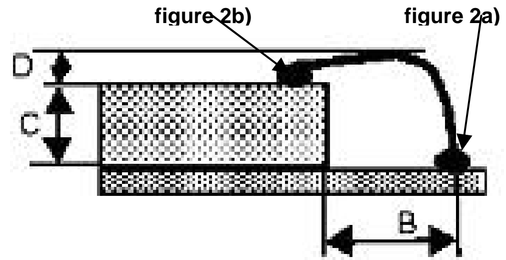
1.1 Package Technology Information

Information about packaging features such as used materials, applied dimensions and so on can be found in respective product PPAPs. Only two minor changes have been applied as described hereafter.

Information to associate concerned package type with respective product will be provided soon through internet (search mask application): http://www.atmel.com

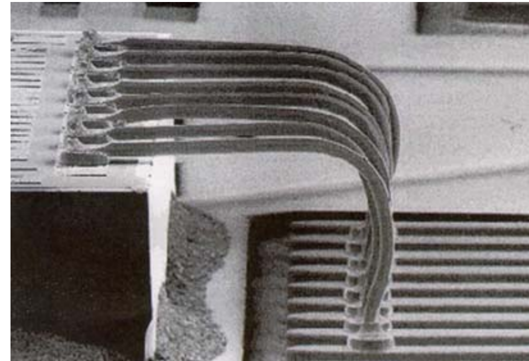
In order to comply with our commitment to satisfy customer's request for steady product quality, an improved bonding method has been applied. This means that all those products bonded with ground bounds get their bonding right now through reverse security bond method instead of former wedge bond method. For better understanding, please refer to detailed drawings as shown on next page.

Further on, some products have been qualified with polyimide layer as final passivation between die surface and the package itself.



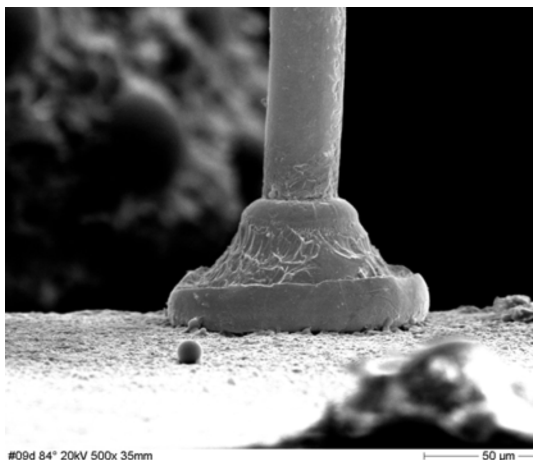
b) drawing of a bond's shape by applying the reverse security bonding method

a) SEM picture of a bond's shape by applying the wedge bonding method

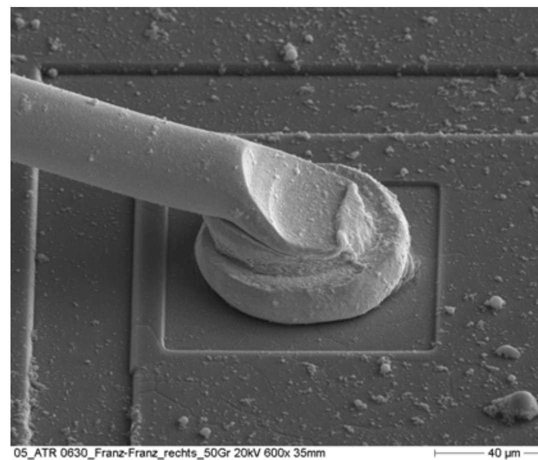


c) SEM picture of a bond's shape by applying the reverse security bonding method

figure 1: comparison between these two different bonding methods



a) ball bond on die pad



b) stitch on ball bond on the die

figure 2: reverse security stitch on ball (RSSB)

2 Engineering Change Documents

See general Pb-free conversion PCN: HC050301.

3 Customer Engineering approval

Customer engineering approval is not applicable as this product is not customer specific.

3.1 Release to Production

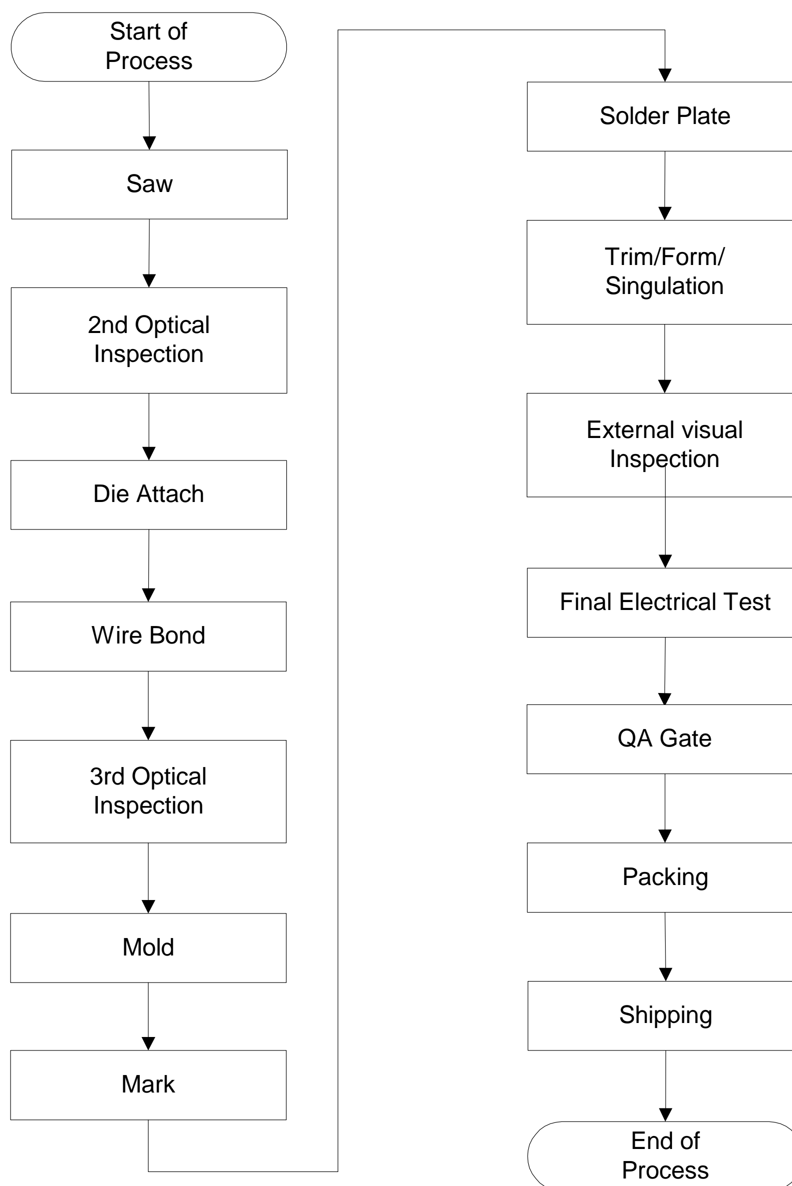
Please refer to the PCN as mentioned in preceding chapter.

4 Design FMEAs

N/A. No change in Design.

5 Process Flow Diagrams

5.1 Package, Packing and Shipping Process Flow Chart



6 Process FMEAs

N/A

7 Dimensional Results

N/A

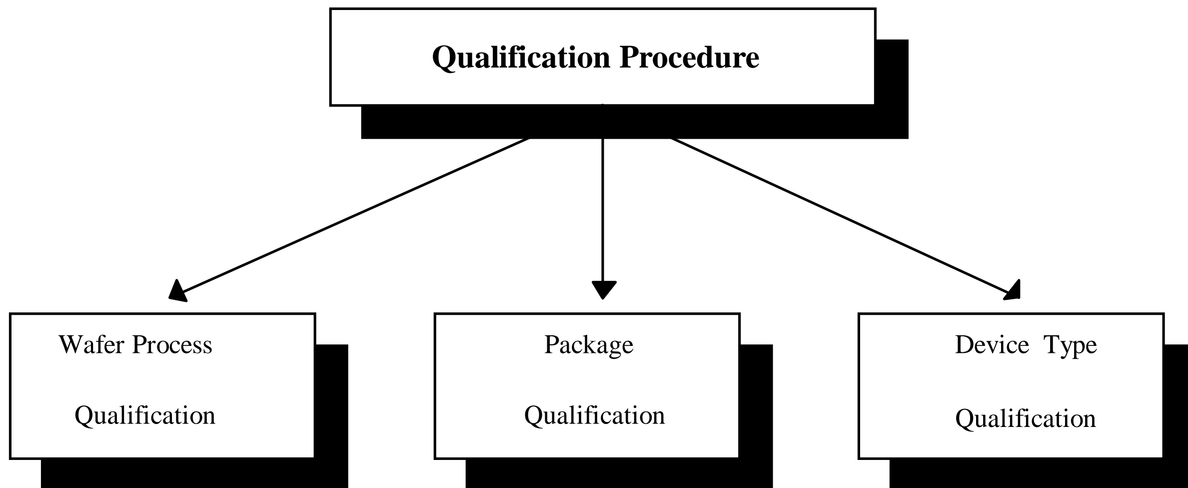
8 Material Performance

8.1 Material Test Results

N/A

8.2 Performance Test Results

8.2.1 Qualification



All product qualifications are split into three distinct areas as shown above. This philosophy is based on AEC-Q100 ‚Stress Test Qualification For Integrated Circuits‘.

The same procedure is also used to qualify a change. Before a product is released for use it must have been manufactured using a qualified process and package. Before a device is released for production processing it must also have successfully completed its required type specific qualification.

The standard tests which are used for this procedure are shown on the

" **Flow Chart for Qualification** "

The data shown for the various qualifications may be from structurally similar parts.

The wafer process may be qualified using the same process but with a similar package.

Similarly the package may be qualified using a similar wafer process.

8.2.2 Change Procedure

All changes are controlled by ECN (Engineering Change Notice). All major changes are notified to those customers using products which are affected by the change with PCN.

A **major change** is defined as a change which affects the electrical and/or mechanical specification as defined in the datasheet or which affects the following parameters as defined in **this PPAP**.

1	Changes in wafer fabrication
1.1	Sequence of fabrication process cycles (as PPAP)
1.2	Fabrication process material
1.3	Doping process (i.e diffusion to ion implantation)
1.4	Passivation material, thickness (including deletion of passivation)
1.5	Metallization system (pattern, material, line width, or thickness)
1.6	Conductor, resistor or dielectric material (for capacitor)
1.7	Wafer fabrication move to another line
1.8	Gate formation process, material, technique (MOS processes only)
1.9	Backside process including metallization and finished thickness
1.10	Ohmic contact formation
1.11	Die size

2	Changes in assembly process
2.1	Type of die attach material
2.2	Wire or ribbon interconnect method
2.3	Wire material and dimensions
2.4	Seal technique (hermetic only)
2.5	Assembly flow (as PPAP)
2.6	Assembly move to another line or sub-contractor
2.7	Scribing or die separation method
2.8	Molding material
2.9	Device marking process

3	Changes in package
3.1	Lead or terminal dimensions (outside datasheet specification)
3.2	Lead or terminal base material
3.3	Lead or terminal plating material, method or specified thickness
3.4	Lid glass seal material (hermetic only)
3.5	Lead glass seal material (hermetic only)
3.6	Lead glass seal diameter (outside specified limits)
3.7	Lead configuration (i.e. J-lead to gullwing)

8.2.3 SO package qualification

a) assembly location: TEMIC Semiconductors Philippines

visual inspection after preconditioning									
package	SO150		SO300					SO175	
preconditioning level	**1**	**3**	**1**	**1**	**3**	**1**	**3**	**1**	**3**
final passivation: w/o polyimide ①	77 - 0	77 - 0	77 - 0	0 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0
final passivation: with polyimide ①	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0

temperature cycling 1000x @ -55°C / +150°C										
passivation	test flow	package								
		SO150		SO300					SO175	
w/o polyimide	room temperature ①	77 - 0	77 - 0	77 - 0	0 - 0	77 - 0	77 - 0	75 - 0	77 - 0	77 - 0
	high temperature ①	77 - 0	77 - 0	77 - 0	0 - 0	77 - 0	0 - 0	0 - 0	77 - 0	77 - 0
with polyimide	room temperature ①	77 - 0	77 - 0	76 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0
	high temperature ①	77 - 0	77 - 0	76 - 0	77 - 0	77 - 0	77 - 0	0 - 0	77 - 0	77 - 0

① the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

(preconditioning) + (humidity 85°C / 85% rH 1000h) + (measurement after stress)										
passivat.	test flow	package								
		SO150		SO300					SO175	
w/o polyimide	preconditioning + subsequent humidity	**1**	**3**	**1**	**1**	**3**	**1**	**3**	**1**	**3**
	room temperature ①	77 - 0	77 - 0	77 - 0	0 - 0	77 - 0	0 - 0	0 - 0	77 - 0	77 - 0
with polyimide	preconditioning + subsequent humidity	**1**	**3**	**1**	**1**	**3**	**1**	**3**	**1**	**3**
	room temperature ①	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0

(preconditioning) + (HAST 130°C / 85% rH 168h) + (measurement after stress)										
passivat.	test flow	package								
		SO150		SO300					SO175	
w/o polyimide	preconditioning + subsequent HAST	1	3	1	1	3	1	3	1	3
	room temperature ①	77 - 0	77 - 0	77 - 0	0 - 0	77 - 0	0 - 0	0 - 0	77 - 0	77 - 0
with polyimide	preconditioning + subsequent HAST	1	3	1	1	3	1	3	1	3
	room temperature ①	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	72 - 0	77 - 0	77 - 0	71 - 0

① the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

b) assembly location: CEI-SAT Thailand

visual inspection after preconditioning						
package	SO150				SO175	
passivation	with polyimide		w/o polyimide		with polyimide	
preconditioning level	**1**	**3**	**1**	**3**	**1**	**3**
visual inspection [1]	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0

temperature cycling 1000x @ -55°C / +150°C						
package	SO150				SO175	
passivation	with polyimide		w/o polyimide		with polyimide	
room temperature [1]	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0
high temperature [1]	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0

(preconditioning) + (humidity 85°C / 85% rH 1000h) + (measurement after stress)						
package	SO150				SO175	
passivation	with polyimide		w/o polyimide		with polyimide	
preconditioning + subsequent humidity	**1**	**3**	**1**	**3**	**1**	**3**
room temperature [1]	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0	77 - 0

(preconditioning) + (HAST 130°C / 85% rH 168h) + (measurement after stress)						
package	SO150				SO175	
passivation	with polyimide		w/o polyimide		with polyimide	
preconditioning + subsequent HAST	**1**	**3**	**1**	**3**	**1**	**3**
room temperature [1]	77 - 0	76 - 0	77 - 0	77 - 0	77 - 0	77 - 0

[1] the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

c) assembly location: ChipPAC Shanghai

following boundary conditions have been applied:

- evaluation performed on SO150 package only
  (final passivation includes a polyimide layer)

visual inspection after preconditioning		
preconditioning level	**1**	**3**
visual inspection ①	77 - 0	77 - 0

temperature cycling 1000x @ -55°C / +150°C		
room temperature	77 - 0	77 - 0
high temperature ①	77 - 0	77 - 0

(preconditioning) + (humidity 85°C / 85% rH 1000h) + (measurement after stress)		
preconditioning + subsequent humidity	**1**	**3**
room temperature ①	77 - 0	77 - 0

(preconditioning) + (HAST 130°C / 85% rH 168h) + (measurement after stress)		
preconditioning + subsequent HAST	**1**	**3**
room temperature ①	77 - 0	77 - 0

① the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

8.2.4 QFN package qualification

Unique assembly location to qualify QFN packages was ChipPAC Malaysia.

a) QFN4x4 / 16 pins

preconditioning L2 + temperature cycling 1000x @ -55°C / +150°C + measurement after stress	
room temperature ①	76 - 0

preconditioning L3 + temperature cycling 1000x @ -55°C / +150°C + measurement after stress	
room temperature ①	76 - 0

① the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

b) QFN5x5 / 28 pins

preconditioning L2 + measurement after stress + visual inspection after stress	
room temperature ①	22 - 0

preconditioning L3 + measurement after stress + visual inspection after stress	
room temperature ①	22 - 0

preconditioning L3 + temperature cycling 1000x @ -55°C / +150°C + measurement after stress				
sample amount	lot 1	lot 2	lot 3	lot 4
room temperature ①	76 - 0	77 - 0	77 - 0	76 - 0
visual inspection ①	22 - 0	22 - 0	0 - 0	0 - 0

① the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

c) QFN7x7 / 44 pins

preconditioning L1 + temperature cycling 1000x @ -55°C / +150°C		
sample amount	lot 1	lot 2
visual inspection before stress ①	30 - 0	30 - 0
measurement at room temperature after stress ①	30 - 0	30 - 0

preconditioning L2 + temperature cycling 1000x @ -55°C / +150°C		
sample amount	lot 1	lot 2
visual inspection before stress ①	30 - 0	30 - 0
measurement at room temperature after stress ①	30 - 0	30 - 0

preconditioning L3 + temperature cycling 1000x @ -55°C / +150°C		
sample amount	lot 1	lot 2
visual inspection before stress ①	30 - 0	30 - 0
measurement at room temperature after stress ①	30 - 0	30 - 0

① the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

d) QFN7x7 / 48 pins

preconditioning L2 + measurement after stress + visual inspection after stress	
room temperature ①	22 - 0

preconditioning L2 + temperature cycling 1000x @ -55°C / +150°C + measurement after stress	
room temperature ①	77 - 0

preconditioning L2 + HAST 130°C / 85% rH 168h + measurement after stress	
room temperature ①	77 - 0

preconditioning L3 + visual inspection + measurement after stress						
sample amount	lot 1	lot 2	lot 3	lot 4	lot 5	lot 6
visual inspection ①	22 - 0	22 - 0	22 - 0	22 - 0	22 - 0	22 - 0
room temperature ①	22 - 0	22 - 0	22 - 0	22 - 0	22 - 0	22 - 0

preconditioning L3 + temperature cycling 500x @ -55°C / +150°C + measurement after stress					
sample amount	lot 1	lot 2	lot 3	lot 4	lot 5
room temperature ①	72 - 0	79 - 0	80 - 0	80 - 0	80 - 0
high temperature ①	72 - 0	79 - 0	80 - 0	80 - 0	80 - 0

preconditioning L3 + HAST 130°C / 85% rH 168h + measurement after stress			
sample amount	lot 1	lot 2	lot 3
room temperature ①	80 - 0	79 - 0	74 - 0

preconditioning L3 + humidity 85°C / 85% rH biased IC 1000h+ measurement after stress			
sample amount	lot 1	lot 2	lot 3
room temperature ①	75 - 0	79 - 0	79 - 0
high temperature ①	75 - 0	79 - 0	79 - 0

① the figures always refer to the tested samples vs. failed samples as a possible result of the test: **tested pcs. - failed pcs.**

8.3 Outgoing Quality and FIT Rate

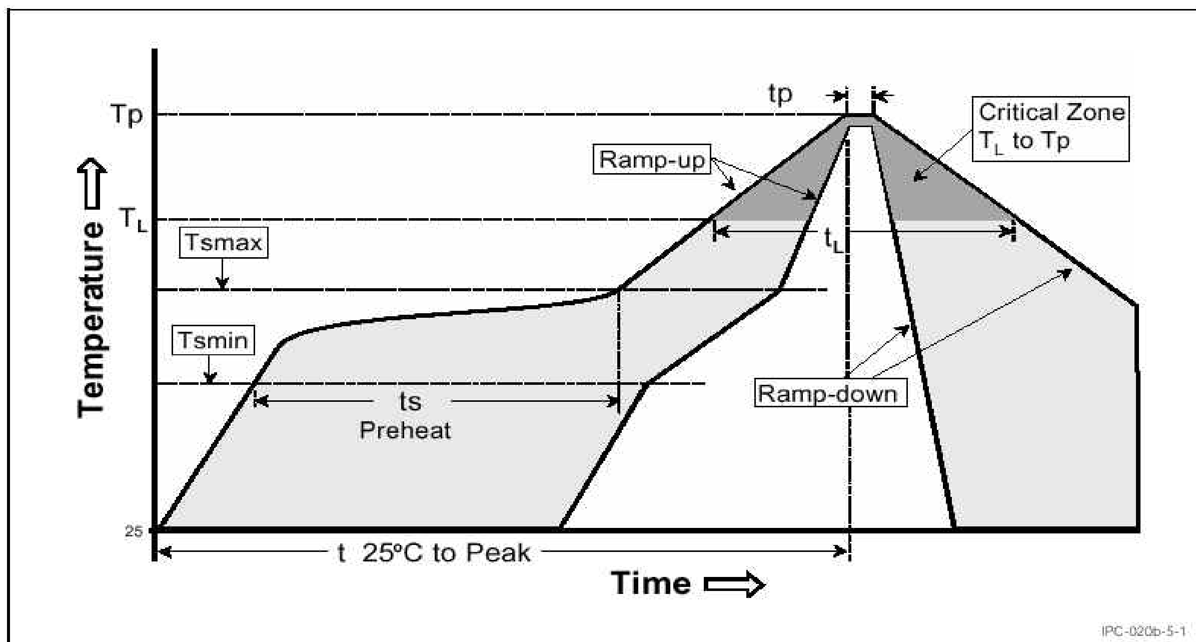
Information's can be retrieved from:

http://www.atmel.com/quality/quality_reliability.asp

8.4 User Information

Recommended Infrared/Convection Solder Reflow Profile (SMD and Flip Chip packages) according JEDEC J-STD-020C

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Tsmax to T_L -Ramp-up Rate		 3°C/second max.
Time maintened above: -Temperature (T_L) -Time (t_L)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature (T_P)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (t_P)	10-30 sec.	20-40 sec.
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.
MSL	Information to associate the right MSL with respective package type will be provided soon through internet (search mask application): http://www.atmel.com	



9 Initial Process Study

N/A

10 Measurement System Analysis Studies

N/A

11 Qualified Laboratory Information

Our laboratories meets all requirements of ISO/TS16949.

12 Control Plan

Company confidential document.

13 PSW (Part Submission Warrant)

Part Name **all products from ATMEL RFA** Part Number

Safety and / or Government Regulation ☐ Yes ☒ No Engineering Drawing Change Level Dated

Additional Engineering Changes --- Dated

Shown on Drawing No. --- Purchase Order No. Weight(kg) **< 0.005**

Checking Aid Number --- Engineering Change Level --- Dated

SUPPLIER MANUFACTURING INFORMATION

Atmel Germany GmbH
Supplier Name
Theresienstr. 2
Street Address
74072 Heilbronn Germany
Zip City State

SUBMISSION INFORMATION

☐ Dimensional ☒ Materials/Functional ☐ Appearance

Customer Name/Division

Buyer/Buyer Code

Application

Note: Does this part contain any restricted or reportable substances ☐ Yes ☒ No
Are plastic parts identified with appropriate ISO markings ☐ Yes ☒ No

REASON FOR SUBMISSION

- ☒ Initial submission
- ☐ Engineering Change(s)
- ☐ Tooling: Transfer, Replacement, Refurbishment, or additional
- ☐ Correction of Discrepancy
- ☐ Tooling Inactive > than 1 year
- ☐ Change to Optional Construction or Material
- ☐ Sub-Supplier or Material Source Change
- ☐ Change in Part Processing
- ☐ Parts produced at Additional Location
- ☐ Other – please specify

REQUESTED SUBMISSION LEVEL (Check one)

- ☐ Level 1 - Warrant only (and for designated appearance items, an Appearance Approval Report) submitted to customer.
- ☐ Level 2 - Warrant with product samples and limited supporting data submitted to customer.
- ☒ Level 3 Warrant with product samples and complete supporting data submitted to customer.
- ☐ Level 4 - Warrant and other requirements as defined by the customer.
- ☐ Level 5 Warrant with product samples and complete supporting data reviewed at supplier's manufacturing location.

SUBMISSION RESULTS

The results for ☐ dimensional measurements ☒ material and functional tests ☐ appearance criteria ☐ statistical process package
These results meet all drawing and specification requirements: ☒ YES ☐ NO (If "NO" – explanation required)
Mold / Cavity / Production Process

DECLARATION

I hereby affirm that the samples represented by this warrant are representative of our parts and have been made to the applicable Production Part Approval Process Manual 3rd Edition Requirements. I further warrant these samples were produced at the production rate of ________ / 8 hours. I have noted any deviations from this declaration below.

EXPLANATION/COMMENTS:

Print Name **Dietmar Sigmann** Title **QM Products** Phone No. ***49 (0) 7131-67-2803 / fax: 2499**

Supplier Authorized Signature i. A. [signature] i. A. Junesch Date **2005-01-31**

FOR CUSTOMER USE ONLY (IF APPLICABLE)

Part Disposition ☐ Approved ☐ Rejected ☐ Other

Part Functional Approval ☐ Approved ☐ Rejected

Customer Name Customer Signature Date

July 1999 **CFG-1001** The original copy of this document shall remain at the suppliers location while the part is active. Optional customer tracking number: #

14 Appearance Approval Report

N/A

15 Bulk Material Requirements Checklist

N/A

16 Sample Product

Samples can be ordered upon request.

17 Checking Aids

N/A

18 Records of Compliance

N/A

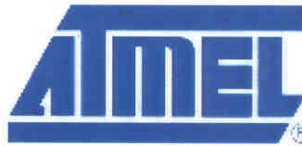
19 Addendum

19.1 Certifications

ZERTIFIKAT ◆ CERTIFICATE ◆ 認証書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

CERTIFICATE

The Certification Body
of TÜV Management Service GmbH
certifies that



Germany GmbH
Theresienstr. 2 • D-74072 Heilbronn

has established and applies a Quality Management System for

Design, Production and Sale of Semiconductor Devices including the design locations Lise-Meitner-Strasse 15, D-89081 Ulm Königsbrücker Strasse 61, D-01169 Dresden

The audit was conducted in accordance with the "Rules for the registration scheme for ISO/TS 16949: 2002, 1st Edition."
An audit was performed, Report No. **70006031**
Proof has been furnished that the requirements according to

ISO/TS 16949: 2002
and the Customer-Specific requirements as listed in enclosure are fulfilled.

The certificate is valid from **2004-02-26** until **2007-02-25**

Certificate Registration No.: **12 111 21628 TMS**

IATF Certificate No.: **0024577**

Mannheim, 2004-02-26

Certification Body
of TÜV Management Service GmbH
Unternehmensgruppe TÜV Süddeutschland
Ridlerstraße 65
D-80339 München

2-IAO-QMC-01004

ZERTIFIKAT ◆ CERTIFICATE ◆ 認証書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

Enclosure 1 of Certificate No.: 12 111 21628 TMS
IATF Certificate No.: 0024577

of 2004-02-26

Germany GmbH
Theresienstr. 2 • D-74072 Heilbronn

Following additional Customer-Specific Requirements were audited and are fulfilled:

Customer Specific Requirements (ISO/TS-16949)
Semiconductor Commodity

Mannheim, 2004-02-26

Certification Body
of TÜV Management Service GmbH
Unternehmensgruppe TÜV Süddeutschland
Ridlerstraße 65
D-80339 München

2-IAO-QMC-01004

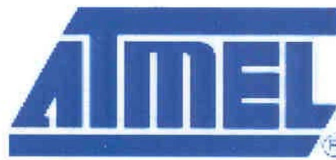
Page 1 of 1

ZERTIFIKAT ◆ CERTIFICATE ◆ 認証書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

CERTIFICATE

The Certification Body
of TÜV Management Service GmbH

certifies that



Germany GmbH
Theresienstr. 2 • D-74072 Heilbronn

has established and applies
a Quality Management System for

Design, Production and Sale of Semiconductor
Devices including the design locations
Lise-Meitner-Strasse 15, D-89081 Ulm
Königsbrücker Strasse 61, D-01169 Dresden

An audit was performed, Report No. **70006031**

Proof has been furnished that the requirements
according to

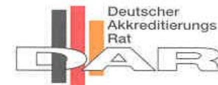
ISO 9001: 2000

are fulfilled. The certificate is valid until **2007-02-25**

Certificate Registration No. **12 100 21628 TMS**

Mannheim, 2004-02-26

Certification Body
of TÜV Management Service GmbH
Unternehmensgruppe TÜV Süddeutschland
Ridlerstraße 65
D-80339 München



TGA-ZM-07-92

19.2 Environmental Information (Brochure)

http://www.atmel.com/quality/quality_env.asp

19.3 Reference

The following data references are available for this device:

1. Information to associate concerned package type with respective product will be provided soon through internet (search mask application): http://www.atmel.com

2. Product data sheets can be retrieved from: http://www.atmel.com

Reference Address

All enquiries relating to this document should be addressed to the following:

Atmel Germany GmbH
Theresienstrasse 2
POB 3535
D-74025 Heilbronn
Tel: (49) 7131 67-0
Fax: (49) 7131 67-2340

Atmel

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19.4 Revision history

Issue	Modification Notice	Refer to page
January 2005	Initial Version	