User's Manual

MSC CXC-US15W

MSC COM Express™ Compact Module

– PRELIMINARY –

Rev.0.5

16.09.2011

Preface

Copyright Notice

Important Information

This documentation is intended for qualified audience only. The product described herein is not an end user product. It was developed and manufactured for further processing by trained personnel.

Disclaimer

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EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Trademarks

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Certification

MSC Vertriebs GmbH is certified according to DIN EN ISO 9001:2000 standards.

Life-Cycle-Management

MSC products are developed and manufactured according to high quality standards. Our life-cycle-management assures long term availability through permanent product maintenance. Technically necessary changes and improvements are introduced if applicable. A product- change-notification and end-of-life management process assures early information of our customers.

Product Support

MSC engineers and technicians are committed to provide support to our customers whenever needed.
Before contacting Technical Support of MSC Vertriebs GmbH, please consult the respective pages on our web site at www.msc-ge.com/support-boards for the latest documentation, drivers and software downloads.
If the information provided there does not solve your problem, please contact our Technical Support:

Email: support.boards@msc-ge.com
Phone: +49 8165 906-200

Contents

1 General Information

1.1 Revision History

Rev.	Date	Description
0.1	2009-10-21	Initial version (wdu/jsid)
0.2	2010-03-10	Added Bios chapter / PCI IRQ Routing table
0.3	2010-05-20	Updated Bios chapter according to X1.00e
0.4	2010-08-04	Minor corrections
0.5	2011-09-16	Setup ACPI corrections

1.2 Reference Documents

[1] COM Express Module Base Specification
COM Express Revision 1.0
Last update: July 10th, 2005

[2] PCI Local Bus Specification Rev. 2.1
PCI21.PDF
Last update: June 1st, 1995
http://www.pcisig.com

[3] ATA/ATAPI-6 Specification
d1410r3b.pdf
http://www.t13.org/

[4] Serial ATA Specification
Serial ATA 1.0 gold.pdf
Last update: August 29th, 2002 Rev.1.0
http://www.sata-io.org/

[5] IEEE Std. 802.3-2002
802.3-2002.pdf
http://www.ieee.org

[6] Universal Bus Specification
usb_20.pdf
Last update: April 27th, 2000
http://www.usb.org

1.3 Introduction

COM Express™, an open specification of the PICMG (PCI Industrial Computer Manufacturer Group), is a module concept to bring PCI Express and other latest technologies like SATA, USB 2.0 and LVDS on a COM (Computer On Module).

A COM Express™ module is plugged onto an application-specific base board similar to the ETX concept, but offers more options and a growth path to future CPU technologies. Utilizing different sizes, COM Express™ can be used for highly embedded solutions up to high performance platforms.

The design of the MSC CXC-US15W module supports the Atom CPU technology.

For evaluation and design-in of the COM Express™ modules we provide evaluation baseboards and develop motherboards providing the interface infrastructure for the COM Express™ module offering PC type connectors for external access.

Up to 440 pins of connectivity are available between COM Express™ modules and the Carrier Board. Legacy buses such as PCI, parallel ATA, LPC, HDA are supported as well as new high speed serial interconnects such as PCI Express, Serial ATA and Gigabit Ethernet.

To enhance interoperability between COM Express™ modules and Carrier Boards, five common signalling configurations (pin-out types) have been defined to ease system integration.

2 Technical Description

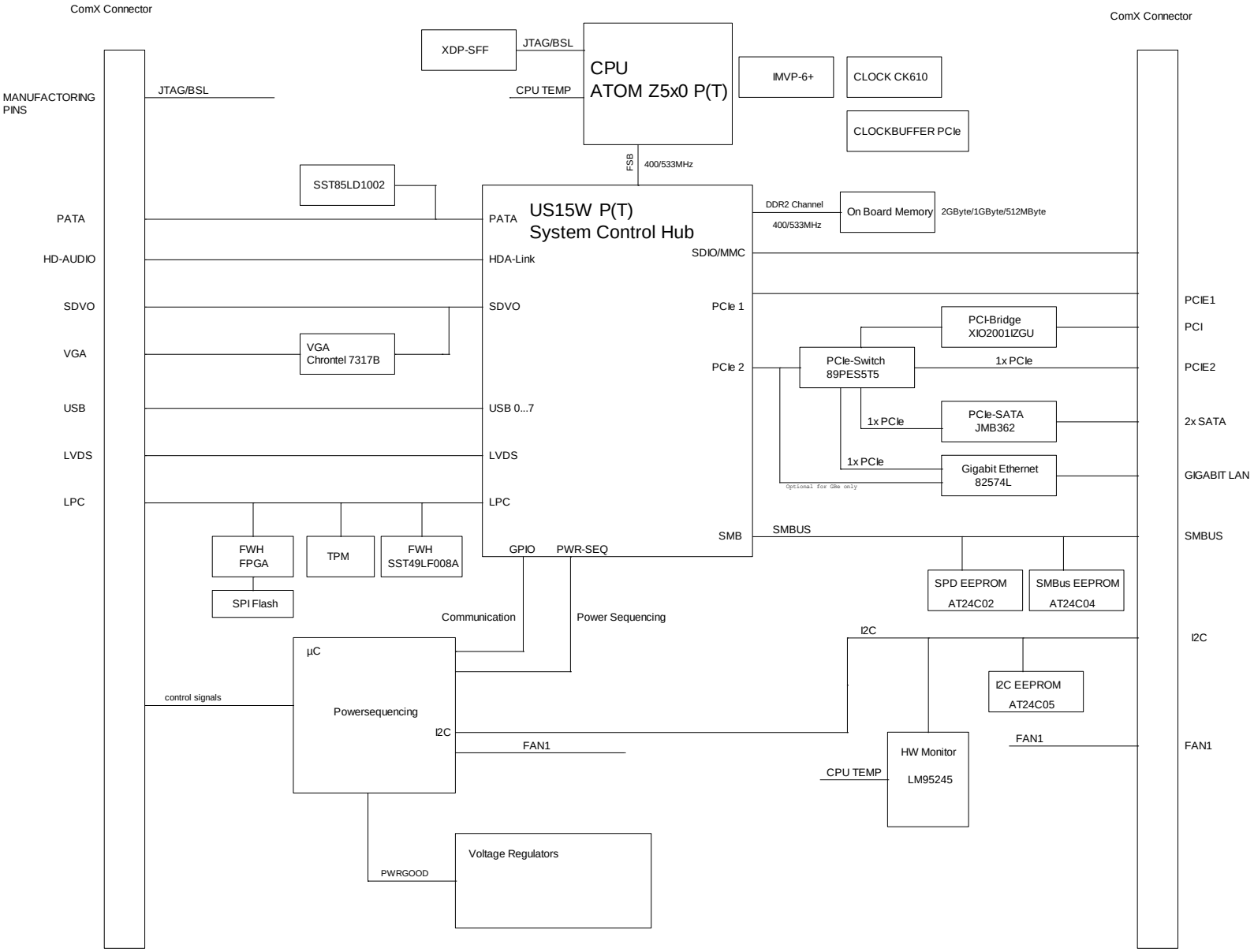
2.1 Key Features

The MSC US15W COM Express Extended module is designed as a type 2 module.

Key features include

- Module size: 155 mm x 110 mm
- 45 mm ‘z’ height with cooling solution with fan (see 2.7 , 5 mm stack option)
- Dual 220 pin connector (440 pins)
- Max 2GB DDR2 400/533 MHz Memory.
- 8 USB 2.0 ports.
- 2 Serial ATA (SATA) ports.
- 2 external PCI Express x1 lanes
- ExpressCard support.
- Single 24-bit LVDS channel
- Single SDVO Channel.
- Analog VGA (optional to SDVO).
- High definition digital audio interface (external CODEC)
- Single Gigabit Ethernet (external magnetic)
- LPC interface
- BIOS
- 8 GPIO pins
- +12V primary power supply input
- +5V standby and 3.3V RTC power supply inputs
- 32 bit PCI interface
- IDE port (to support legacy ATA devices such as CD-ROM drives and Compact Flash storage cards)
- TPM module (option, TPM 1.2, SLB9635)

2.2 Block diagram



2.3 Com Express Implementation

COM Express™ required and optional features of pin-out type 2 are summarized in the following table. The features identified as minimum (Min.) **shall** be implemented by all modules. Features identified up to maximum (Max) **may** be additionally implemented by a module.

The column MSC US15W shows the implemented features of the MSC module:

Function	Type 2	MSC US15W	Note
	Min / Max		
System I/O			
PCI Express Graphics (PEG)	0 / 1	0	
PCI Express Lanes 0 - 5	2 / 6	2 x1	
PCI Express Lanes 16-31 (same as PEG pins)	0 / 16	0	
SDVO Channels	0 / 2	1	Optional to VGA
LVDS Channels	0 / 2	1	1x Single channel, 24 bit
VGA Port	0 / 1	1	Optional to SDVO
TV-Out	0 / 1	0	
PATA Port	1 / 1	1	
SATA Ports	2 / 4	2	
Digital Audio Interface	0 / 1	1	High Definition Audio
USB 2.0 Ports	4 / 8	8	
LAN 0 (10/100Base-T min)	1 / 1	1	82574 GigaBit LAN
PCI Bus - 32 Bit	1 / 1	1	
Express Card Support	1 / 2	2	
LPC Bus	1 / 1	1	
System Management			
General Purpose Inputs	4 / 4	4	
General Purpose Outputs	4 / 4	4	
SMBus	1 / 1	1	
I2C	1 / 1	1	
Watch Dog Timer	0 / 1	1	
Speaker Out	1 / 1	1	
External BIOS ROM support	0 / 1	1	
Reset Functions	1 / 1	1	
Power Management			
Thermal Protection	0 / 1	1	
Battery Low Alarm	0 / 1	1	
Suspend	0 / 1	1	
Wake	0 / 2	2	WOL, PCI Wake
Power Button Support	1 / 1	1	
Power Good	1 / 1	1	
Security			
TPM	0 / 0	1	TPM 1.2 module

2.4 Functional Units

CPUs	Intel® Atom™ Z530P (1.6 GHz, FSB 400/533MHz, 441 FCBGA) Intel® Atom™ Z520PT (1.33 GHz, FSB 400/533MHz, 441 FCBGA) Intel® Atom™ Z510PT (1.1 GHz, FSB 400/533MHz, 441 FCBGA)
Chipset	Intel® US15W SCH (System Controller Hub)
Memory	Single channel memory down configuration. Max 2GB DDR2 Memory.
SATA	2 x SATA channels up to 300MB/s each
EIDE	1 x Enhanced IDE port ATA/UDMA100
USB	8 x USB 2.0
COM Express™	Type 2 interface, fully compliant
PCI Express™	2 x PCIe x1
PCI	32 Bit standard interface
LPC	Low Pincount Bus for heritage interfaces
Graphics Controller	Mobile Intel® Graphics Media Accelerator 500 (integrated in Intel® US15W chipset)
Video Memory	UMA
LCD Interface	Single LVDS 24Bit channel. max. resolution 1600 x 1200
SDVO Interface	1 SDVO port. Optional to VGA.
CRT Interface	QXGA maximum resolution 2048 x 1536
Ethernet	Integrated 10/100/1000 GbE MAC (US15W) with Intel® 82574 Gigabit Platform LAN Connect
Sound Interface	High Definition Audio interface
Watchdog Timer	Integrated in microcontroller Creates system reset (programmable, 1s … 255h)
TPM (option)	Optional TPM module, TPM 1.2, SLB9635
Fan Supply	3-pin header for 12V fan (GND, +12V, TACHO)
Real Time Clock	Integrated RTC in US15W
Battery	External 3V battery
System Monitoring	Voltage , Temperature , Fan ▪ Core voltage ▪ 3.3V ▪ 5V_SBY (from external) ▪ 12V (from external) ▪ CPU thermal diode ▪ Memory temperature sensor ▪ Board temperature sensor ▪ Fan Speed

2.5 Power Supply

+12V primary power supply input

+5V standby

Option, is not required for module operation.
If not present, there is no support for power management states and ATX power supply functionality.

3.3V RTC power supply

Option, is not required for module operation.

BIOS SETUP data is stored in a non volatile backup memory device (EEPROM), therefore configuration data will not get lost during power off (except for time and date information)

Voltage	Input range	Current
+12V	+11.4V - 12.6 V	See next table
+5V Standby	+4.75V - 5.25 V	0,08A
+3V RTC power supply	+2.0V - 3.3V	max. 6µA

2.6 Power dissipation

DOS Prompt, 2x 512MB DDR2 SO-DIMM, T_a= 25°C

Module (CPU)	Voltage	Watt (typ.)
Intel® Atom™ Z530P (Low Power, 1.6 GHz)	+12V	
Intel® Atom™ Z520PT (Low Power, 1.33 GHz)	+12V	
Intel® Atom™ Z510PT (Low Power, 1.1 GHz)	+12V	

INTEL Thermal Analysis Tool (TAT! 2.05), 80% workload, all cores active, T_a= 25°C

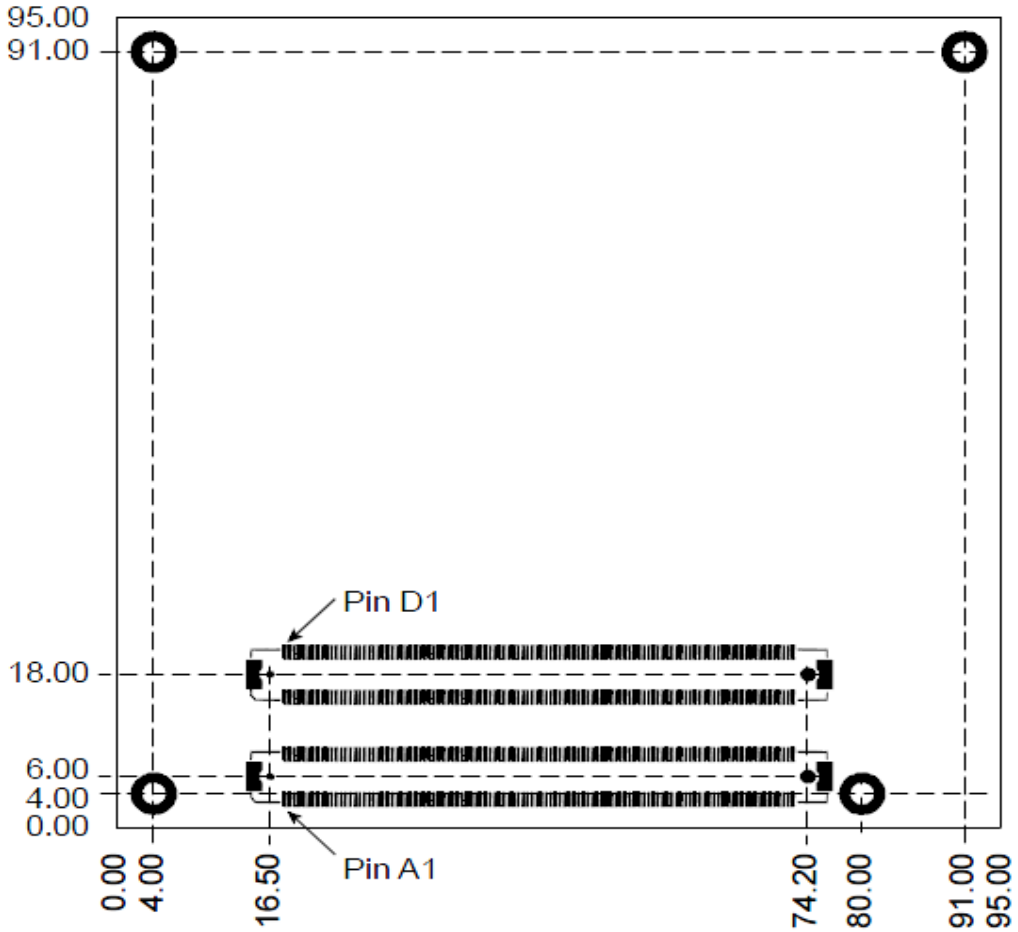
Module (CPU)	Voltage	Watt (typ.)
Intel® Atom™ Z530P (Low Power, 1.6 GHz)	+12V	
Intel® Atom™ Z520PT (Low Power, 1.33 GHz)	+12V	
Intel® Atom™ Z510PT (Low Power, 1.1 GHz)	+12V	

Max, T_a= 25°C

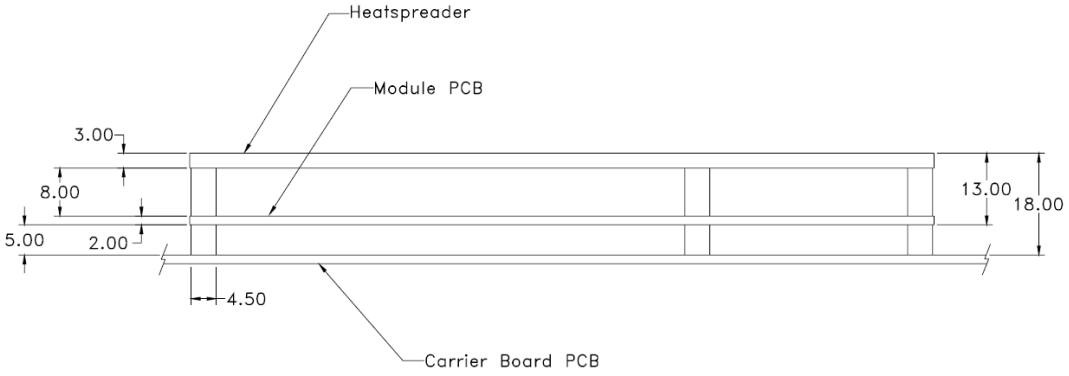
Module (CPU)	Voltage	Watt (typ.)
Intel® Atom™ Z530P (Low Power, 1.6 GHz)	+12V	
Intel® Atom™ Z520PT (Low Power, 1.33 GHz)	+12V	
Intel® Atom™ Z510PT (Low Power, 1.1 GHz)	+12V	

2.7 Mechanical Dimensions

Compact Module



There are two height options defined in the COM Express specification: 5mm and 8mm. The height option is defined by the connectors on the baseboard.



MSC CXC-US15WTop view

MSC CXC-US15WBottom view

2.8 Cooling solution

A special cooling solution is available for the CXC US15W module.

2.9 Signal description

The following tables define the signals on COM Express ™ interface connectors.
Pins are marked in the following tables with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different. For example, the PCI group is defined as having a 3.3V power rail, meaning that the output signals will only be driven to 3.3V, but the pins are tolerant of 5V signals.
The column “Suspend state” indicates whether the pin is active or inactive during suspend states (S3, S4, S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.
Signal names with # at the end are asserted active when their voltage level is ***low***.
Signal names without # at the end are asserted active when their voltage level is ***high***.

Pin Types

I	Input to the module
O	Output from the module
I/O	Bi-directional input / output signal
OD	Open drain output

Buffer Types

CMOS	Logic input or output. Input thresholds and output levels shall be 80% of supply rail for high side and 20% of the relevant supply rail for low side.
PCIE	PCI Express compatible differential signal. Please refer to the PCI Express Specification for details. PCIE transmit pins (module outputs) shall be AC coupled on the module. PCIE receive pins (module inputs) shall be DC coupled on the COM Express ™ module and shall be assumed to be AC coupled off-module, close to the signal source. If the target PCI Express device resides on the Carrier Board, the PCIE receive lanes on the module (= PCIE device transmit lanes from carrier board) shall be AC coupled near the device on the carrier board. If the carrier board implements a PCIE slot, then these signals shall be AC coupled on the add-in card, not on the Carrier Board.
PCI	PCI 2.3 compatible signal. Please refer to the PCI Rev. 2.3 Specification for details.
SATA	SATA compatible differential signal. Please refer to the SATA Specification for details. All COM Express™ SATA signals shall be AC coupled on the module.
LVDS	Low Voltage Differential Signalling – 330mV nominal; 450mV maximum differential signal.
USB	USB 2.0 compatible differential signal. Please refer to the USB 2.0 Specification for details.
REF	Reference voltage output. May be sourced from a module power plane.
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities to the Carrier Board.
Analog	Inputs and Outputs used for Ethernet, VGA and TV OUT are analog signals.
Power	Inputs used for power delivery to the module electronics.

PU/PD

The PU/PD column shows whether a signal is pulled high or low on the module.

PU[value] Pull-up resistor on COM Express module. *Value* shows the nominal resistor value. If not other mentioned the resistor is pulled to the voltage rail defined in the Rail column.

PD[*value*] Pull-down resistor on COM Express module. *Value* shows the nominal resistor value.

iPU[*value*] Chipset internal pull-up resistor. *Value* shows the nominal resistor value. If not other mentioned the resistor is pulled to the voltage rail defined in the Rail column. Typically the value of a chipset internal pull-up resistor may vary within a wide range.

iPD[*value*] Chipset internal pull-down resistor. *Value* shows the nominal resistor value. Typically the value of a chipset internal pull-down resistor may vary within a wide range.

2.9.1 High definition audio

Signal Name	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
HDA_RST#	O CMOS	3.3V	active		**Intel® High Definition Audio Reset:** Master hardware reset to external codec(s).	US15W
HDA_SYNC	O CMOS	3.3V	not active	iPD 20k	**Intel High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number. HDA_SYNC is sampled at the rising edge of PWROK as a functional strap. ***Refer to chapter 2.9.5 PCI Express Lanes for details.***	US15W
HDA_BITCLK	I/O CMOS	3.3V	not active	iPD 20k	**Intel High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel High Definition Audio controller.	US15W
HDA_SDOUT	O CMOS	3.3V	not active	iPD 20k	**Intel High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. HDA_SDOUT is sampled at the rising edge of PWROK as a functional strap. Refer to chapter ***2.9.5 PCI Express Lanes 0 – 5*** for details.	US15W
HDA_SDIN[0:2]	I CMOS	3.3V	active	iPD 20k	**Intel High Definition Audio Serial Data In [3:0]**: Serial TDM data inputs from the codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel® High Definition Audio.	US15W

2.9.2 Gigabit ethernet

Signal Name	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	I/O Analog	3.3V	active[1]		**Gigabit Ethernet Controller 0**: Media Dependent Interface Differential Pairs 0, 1, 2, 3. The MDI can operate in 1000, 100 and 10 Mbit/sec modes.	82574L
GBE0_ACT#	OD CMOS 20mA sink	3.3V	active[1]		**Gigabit Ethernet Controller 0:** Activity indicator, active low.	82574L
GBE0_LINK#	OD CMOS 20mA sink	3.3V	active[1]		**Gigabit Ethernet Controller 0:** Link indicator, active low.	82574L
GBE0_LINK100#	OD CMOS 20mA sink	3.3V	active[1]		**Gigabit Ethernet Controller 0:** 100 Mbit/sec link indicator, active low.	82574L
GBE0_LINK1000#	OD CMOS 20mA sink	3.3V	active[1]		**Gigabit Ethernet Controller 0:** 1000 Mbit/sec link indicator, active low.	82574L

GBE0_CTREF	REF	1.8V	active[1]		**Gigabit Ethernet Controller 0:** Center Tap Reference Voltage for LAN magnetic, 1.8V	82574L

1) If Gigabit Ethernet Controller 0 is enabled in BIOS SETUP and Wake On LAN (WOL) is enabled in the network driver.

2.9.3 IDE

Signal Name	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
IDE_D[0:15]	I/O CMOS	3.3V	not active	iPD 11.5k IDE_D[7]	**IDE Device Data:** Bidirectional data to / from IDE device. 5V tolerant input.	US15W
IDE_A[0:2]	O CMOS	3.3V	not active		**IDE Device Address:** Selects bytes in ATA command block or control block of the IDE device.	US15W
IDE_IOW#	O CMOS	3.3V	not active		**IDE Device I/O Write**: Data is latched by the IDE device on the deassertion of IDE_IOW#.	US15W
IDE_IOR#	O CMOS	3.3V	not active		**IDE Device I/O read:** Data is latched by the US15W on the deassertion of IDE_IOR#.	US15W
IDE_REQ	I CMOS	3.3V	not active	iPD 15k	**IDE Device DMA Request:** It is asserted by the IDE device to request a data transfer. 5V tolerant input.	US15W
IDE_ACK#	O CMOS	3.3V	not active		**IDE Device DMA Acknowledge:** Asserted by the US15W to indicate that a given data transfer cycle is a DMA cycle.	US15W
IDE_CS1#	O CMOS	3.3V	not active		**IDE Device Chip Select:** Range 1F0h to 1FFh.	US15W
IDE_CS3#	O CMOS	3.3V	not active		**IDE Device Chip Select:** Range 3F0h to 3FFh.	US15W
IDE_IORDY	I CMOS	3.3V	not active	PU 4.7k	**IDE device I/O Ready:** Pulled low by the IDE device to extend the cycle. 5V tolerant input.	US15W
IDE_RESET#	O CMOS	3.3V	not active		**IDE Device Reset:** Reset output to IDE device, active low.	US15W
IDE_IRQ	I CMOS	3.3V	not active	PU 8.2k	**IDE Device Interrupt Request:** Interrupt request from IDE device. 5V tolerant input.	US15W
IDE_CBLID#	I CMOS	3.3V	not active	PD 10k	**IDE Cable Identification:** Input from IDE connector to indicate the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes. 5V tolerant input.	US15W

2.9.4 Serial ata

Signal Name	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
SATA0_TX+/-	O SATA	AC coupled on module	not active		**Serial ATA 0 Differential Transmit Pair:** These are outbound high-speed differential signals to SATA Port 0.	US15W

					In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.	
SATA0_RX+/-	I SATA	AC coupled on module	not active		**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from SATA Port 0.	US15W
SATA1_TX+/-	O SATA	AC coupled on module	not active		**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to SATA Port 1.	US15W
SATA1_RX+/-	I SATA	AC coupled on module	not active		**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from SATA Port 1.	US15W
ATA_ACT# ???????	OC	3.3V	not active	PU 10k iPD 15k [2]	**Serial ATA Activity Indicator:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tristated, the LED is off. **Note:** This pin is sampled as a functional strap. Refer to chapter ***2.9.5 PCI Express Lanes 0 – 5*** for details.	US15W

2) The internal pull-up is only enabled during PLTRST# assertion.

2.9.5 PCI express lanes 0-1

Signal Name (PCIe 1x)	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
PCIE_TX[0:1]+/-	O PCIE	AC coupled on module	not active		PCI Express Differential Transmit Pairs 0 through 1	US15W
PCIE_RX[0:1]+/-	I PCIE	AC coupled on module	not active		PCI Express Differential Receive Pairs 0 through 1	US15W
PCIE_CLK_REF+/-	O CMOS	3.3V	not active		Reference clock output for all PCI Express lanes	PI6C20400

2.9.6 Express card support

Signal Name	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
EXCD[0]_CPPE#	I CMOS	3.3V	not active		PCI ExpressCard: PCI Express capable card request, active low, one per card	EC
EXCD[1]_CPPE#	I CMOS	3.3V	not active		PCI ExpressCard: PCI Express capable card request, active low, one per card	EC
EXCD[0]_RST#	O CMOS	3.3V	not active		PCI ExpressCard: reset, active low, one per card	EC
EXCD[1]_RST#	O CMOS	3.3V	not active		PCI ExpressCard: reset, active low, one per card	EC

2.9.7 PCI Bus

Signal Name	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
PCI_AD[0:31]	I/O CMOS	3.3V	not active		PCI bus multiplexed address and data lines	XIO2001
PCI_C/BE[0:3]#	I/O CMOS	3.3V	not active		PCI bus byte enable lines, active low	XIO2001
PCI_DEVSEL#	I/O CMOS	3.3V	not active	PU 8k2	PCI bus Device Select, active low.	XIO2001
PCI_FRAME#	I/O CMOS	3.3V	not active	PU 8k2	PCI bus Frame control line, active low.	XIO2001
PCI_IRDY#	I/O CMOS	3.3V	not active	PU 8k2	PCI bus Initiator Ready control line, active low.	XIO2001
PCI_TRDY#	I/O CMOS	3.3V	not active	PU 8k2	PCI bus Target Ready control line, active low.	XIO2001
PCI_STOP#	I/O CMOS	3.3V	not active	PU 8k2	PCI bus STOP control line, active low, driven by cycle initiator.	XIO2001
PCI_PAR	I/O CMOS	3.3V	not active		PCI bus parity	XIO2001
PCI_PERR#	I/O CMOS	3.3V	not active	PU 8k2	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	XIO2001
PCI_REQ[0:3]#	I CMOS	3.3V	not active	PU 8k2	PCI bus master request input lines, active low.	XIO2001
PCI_GNT[0:3]#	O CMOS	3.3V	not active	iPU 20k	PCI bus master grant output lines, active low. **Note:** These signals are sampled as functional straps during power up. Refer to	XIO2001
PCI_RESET#	O CMOS	3.3V	active		PCI Reset output, active low.	XIO2001
PCI_LOCK#	I/O CMOS	3.3V	not active	PU 8k2	PCI Lock control line, active low.	XIO2001
PCI_SERR#	I/OD CMOS	3.3V	not active	PU 8k2	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	XIO2001
PCI_PME#	I/OD CMOS	3.3V	active	iPU 20k	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	XIO2001
PCI_CLKRUN#	I/O CMOS	3.3V	not active	PU 8k2	Bidirectional pin used to support PCI clock run protocol for mobile systems.	XIO2001
PCI_IRQ[A:D]#	I CMOS	3.3V	not active	PU 8k2	PCI interrupt request lines.	XIO2001
PCI_CLK	O CMOS	3.3V	not active		PCI 33MHz clock output.	XIO2001
PCI_M66EN	I CMOS	3.3V	not active		This input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation. If the module is not capable of supporting 66 MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66 MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33 MHz.	not supported

Note: All PCI signals I, I/O and I/OD signals are 5V input tolerant.

2.9.8 USB

Signal Name	Pin/Buffer Type	Power Rail	Suspend state	PU/PD	Description / Comment	Device
USB[0:7]+ USB[0:7]-	I/O USB	3.3V	active		USB 2.0 differential pairs, channels 0 through 7	US15W
USB_0_1_OC#	I CMOS	3.3V	active	PU 10k	USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. ***Don't pull this line high on the Carrier Board***.	US15W
USB_2_3_OC#	I CMOS	3.3V	active	PU 10k	USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. ***Don't pull this line high on the Carrier Board***.	US15W
USB_4_5_OC#	I CMOS	3.3V	active	PU 10k	USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. ***Don't pull this line high on the Carrier Board***.	US15W
USB_6_7_OC#	I CMOS	3.3V	active	PU 10k	USB over-current sense, USB channels 6 and 7. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. ***Don't pull this line high on the Carrier Board***.	US15W

2.9.9 LVDS flat panel

Signal Name	Pin/Buffer	Pwr Rail	Suspend	PU/PD	Description	Device

	Type		state			
LVDS_A[0:3]+ LVDS_A[0:3]-	O LVDS		not active not active		LVDS Channel A differential pairs	US15W
LVDS_A_CK+ LVDS_A_CK-	O LVDS		not active not active		LVDS Channel A differential clock	US15W
LVDS_VDD_EN	O CMOS	3.3V / 3.3V	not active		LVDS panel power enable	US15W
LVDS_BKLT_EN	O CMOS	3.3V / 3.3V	not active		LVDS panel backlight enable	US15W
LVDS_BKLT_CTRL	O CMOS	3.3V / 3.3V	not active		LVDS panel backlight brightness control	US15W
LVDS_I2C_CK	O CMOS	3.3V / 3.3V	not active		I2C clock output for LVDS display use	US15W
LVDS_I2C_DAT	I/O OD CMOS	3.3V / 3.3V	not active		I2C data line for LVDS display use	US15W

2.9.10 LPC Bus

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
LPC_AD[0:3]	I/O CMOS	3.3V / 3.3V	not active		LPC multiplexed address, command and data bus	US15W
LPC_FRAME#	O CMOS	3.3V / 3.3V	not active		LPC frame indicates the start of an LPC cycle	US15W
LPC_DRQ[0:1]#	I CMOS	3.3V / 3.3V	not active		LPC serial DMA request	US15W
LPC_SERIRQ	I/O CMOS	3.3V / 3.3V	not active		LPC serial interrupt	US15W
LPC_CLK	O CMOS	3.3V / 3.3V	not active		LPC clock output - 33MHz nominal	US15W

2.9.11 Analog VGA

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
VGA_RED	O Analog		not active	PD 150 Ohm	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	US15W
VGA_GRN	O Analog		not active	PD 150 Ohm	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	US15W
VGA_BLU	O Analog		not active	PD 150 Ohm	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	US15W
VGA_HSYNC	O CMOS	3.3V / 3.3V	not active		Horizontal sync output to VGA monitor	US15W
VGA_VSYNC	O CMOS	3.3V / 3.3V	not active		Vertical sync output to VGA monitor	US15W
VGA_I2C_CK	O CMOS	3.3V / 3.3V	not active	PU 2,2k	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	US15W
VGA_I2C_DAT	I/O OD CMOS	3.3V / 3.3V	not active	PU 2,2k	DDC data line.	US15W

2.9.12 SVDO

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
SDVOB_RED+ SDVOB_RED-	O PCIE	AC coupled on module	not active not active		Serial Digital Video B red output differential pair Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair	US15W GMCH
SDVOB_GRN+ SDVOB_GRN-	O PCIE	AC coupled on module	not active not active		Serial Digital Video B green output differential pair Multiplexed with PEG_TX[1]+ and PEG_TX[1]-	US15W GMCH
SDVOB_BLU+ SDVOB_BLU-	O PCIE	AC coupled on module	not active not active		Serial Digital Video B blue output differential pair Multiplexed with PEG_TX[2]+ and PEG_TX[2]-	US15W GMCH
SDVOB_CK+ SDVOB_CK-	O PCIE	AC coupled on module	not active not active		Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-	US15W GMCH
SDVOB_INT+ SDVOB_INT-	I PCIE	AC coupled off module	not active not active		Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-	US15W GMCH
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I PCIE	AC coupled off module	not active		Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-	not supported

SDVO_FLDSTALL+ SDVO_FLDSTALL-	I PCIE	AC coupled off module	not active		Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-	US15W GMCH
SDVO_I2C_CK	O CMOS	2.5V / 2.5V	not active		SDVO I2C clock line - to set up SDVO peripherals.	US15W GMCH
SDVO_I2C_DAT	I/O OD CMOS	2.5V / 2.5V	not active		SDVO I2C data line - to set up SDVO peripherals.	US15W GMCH

2.9.13 Miscellaneous

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
I2C_CK	O CMOS	3.3V / 3.3V		PU 2,2k	General purpose I2C port clock output	US15W/ GPIO2
I2C_DAT	I/O OD CMOS	3.3V / 3.3V		PU 2,2k	General purpose I2C port data I/O line	US15W/ GPIO1
SPKR	CMOS	3.3V / 3.3V	not active		Output for audio enunciator - the "speaker" in PC-AT systems	US15W
BIOS_DISABLE#	I CMOS	3.3V / 3.3V			Module BIOS disable input. Pull low to disable module BIOS.	Disables firmware hub
WDT	O CMOS	3.3V / 3.3V			Output indicating that a watchdog time-out event has occurred.	not supported
KBD_RST#	I CMOS	3.3V / 3.3V		PU 10k	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	US15W
KBD_A20GATE	I CMOS	3.3V / 3.3V		PU 10k	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC- AT. Pulled high on the module.	US15W

2.9.14 Power and System Management

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
PWRBTN#	I CMOS	3.3V / 3.3V Suspend			Power button to bring system out of S5 (soft off), active on rising edge.	US15W
SYS_RESET#	I CMOS	3.3V / 3.3V Suspend			Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.	US15W
CB_RESET#	O CMOS	3.3V / 3.3V Suspend			Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	US15W US15W FWH LAN TPM
PWR_OK	I CMOS	3.3V / 3.3V			Power OK from main power supply. A high value indicates that the power is good.	LTC1727
SUS_STAT#	O CMOS	3.3V / 3.3V Suspend			Indicates imminent suspend operation; used to notify LPC devices.	US15W
SUS_S3#	O CMOS	3.3V / 3.3V Suspend			Indicates system is in Suspend to RAM state. Active low output.	US15W
SUS_S4#	O CMOS	3.3V / 3.3V Suspend			Indicates system is in Suspend to Disk state. Active low output.	US15W
SUS_S5#	O CMOS	3.3V / 3.3V Suspend			Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.	US15W
WAKE0#	I CMOS	3.3V / 3.3V Suspend			PCI Express wake up signal.	US15W (82573)
WAKE1#	I CMOS	3.3V / 3.3V Suspend			General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	US15W
BATLOW#	I CMOS	3.3V / 3.3V Suspend			Indicates that external battery is low.	US15W
THRM#	I CMOS	3.3V / 3.3V			Input from off-module temp sensor indicating an over-temp situation.	US15W (GPI12)
THERMTRIP#	O CMOS	3.3V / 3.3V			Active low output indicating that the CPU has entered thermal shutdown.	CPU US15W
SMB_CK	I/O OD	3.3V / 3.3V	active	PU 6,8k	System Management Bus bidirectional clock line. Power	US15W

	CMOS	Suspend Rail			sourced through 5V standby rail and main power rails.	
SMB_DAT	I/O OD CMOS	3.3V / 3.3V Suspend Rail	active	PU 6,8k	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	US15W
SMB_ALERT#	I CMOS	3.3V / 3.3V Suspend Rail		PU 10k	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	US15W

2.9.15 General Purpose I/O

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
GPO[0:3]	O CMOS	3.3V / 3.3V			General purpose output pins. Upon a hardware reset, these outputs are low.	Micro controller
GPI[0:3]	I CMOS	3.3V / 3.3V			General purpose input pins. Pulled high internally on the module.	Micro controller

2.9.16 Module Type Definition

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
TYPE[0:2]#	PDS				The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) 24 rare no-connects (NC). For Pin-out Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pin-out Type 1 **NC NC NC Pin-out Type 2** NC NC GND Pin-out Type 3 (no DIE) NC GND NC Pin-out Type 4 (no PCI) NC GND GND Pin-out Type 5 (no DIE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin- out type is detected. The Carrier	MSC US15W

					Board logic may also implement a fault indicator such as an LED.	

2.9.17 Power and GND

Signal Name	Pin/Buffer Type	Pwr Rail	Suspend state	PU/PD	Description	Device
VCC_12V	Power				Primary power input: +12V (+/- 5%)	Voltage regulators
VCC_5V_SBY	Power				Standby power input: +5.0V (+/- 5%) If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	VCC3.3V SUS regulator
VCC_RTC	Power				Real-time clock circuit-power input : +3.0V (+2.0V – 3.3V)	US15W
GND	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

2.9.18 Pin List for MSC US15W module (Type 2)

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	IDE_D7	D2	IDE_D5
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	IDE_D6	D3	IDE_D10
A4	GBE0_LINK100#	B4	LPC_AD0	C4	IDE_D3	D4	IDE_D11
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	IDE_D15	D5	IDE_D12
A6	GBE0_MDI2-	B6	LPC_AD2	C6	IDE_D8	D6	IDE_D4
A7	GBE0_MDI2+	B7	LPC_AD3	C7	IDE_D9	D7	IDE_D0
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	IDE_D2	D8	IDE_REQ
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	IDE_D13	D9	IDE_IOW#
A10	GBE0_MDI1+	B10	LPC_CLK	C10	IDE_D1	D10	IDE_ACK#
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	IDE_D14	D12	IDE_IRQ
A13	GBE0_MDI0+	B13	SMB_CK	C13	IDE_IORDY	D13	IDE_A0
A14	GBE0_CTREF	B14	SMB_DAT	C14	IDE_IOR#	D14	IDE_A1
A15	SUS_S3#	B15	SMB_ALERT#	C15	PCI_PME#	D15	IDE_A2
A16	SATA0_TX+	B16	SATA1_TX+	C16	PCI_GNT2#	D16	IDE_CS1#
A17	SATA0_TX-	B17	SATA1_TX-	C17	PCI_REQ2#	D17	IDE_CS3#
A18	SUS_S4#	B18	SUS_STAT#	C18	PCI_GNT1#	D18	IDE_RESET#
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCI_REQ1#	D19	PCI_GNT3#
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCI_GNT0#	D20	PCI_REQ3#
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	*SATA2_TX+*	*B22*	*SATA3_TX+*	C22	PCI_REQ0#	D22	PCI_AD1
A23	*SATA2_TX-*	*B23*	*SATA3_TX-*	C23	PCI_RESET#	D23	PCI_AD3
A24	SUS_S5#	B24	PWR_OK	C24	PCI_AD0	D24	PCI_AD5
A25	*SATA2_RX+*	*B25*	*SATA3_RX+*	C25	PCI_AD2	D25	PCI_AD7
A26	*SATA2_RX-*	*B26*	*SATA3_RX-*	C26	PCI_AD4	D26	PCI_C/BE0#
A27	BATLOW#	B27	WDT	C27	PCI_AD6	D27	PCI_AD9
A28	ATA_ACT#	B28	AC_SDIN2	C28	PCI_AD8	D28	PCI_AD11
A29	AC_SYNC	B29	AC_SDIN1	C29	PCI_AD10	D29	PCI_AD13
A30	AC_RST#	B30	AC_SDIN0	C30	PCI_AD12	D30	PCI_AD15
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	C32	PCI_AD14	D32	PCI_PAR
A33	AC_SDOUT	B33	I2C_CK	C33	PCI_C/BE1#	D33	PCI_SERR#
A34	BIOS_DISABLE#	B34	I2C_DAT	C34	PCI_PERR#	D34	PCI_STOP#
A35	THRMTRIP#	B35	THRM#	C35	PCI_LOCK#	D35	PCI_TRDY#
A36	USB6-	B36	USB7-	C36	PCI_DEVSEL#	D36	PCI_FRAME#
A37	USB6+	B37	USB7+	C37	PCI_IRDY#	D37	PCI_AD16
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	PCI_C/BE2#	D38	PCI_AD18
A39	USB4-	B39	USB5-	C39	PCI_AD17	D39	PCI_AD20
A40	USB4+	B40	USB5+	C40	PCI_AD19	D40	PCI_AD22
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	PCI_AD21	D42	PCI_AD24
A43	USB2+	B43	USB3+	C43	PCI_AD23	D43	PCI_AD26
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	PCI_C/BE3#	D44	PCI_AD28
A45	USB0-	B45	USB1-	C45	PCI_AD25	D45	PCI_AD30
A46	USB0+	B46	USB1+	C46	PCI_AD27	D46	PCI_IRQC#
A47	VCC_RTC	*B47*	*EXCD1_PERST#*	C47	PCI_AD29	D47	PCI_IRQD#
A48	EXCD0_PERST#	*B48*	*EXCD1_CPPE#*	C48	PCI_AD31	D48	PCI_CLKRUN#
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	PCI_IRQA#	*D49*	*PCI_M66EN*
A50	LPC_SERIRQ	B50	CB_RESET#	C50	PCI_IRQB#	D50	PCI_CLK

= not supported on MSC US15W module

Row A		Row B		Row C		Row D	
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	*PCIE_TX5+*	*B52*	*PCIE_RX5+*	C52	PEG_RX0+	D52	PEG_TX0+
A53	*PCIE_TX5-*	*B53*	*PCIE_RX5-*	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	PEG_LANE_RV#
A55	*PCIE_TX4+*	*B55*	*PCIE_RX4+*	C55	PEG_RX1+	D55	PEG_TX1+
A56	*PCIE_TX4-*	*B56*	*PCIE_RX4-*	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PEG_RX2+	D58	PEG_TX2+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PEG_RX2-	D59	PEG_TX2-
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PEG_RX3+	D61	PEG_TX3+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PEG_RX3-	D62	PEG_TX3-
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PEG_RX4+	D65	PEG_TX4+
A66	GND	B66	WAKE0#	C66	PEG_RX4-	D66	PEG_TX4-
A67	GPI2	B67	WAKE1#	C67	RSVD	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PEG_RX5+	D68	PEG_TX5+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PEG_RX5-	D69	PEG_TX5-
A70	GND (FIXED)	B70	GND (FIXED)	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71	PEG_RX6+	D71	PEG_TX6+
A72	LVDS_A0-	B72	LVDS_B0-	C72	PEG_RX6-	D72	PEG_TX6-
A73	LVDS_A1+	B73	LVDS_B1+	C73	SDVO_DATA	D73	SDVO_CLK
A74	LVDS_A1-	B74	LVDS_B1-	C74	PEG_RX7+	D74	PEG_TX7+
A75	LVDS_A2+	B75	LVDS_B2+	C75	PEG_RX7-	D75	PEG_TX7-
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD	D77	IDE_CBLID#
A78	LVDS_A3+	B78	LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	RSVD	D83	RSVD
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	KBD_RST#	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	KBD_A20GATE	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE0_CK_REF+	B88	RSVD	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE0_CK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	RSVD	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	RSVD	B92	VGA_BLU	C92	PEG_RX12-	D92	PEG_TX12-
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	RSVD	B94	VGA_VSYNC	C94	PEG_RX13+	D94	PEG_TX13+
A95	RSVD	B95	VGA_I2C_CK	C95	PEG_RX13-	D95	PEG_TX13-
A96	GND	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	VCC_12V	*B97*	*TV_DAC_A*	C97	RSVD	D97	PEG_ENABLE#
A98	VCC_12V	*B98*	*TV_DAC_B*	C98	PEG_RX14+	D98	PEG_TX14+
A99	VCC_12V	*B99*	*TV_DAC_C*	C99	PEG_RX14-	D99	PEG_TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	VCC_12V	B101	VCC_12V	C101	PEG_RX15+	D101	PEG_TX15+
A102	VCC_12V	B102	VCC_12V	C102	PEG_RX15-	D102	PEG_TX15-
A103	VCC_12V	B103	VCC_12V	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

= not supported on MSC US15W module

3 Watchdog

The module has a watchdog function implemented using a microcontroller .

Via SETUP the watchdog can be enabled and configured.

If the watchdog is enabled a counter is started which creates a reset if it is not retriggered within a programmable time window.

The watchdog menu in the BIOS provides the following parameters:

Watchdog: Enabled / **Disabled** (default)

Initial Delay: 1s, 5s, 10s, **30s** (default), 1min, 5min, 10min, 30min
Timeout: 0,4s, 1s, 5s, 10s, **30s** (default), 1min, 5 min, 10min

Start on Boot: If yes, watchdog starts at the end of POST (power on selftest) before the OS is loaded

The watchdog can be accessed via the 16 Bit UEBI or the 32 Bit USPEPC software interface

4 System resources

4.1 Carrier Board PCI Resource Allocation

The external PCI resource allocation on the carrier board should be as follows:

Slot / Device Signal	Slot / Device 0	Slot / Device 1	Slot / Device 2	Slot / Device 3
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
PCI Clock	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTD# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#
REQ0# (if used)	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#
REQ1# (if used)	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#
REQ2# (if used)	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#
REQ3# (if used)	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#
GNT0# (if used)	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#
GNT1# (if used)	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#
GNT2# (if used)	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#
GNT3# (if used)	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#

The signals PCI_IRQx, PCI_REQx or PCI_GNTx are are routed exclusively to the COM Express connector. They are not shared on the CPU board.

4.2 PCI Devices

Qseven			Interrupts of Controller (US15W)							
Slot Number (or Onboard Device)	**IDSEL # or DEV. #**	**Bus #**	**PIRQ 0 (INT A)**	**PIRQ 1 (INT B)**	**PIRQ 2 (INT C)**	**PIRQ 3 (INT D)**	**PIRQ 4 (INT E)**	**PIRQ 5 (INT F)**	**PIRQ 6 (INT G)**	**PIRQ 7 (INT H)**
Internal Graphic Device	Dev 02h	0					A			
HD Audio	Dev 27 Fkt 2	0					A			
PCI Express Root Port	Dev 28 Fkt 0/1	0	B	A						
USB UHCI Host Controller	Dev 29 Fkt 0	0								A
USB UHCI Host Controller	Dev 29 Fkt 1	0							B	
USB UHCI Host Controller	Dev 29 Fkt 2	0							C	
USB EHCI Controller	Dev 29 Fkt 7	0						D		
SDIO	Dev 30 Fkt 0/1/2	0					A/B/C			
SATA (optional)	Dev ? Fkt 0	-			A					
GB Lan Controller (optional)	Dev ? Fkt 0	-		A* (NO switch)		A* (switch)				
PCIe Slot 1 (optional)	Dev ? Fkt 0	-	A	B	C	D				
PCIe Slot 2 (optional)	Dev ? Fkt 0	-	D	A	B	C				
PCI Slot 1	Dev ? Fkt 0	-	A	B	C	D				
PCI Slot 2	Dev ? Fkt 0		B	C	D	A				
PCI Slot 3	Dev ? Fkt 0		C	D	A	B				
PCI Slot 4	Dev ? Fkt 0		D	A	B	C				

*) Routing for GB Lan Controller depends on how it is connected to PCIe bus (device directly connected to PCIe root port or behind PCIe switch).

4.3 SMB Address Map

Device	A6	A5	A4	A3	A2	A1	A0	R/W	address *)
SCH US15W									Master
PCIe Switch (89HPES5T5)	0	1	1	1	0	1	1	x	76h / 3Bh
GigaBit LAN 82574L	1	1	0	0	0	0	1	x	C2h / 61h
SATA Controller JMB362	0	1	0	0	0	1	0	x	44h / 22h
Clock Generator CK610	1	1	0	1	0	0	1	x	D2h / 69h
Clock Buffer PI6C20400	1	1	0	1	1	1	0	x	DCh / 6Eh
CMOS backup EEPROM	1	0	1	0	1	0	0	x	A9h / 54h
SPD EEPROM (SO-DIMM)	1	0	1	0	0	0	0	x	A1h / 50h
H/W Monitor LM95245	1	0	0	1	1	0	0	x	99h / 4Ch
ADC MAX11601	1	1	0	0	1	0	0	x	C9h / 64h
EC EEPROM	1	0	1	0	1	0	0	x	A9h / 54h

*) 8 bit address (with R/W) / 7 bit address (without R/W)

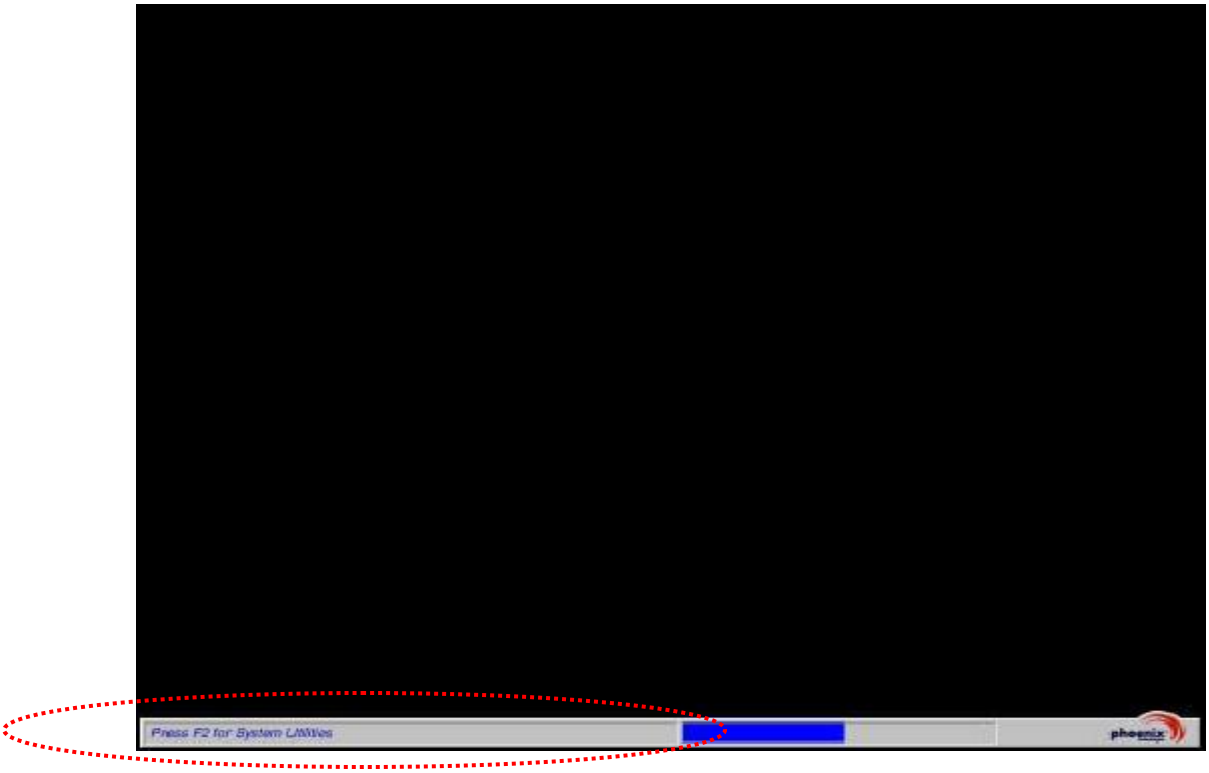
5 BIOS

5.1 Introduction

This guide describes the Phoenix TrustedCore Startup screen and contains information on how to access Phoenix TrustedCore setup to modify the settings which control Phoenix pre-OS (operating system) functions.

5.1.1 Startup Screen Overview

The Phoenix TrustedCore Startup screen is a graphical user interface (GUI) that is included in Phoenix TrustedCore products. The default bios behavior is to show an informational text screen during bios POST phase, but the graphical boot screen can be enabled in the bios setup. The standard boot screen is a black screen, including a progress bar at the bottom of the screen. This bar indicates the progress of the Startup Screen functions and provides user prompting and POST status. The following figure shows the various parts of a generic Startup Screen at 1024x768 resolution:



5.1.2 Activity Detection Background

While the Startup screen is displayed, press the Setup Entry key (F2 – TrustedCore default). The Startup Status Bar acknowledges the input, and at the end of POST, the screen clears and setup launches.
An example of the Startup Status Bar displaying changing state is shown in the following figure. The “Please Wait…” text is displayed after the F2 key is pressed to acknowledge user input.

Active status bar:

5.2 TrustedCore Setup Utility

With the Phoenix TrustedCore Setup program, you can modify TrustedCore settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter provides an overview of the Setup utility and describes at a high-level how to use it.

5.2.1 Configuring the System BIOS

To start the Phoenix TrustedCore Setup utility, press [F2] to launch Setup. The Setup main menu appears.

The BIOS Menu Structure

The BIOS Menu is structured in the following way:

Main		
	Board Information	
	Primary Master	
	Primary Slave	
	Keyboard Features	
	Boot Options	
Advanced		
	Cache Memory	
	Atom CPU Control Sub-Menu	
	Chipset Control Sub-Menu	
		PCI Express Control Sub-Menu
		PCI Control Sub-Menu
		USB Control Sub-Menu
	Video (Intel IGD) Control Sub-Menu	
	I/O Device Configuration	
	ACPI Control Sub-Menu	
	Watchdog Options	
Security		
Power		
	Hardware Monitor	
Boot		
Exit		

The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu Items	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Security	Use this menu to set User and Supervisor Passwords and the Backup and Virus-Check reminders.
Power	Use this menu to configure Power-Management features.
Boot	Use this menu to set the boot order in which the BIOS attempts to boot to OS.
Exit	Exits the current menu.

Use the left and right arrow keys on your keyboard to make a menu selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom of the screen to make your selections, or to exit the current menu. The following table describes the legend keys and their alternates:

Key	Function
F1 or Alt-H	General Help window.
Esc	Exit this menu.
Arrow keys	Select a different menu.
Up and down arrow keys	Move cursor up and down.
Tab or Shift-Tab	Move cursor left and right (i.e. at System Time / System Date).
Home or End	Move cursor to top or bottom of window.
PgUp or PgDn	Move cursor to next or previous page.
F5 or -	Select the previous value for the field.
F6 or + or Space	Select the next value for the field.
F9	Load the Default Configuration values (for all menus).
F10	Save and exit.
Enter	Execute command or select submenu.

Select an item

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

Display a submenu

To display a submenu, use the arrow keys to move the cursor to the sub menu you want. Then press Enter. A pointer marks all submenus.

5.2.2 The Main Menu

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options	Description
Board Information	Submenu	Displays BIOS Version
System Time	Enter Time (HH:MM:SS)	Set the System Time.
System Date	Enter Date (DD/MM/YYYY)	Set the System Date.
Primary Master	Submenu	Configure Primary Master settings
Primary Slave	Submenu	Configure Primary Slave settings
Keyboard Features	Submenu	Configure Keyboard Options
Boot Options	Submenu	Configure Boot Options

5.2.2.1 Board Information

Feature	Options	Description
HW Platform	Informative	Name of the hardware platform
HW Revision	Informative	Hardware revision number
Bios Version	Informative	Shows current bios version.
Serial #	Informative	Hardware Serial Number
MAC Address	Informative	Internal Lan Mac Adress
Boot Counter	Informative	The number of times this board has booted up.
CPU String	Informative	CPU Identification string
CPU Speed	Informative	CPU Speed
CPU Class	Informative	CPU ID Class code
CPU Model	Informative	CPU ID Model code
CPU Stepping	Informative	CPU ID Stepping
CPU Cores	Informative	Number of CPU cores
Microcode Patch ID	Informative	Microcode Patch ID
EC HW Name	Informative	Embedded Controller Hardware Name
EC HW Version	Informative	Embedded Controller Hardware Version
EC SW Name	Informative	Embedded Controller Software Version
EC SW Version	Informative	Embedded Controller software Version
System Memory	Informative	Amount of memory below 1MB
Extended Memory	Informative	Total amount of memory

5.2.2.2 Masters & Slaves

The **Master** and **Slave** settings on the Main Menu control these types of devices:

- **Hard-disk drives (IDE and SATA)**
- **Removable-disk drives**
- **CD-ROM drives**

There is one IDE connector on your motherboard, usually labeled "Primary IDE". There are usually two connectors on each ribbon cable attached to IDE connector. When you have connected two drives to this connector, the one on the end of the cable is the Master.

When you enter Setup, the Main Menu displays the results of **Autotyping** information each drive provides about its own size and other characteristics–and how they are arranged as Masters or Slaves on your machine.

Note: Using Master/Slave functionality is not possible if a Nand Drive is equipped on your module. So only the Nand Drive can be used on the Primary IDE.

Note: Do not attempt to change these settings unless you have an installed drive that does not autotype properly (such as an older hard-disk drive that does not support autotyping).

If you need to change your drive settings, select one of the Master or Slave drives on the Main Menu. This will display a menu like this:

Note: The capacity is displayed in 'real' Mbytes (1MB=1024*1024 Bytes) Drives with a total capacity greater than 8Gbyte operate in LBA format only.

Feature	Options	Description
Type	None, Auto, User, IDE Removable, ATAPI Removable, Other ATAPI, CD-ROM	**None** = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. **Auto** = Autotyping, the drive itself supplies the information. **User** = You supply the hard-disk drive information in the following fields. **IDE Removable** = Removable Disk Drive **ATAPI Removable** = Removable Disk Drive **Other ATAPI** = non-specific ATAPI Device **CD-ROM** = CD-ROM drive.
Cylinders	1 to 65536	Number of Cylinders
Heads	1 to 16	Number of read/write heads
Sectors	1 to 63	Number of sectors per track
Multi-Sector Transfers	Disabled, 2 sectors, 4 sectors, 8 sectors, 16 sectors	Any selection except **Disabled** determines the number of sectors transferred per block.
LBA Mode Control	Disabled, Enabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, & Sectors.

Feature	Options	Description
32 Bit I/O	Disabled, Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
Ultra DMA Mode	Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5	Ultra DMA Mode supports 33/66/100 MB/sec transfer rate for fixed disk drives.
SMART Monitoring	Disabled, Enabled	Displays the status of SMART Monitoring if supported by the used drive.

WARNING: Incorrect settings can cause your system to malfunction.

5.2.2.3 Keyboard Features

Feature	Options	Description
NumLock	Auto, On, Off	Selects Power-on state for NumLock
Keyclick	Enabled, Disabled	Enables Key click
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18.5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Selects key repeat rate
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Selects delay before key repeat

5.2.2.4 Boot Options

Feature	Options	Description
Summary screen	Disabled, Enabled	**Enabled** displays system configuration on boot.
Boot-time Diagnostic Screen	Disabled, Enabled	**Enabled** displays the diagnostic screen during boot. **Disabled** displays the Boot Logo.

Feature	Options	Description
Quick Boot Mode	Enabled, Disabled	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system. If enabled, SATA Oprom message will not appear.
Extended Memory Testing	Normal, Just zero it, None	Determines which type of test will be performed on extended memory during POST (above 1 MB).
Post Errors	Disabled, Enabled	Pauses and displays Setup Entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.

5.2.3 The Advanced Menu

Feature	Options	Description
Installed O/S	Other, Win95, Win98, WinMe, Win2000, WinXP	Select the operating system installed on your system which you will use most commonly. **NOTE**: An incorrect setting can cause some operating systems to display unexpected behavior.
Reset configuration Data	No, Yes	Select 'Yes' if you want to clear the Extended System Configuration Data (ESCD) area.
Large Disk Access Mode	Other, DOS	Select **Other** for UNIX, Novell NetWare. Select **DOS** for all other operating systems.
Small LBA-Disk CHS Translation	No, Yes	Select if CHS translation should be made for a LBA-capable hard disk with less than 1024 cylinders, e.g. CompactFlash(R). If you have problems with booting from a CompactFlash(R), try to change this setting. No = translate CHS only if HDD has >1024 cyls. Yes = translate CHS for all LBA-capable disks.

Feature	Options	Description
On-board Lan	Enabled, Disabled	Controls Power to the onboard Device Disabled = Disables the on-board LAN device. Enabled: Enables the on-board LAN device.
PXE OPROM	Enabled, Disabled	Enable PXE Option ROM for the onboard LAN device. Note: This option is appears only if the on-board LAN device is enabled.
Serial ATA OPROM	Enabled, Disabled	Enables or disables the Onboard Serial ATA OPROM. Note: To enable SATA Oprom message, Quick Boot has to be disabled.
Serial ATA Mode	Enhanced, Compatible	Compatible: SATA Controller is in Legacy Mode. Enhanced: SATA Controller is in Native Mode. **Note:** -To install Win XP in Enhanced Mode, it is necessary to include Jmicron Drivers by Floppy during Installation by pressing F6. Otherwise it is also possible to install in compatible mode and install Jmicron Drivers after Installation. -In both cases it is **recommended** to install the latest JMicron Sata drivers for correct functionality.
SDIO Card Boot OPROM	Enabled, Disabled	Enable or disable the SD Controller's Bootrom which adds support for booting from SD cards.
Cache Memory	Submenu	Configure Cache Memory
CPU Control Sub-Menu	Submenu	Configure CPU Control
Chipset Control Sub-Menu	Submenu	Configure MCH Control
Video (Intel IGD) Control Sub-Menu	Submenu	Configure Video (Intel IGD) Control
I/O Device Configuration	Submenu	Configure I/O Device

Feature	Options	Description
ACPI Control Sub-Menu	Submenu	Configure ACPI Control
Watchdog Option	Submenu	Configure Watchdog

5.2.3.1 Cache Memory Control Menu

Feature	Options	Description
Memory Cache:	Enabled, Disabled	Sets the state of the memory cache.
Cache System BIOS area	Uncached, Write Protect	Enables caching of system BIOS area.
Cache Video BIOS area	Uncached, Write Protect	Enables caching of video BIOS area.
Cache D000 – D3FF Cache D400 – D7FF Cache D800 – DBFF Cache DC00 - DFFF Cache E000 – E3FF	Disabled, Write Through, Write Protect, Write Back	**Disabled** = This block is not cached. **Write through** = Writes are cached and sent to main memory at once. **Write Protect** = Writes are ignored. **Write Back** = Writes are cached but not sent to main memory until necessary.

5.2.3.2 Atom CPU Control Sub-Menu

Feature	Options	Description
Hyperthreading	Enabled, Disabled	Enabling Hyperthreading activates additional CPU threads. These threads may appear as additional processors but will share some resources with other threads within the physical package. ***Note:*** ***Only supported by Intel Atom Z530***
Processor Power Management	Disabled, GV3 only, C-States Only, Enabled	Selects the Processor Power Management desired: Disabled = C-States and GV3 are disabled. GV3 Only = C-States are disabled. C-States Only = GV3 is disabled. Enabled = C-States und GV3 are enabled. **Note**: GV3 refers to the speed step capability of the CPU. **Note**: If GV3 is disabled, OS will not run with maximum frequency. To use maximum frequency, GV3 has to be enabled and OS must Control the CPU frequency via Power management. **Note**: For optimal response times the GV3 (Speed step) must be enabled and C-States disabled. Also disable C-States if using RS232 @ 115k baud. Otherwise receiving errors could occur.
Enhanced C-States	Enabled, Disabled	Enables Enhanced C-State support Disabled = Enhanced C-States disabled. Enabled = Enhanced C-States enabled.
Thermal Control Circuit	Disabled TM1 TM2 TM1 and TM2	Setting this bit enables the thermal control circuit (TCC) portion of the Thermal Monitor feature of the CPU. Intel Thermal Monitor TM1= 50% duty cycle TM2= Geyserville III

Feature	Options	Description
DTS Enable	Disabled, Enabled	Enables the Atom DTS to be used for platform Thermal Management.
No Execute Mode Mem Protection	Enabled, Disabled	Reduces exposure to viruses and malicious-code attacks and prevents harmful software from executing and propagating on the server or network.
Intel ® Virtualization Technology	Enabled, Disabled	Enables or disables Intel Virtualization Technology. ***Note:*** ***Only supported by Intel Atom Z530***
Set Max Ext CPUID = 3	Disabled, Enabled	Sets Max CPUID extended function value to 3.

5.2.3.3 US15W Control Sub-Menu

Feature	Options	Description
PCI Express Control Sub-Menu	Sub-Menu	Configure PCI Express Control
PCI Control Sub-Menu	Sub-Menu	Additional setup menus to configure PCI devices.
USB Control Sub-Menu	Sub-Menu	Configure USB Control
CK-610 Clock Controller	Default, Program	Control Programming of the CK-610 Clock Chip. Default = Power On Default Values
CPU Spread Spectrum	Off, Down Spread	Programming of CPU Spread Spectrum Clock. Off = SPU Spread Spectrum is disabled. Down Spread= 0.5%
Graphic Spread Spectrum	Off, Software	Programming of Graphic Spread Spectrum Off = Graphic Spread Spectrum is disabled.
Spread Percentage	Down : 0.5% , 1%, 2%, 2.5% center: 0.25%, 0.5%, 1%, 1.25%	Select Percentage for the Graphic Spread Spectrum. If set to software Controlled, the use may select from the following Spread ranges: Down Spread range is from -0.5% to -2.5% Center Spread range is from +- 0.25% to +-1.25%

Feature	Options	Description
HD Audio Controller	Disabled, Auto	Control Detection of the Azalia Device. Dev 27, Fun 0 Disabled = Azalia will be unconditionally disabled, regardless of presence. Auto = Azalia will be enabled if present, disabled otherwise.
SDIO Controller	Enabled, Disabled	Control SDIO functionality through this Setup Item. Dev 30, Fun 0/1/2
Pop Up Mode Enable	Disabled, Enabled	Select the proper mode: If disabled, bus master traffic is a break event and it will return from C3/C4 to C0 based on break events. If enabled, ICH will observe a bus master request and it will take the system from a C3/C4 state to a C2 state and auto enable bus masters.
Pop Down Mode Enable	Disabled, Enabled	Should be enabled only if Pop up is enabled: If disabled, ICH will NOT attempt to automatically return. If enabled, ICH will observe a NO bus master request and it can return to a previous C3 or C4 state.

5.2.3.4 PCI Express Control Sub-Menu

Feature	Options	Description
PCI Express – Root Port 1	Disabled, Enabled, Auto	Control PCI Express Port via this setup option. Disabled = Port always Disabled. Auto = Only enable if card found. Note that if Root Port 1 is disabled Root Port 2 will be disabled as well.
PCI Express – Root Port 2	Disabled, Enabled, Auto	Control PCI Express Port via this setup option. Disabled = Port always Disabled. Auto = Only enable if card found. Note that if Root Port 1 is disabled Root Port 2 will be disabled as well.
Root Port ASPM Support	Disabled, Auto	Control ASPM support for all the enabled Root Ports. Auto = will set APMC to the highest common supported ASPM between the Port and Endpoint.
ASPM Latency Checking	Disabled, Enabled	Disabled: ASPM latencies are ignored when enabling ASPM. Enabled: Enables ASPM latency checking when enabling ASPM.
PCIe Drive Strenght	Disabled, Enabled	Enables or disables the PCIe drive strength or PCIe port 1.

5.2.3.5 PCI Control Sub-Menu

Feature	Options	Description
PCI IRQ Line 0	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports, PCI Slots

Feature	Options	Description
PCI IRQ Line 1	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports, PCI Slots
PCI IRQ Line 2	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports, PCI Slots
PCI IRQ Line 3	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: PCIe Ports, PCI Slots
PCI IRQ Line 4	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: Internal Graphics, HD Audio, SD Card Controller
PCI IRQ Line 5	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: EHCI Controller
PCI IRQ Line 6	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: UHCI Controller 2, UHCI Controller 3
PCI IRQ Line 7	Auto Select, 3, 4, 5, 6, 7, 10, 11, 12	Select which Interrupt should be assigned to this PCI Irq Devices: UHCI Controller 1

5.2.3.6 USB Control Sub-Menu

Feature	Options	Description
USB 1.1 Controllers	Port 0-1 Port 0-3 Port 0-5	Select the number of enabled USB1.1 Controllers. Port 0-1 = Dev 29, Fun 0 Port 2-3 = Dev 29, Fun1 Port 4-5 = Dev 29, Fun 2 Note: Port 6-7 can only be used as USB 2.0 Port 1 in the chipset is equivalent to Port 2 on the Q7 connector. Port 2 in the chipset is equivalent to Port 1 on the Q7 connector.
USB 2.0 Ports	Disabled, Enabled	Control USB 2.0 functionality of port 0-7 through this Setup Item. Dev 29, Fun 7 Note: Port 6-7 can only be used as USB 2.0

5.2.3.7 Video (Intel IGD) Control Sub-Menu

Feature	Options	Description
IGD – Device 2	Disabled, Auto	Enables or Disable the Internal Graphics Device by setting item to the desired value.
IGD – Boot Type	VBIOS default, CRT, LFP, TV, EFP,	Select the Video Device that will be activated during POST.
Pre-Allocated Memory Size	1 MB, 4 MB, 8 MB	Select the amount of Pre-Allocated Graphics Memory for use by the Internal Graphics Device.

Feature	Options	Description
IGD – LCD Panel Type	640x480 1 PPC, 18b 800x600 1 PPC, 18b 1024x768 1 PPC, 18b 640x480, 1 PPC, 18b 800x480, 1 PPC, 18b 1024x600 1 PPC, 18b 800x480 1 PPC, 24b 800x600 1 PPC, 24b 1024x768 1 PPC, 24b 1280x800 1 PPC, 24b 1366x768 1 PPC, 24b 12: Reserved 13: Reserved 1280x800, 1PPC, 18b 1280x600, 1PPC, 18b 1366x768, 1PPC, 18b	Select the LCD panel used by the Internal Graphics Device by selecting the appropriate setup item. The first item is Panel 1, the last item is Panel 16. Some Panels are not numbered due to size constraints. **Note**: Due to size constrains not all Panels are exactly numbered. The first item is Panel 1, the last one Panel 16.
IGD – Panel Scaling	Auto, Force Scaling, Off	Selects the LCD panel scaling option used by the Internal Graphics Device. 1. Auto 2. Force Scaling 3. Off
Backlight Brightness	10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100%	Select the starting brightness for the LVDS backlight signal. **Note**: some backlight inverters use an inverted level for brightness control – please check the inverter spec. for the display panel
Onbaord EDID EEPROM	Disabled, Enabled	Enables or disables the Onboard EDID EEPROM
SDVO Drive Strenght	Disabled, Enabled	Enables or disables SDVO drove strength.

5.2.3.8 I/O Device Configuration Menu

Feature	Options	Description
Serial Port A	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port A.
Interrupt	3, 4	Set the interrupt for Serial Port A.
Serial Port B	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Mode	Normal, IR, ASK-IR	Set the mode for Serial Port B (wired / infrared).
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port B.
Interrupt	3, 4	Set the interrupt for Serial Port B.
Parallel Port	Diabled, Enabled, Auto	Configure Parallel Port using options: Disabled: No Configuration Enabled: User Configuration Auto: Bios or OS chooses configuration (OS controlled): Displayed when controlled by OS
Mode	Output only, Bi-directional, ECP	Set the mode for Parallel Port.
Base I/O address	378, 278, 3BC	Set the base I/O address for Parallel Port.
Interrupt	5, 7	Set the interrupt for Parallel Port.
DMA channel	1, 3	Set the DMA channel for Parallel Port (only available if mode was set to ECP).

Warning: If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting settings.

Note: Depending on type of the Super IO used it is possible to have more than 2 Com Ports selectable in this Menu.

Note: If using RS232 @ 115k baud, it is recommended to disable C-States and enable GV-3 only in CPU-Control Sub-Menu. Otherwise receiving errors could occur due to chipset and cpu related limitations.

5.2.3.9 ACPI Control Sub-Menu

Feature	Options	Description
Passive Cooling Trip Point (only valid for Z510 PT CPU and Z520 PT CPU)	Disabled, 63° C, 71° C, 79° C, 87° C, 95° C, 103° C	This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the CPU.
Passive Cooling Trip Point (only valid for Z510P CPU and Z530P CPU)	Disabled, 63° C, 71° C, 79° C, 87° C	This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the CPU.
Passive TC1 Value, Passive TC2 Value,	0 – 15	This value sets the TC1-2 value for the ACPI Passive Cooling Formula.
Passive TSP Value	1 – 15	This item sets the TSP value for the ACPI Passive Cooling Formula. It represents in tenths of a second how often the OS will read the temperature when Passive Cooling is Enabled.
Critical Trip Point (only valid for Z510 PT CPU and Z520 PT CPU)	POR, 63° C, 71° C, 79° C, 87° C, 95° C, 103° C	This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off. POR=110°C (Tjmax)
Critical Trip Point (only valid for Z510P CPU and Z530P CPU)	POR, 63° C, 71° C, 79° C, 87° C	This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off. POR=90°C (Tjmax)
FACP – RTC S4 Flag Value	Disabled, Enabled	Valid only for ACPI Control the value for the RTC S4 flag in the FACP Table
FACP – PM Timer Flag Value	Disabled, Enabled	Valid only for ACPI Controls the timer used by the OS through the FACP Tables Flags. This is now possible with WINXP SP2 and beyond.
HPET Support	Disabled, Enabled	This field is valid only in the WindowsXP OS. Control the High Performance Event Timer through this setup option when enabled. The HPET Table will then be pointed to by the RSDT and the proper enable bits will be set.

Feature	Options	Description
HPET Base Address	0xFED00000, 0xFED01000, 0xFED02000, 0xFED03000	Select the Base Address for the High Performance Event Timer.

5.2.3.10 Watchdog Options

Feature	Options	Description
Watchdog delay	1 second, 5 seconds, 10 seconds, 30 seconds 1 minute , 5 minutes, 10 minutes, 30 minutes	After watchdog is activated, it waits selected delay time before it starts counting the timeout period.
Watchdog timeout	0.4 second, 1 second, 5 seconds, 10 seconds, 30 seconds, 1 minute , 5 minutes, 10 minutes	Select the maximum watchdog trigger period. If the watchdog will not be triggered during selected period, system reset will be generated.
Watchdog start on boot	No, Yes	Select if the watchdog should be started at the end of POST.

5.3 The Security Menu

Feature	Options	Description
Supervisor Password Is	Displays Supervisor Password Is	Displays the current status of the Supervisor password (“Clear” or “Set”)
User Password Is	Displays User Password Is	Displays the current status of the User password (“Clear” or “Set”)
Set Supervisor Password	Press return to enter supervisor password	Supervisor Password controls access to the setup utility.
Set User Password	Press return to enter user password	User Password controls access to the system at boot.
Password on boot	Disabled, Enabled	Enables password entry on boot

5.4 The Power Menu

Feature	Options	Description
After Power Failure	Power On, Off	Sets the mode of operation if an AC Power Loss occurs.
Power Button Wake	Always, S4/S5 only	This item controls from which sleep state the Power Button shall wake the system. Always – from S3, S4 and S5 S4/S5 only – from S4 and S5
Wake Signal	Off, S3 only, S4/S5 only, Always	This item controls from which sleep state the Wake signal shall wake the system. Off – Never S3 – from S3 only S4/S5 only – from S4 and S5 Always – from S3, S4 and S5
Hardware Monitor	Submenu	Configure Hardware Monitor

5.4.1.1 Hardware Monitoring Menu

Feature	Description
CPU Temperature Sensor	Displays the current CPU temperature.
Local Temperature	Displays the current local temperature on the bottom side near the RAM.
Fan Speed	Displays current Fan Speed in RPM.

5.5 The Boot Menu

After you turn on your computer, it will attempt to load the operating system (such as DOS, Windows XP or Linux) from a device listed in the boot priority order. If it cannot find the operating system on that device, it will attempt to load it from the next device in that list. Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD ROMs, removable devices (e.g. USB sticks), and network cards.

Note: Specifying any device as a boot device on the Boot Menu requires the availability of an operating system on that device.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

Feature	Description
Boot priority order: 1: USB KEY: 2: USB HDD: 3: IDE HDD: 4: USB-CD ROM 5: PCI SCSI: 6: PCI BEV: 7: 8:	Boot priority order for next boot. System tries to boot the first bootable device in this list. Use <+> and <-> to change order. Use <x> to exclude or include device to boot priority list.
Exclude from boot order: : USB FDC: : Bootable Add-in Cards : IDE CD:	System does not try to boot a device from this list.

Pressing the “F10” key during the bios boot phase will bring up the bios boot menu, which will allow you to select a different boot device for the current boot process only. In this boot menu, only devices in the “Boot priority list” will selectable. Devices excluded from boot order will not be shown.

5.6 The Exit Menu

The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Exit Saving Changes

After making your selections on the Setup menus, always select "Exit Saving Changes". This procedures stores the selections displayed in the menus in CMOS (short for "battery-backed CMOS RAM") a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.
If you attempt to exit without saving, the program asks if you want to save before exiting.
During boot-up, PhoenixBIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu.
If, during boot-up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

System CMOS checksum bad - run SETUP Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.
Press <F1> to resume the boot or <F2> to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS. Selecting “Discard Changes” on the Exit menu updates all the selections with their previous values.

Save Changes

Selecting “Save Changes” saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

5.7 BIOS and Firmware Update

If a System-BIOS and Microcontroller Firmware update is required please follow these instructions:

Firmware update:

1.) Create a bootable DOS disk/usb-stick/hdd.

2.) Copy the directories \BIOS and \Firmware to this device.

3.) Boot the system from this device.

4.) Change to the directory \Firmware

5.) Type "ecupdate" to update the System Firmware.

6.) When the Firmware update has finished, the system switches off automatically.

NOTE : depending on how old the previous Firmware version was, the Firmware update may well fail on the first attempt (board reboots or turns off without any update) In this case simply repeat the procedures 3 – 6 above.

BIOS update:

1. to 3.) see above

4.) Change to the directory \BIOS

5.) Type "update" to update the System BIOS.

6.) When the BIOS update has finished, reboot the system.

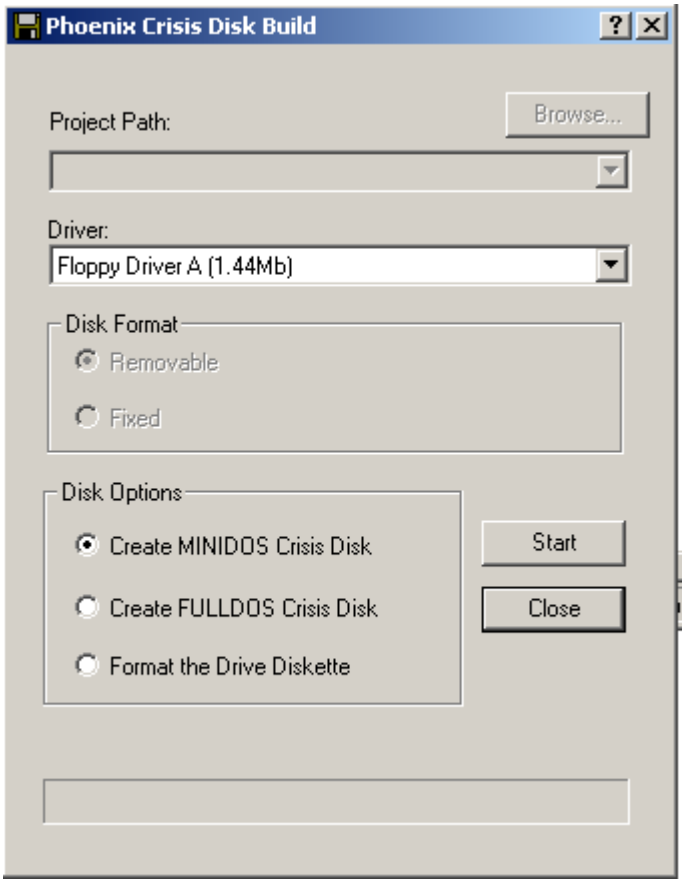
Note: After the system has been updated, the CMOS has been changed to defaults and therefore it is necessary to enter Setup (press F2 at boot time) to configure the system settings.

5.8 Bios Crisis Recovery

Note: Contact Technical Support for information on how to obtain the CRISDISK.ZIP software and a USB recovery dongle.

Please follow these simple steps to create a bootable crisis recovery medium:

Unzip CRISDISK.ZIP and start the windows-based program WINCRIS.EXE on the host system. A window will pop up as shown below:



In the drop-down box, either select “Floppy Drive A” to create a recovery disk, or select “Removable Disk 0 (xxxMb)” to create a recovery usb stick. Disk options should be left at “Create MINIDOS Crisis Disk”.

Press the start button to generate the selected crisis recovery medium.

There are two possibilities to force the target system into crisis recovery mode: either by USB crisis recovery dongle or by crisis recovery jumper.

With the dongle, you just have to plug it into a free USB port before switching the system on. Please make sure that you use different USB controllers for USB dongle and USB crisis recovery medium. After powerup, crisis recovery mode should automatically start.

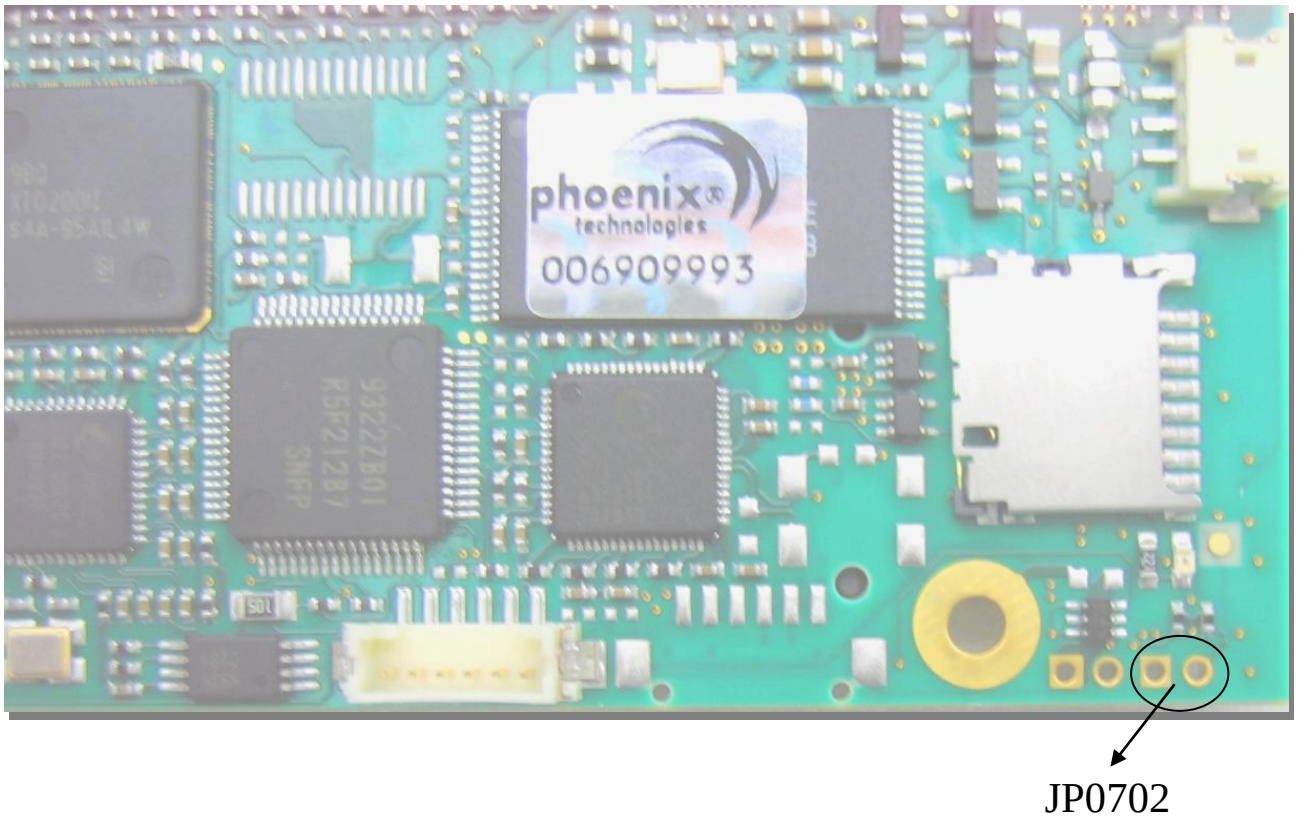
The programming process is signalled by short beeps and terminated after successfull programming with one long beep. After that, the system is automatically rebooted.

Important Notes:

USB recovery dongle and USB crisis recovery device must not be plugged to the same USB controller.
Crisis recovery may take up to 5 minutes
A long beep indicated successful recovery
Crisis recovery does not include the bootblock.

If a bios crisis recovery is necessary and you use the crisis recovery jumper please short the JP0702 with a small tweezers and press the reset button. After the crisis beep you can release the tweezers.

Please see also the bios recovery procedure described in the ***Bios crisis recovery*** section.



5.9 Diagnostics Postcodes

Postcodes can be seen on a special Postcode display, either on the MSC mainboard or on an external Postcode PCI card. There is an item in the bios setup to select the bus that should get the postcode data: either PCI (for external cards) or LPC (for onboard displays).

If a postcode display has only 2 digits, only the lower byte of word-value postcodes will be shown.

5.9.1 Bootblock Bios Postcodes

Code	Bootblock Task Description
BBH	Bootblock Early Init after Reset
80h	Chipset Init
81h	Bridge Init
82h	CPU Init
83h	System Timer Init
84h	System I/O Init
85h	Check forced Recovery Boot, CMOS & CMOS Backup Clear
86h	Check BIOS Checksum
87h	Goto BIOS, start early BIOS initialzations
88h	Init Multi Processor
89h	Set Huge Segment
8Ah	OEM Initializations
8Bh	Init Interrupt and DMA Controller
8Ch	Init Memory Type
8Dh	Init Memory Size
8Eh	Shadow Boot Block
8Fh	Init SMM
90h	System Memory Test
91h	Init Interrupt Vectors
92h	Init Realtime Clock
93h	Init Standard Video
94h	Init Beeper
95h	Initialize USB Controller
95h	Init Boot
96h	Clear Huge Segment
97h	Boot OS
99h	Init Security

5.9.2 System Bios Postcodes

Code	Beeps	POST Task Description
04h		Get CPU type
03h		Disable Non-Maskable Interrupt (NMI)
06h		Initialize system hardware
07h		Disable shadow and execute code from the ROM.
08h		Initialize chipset with initial POST values
09h		Set IN POST flag
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component
0Fh		Initialize fixed disk drives
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1-2-2-3	BIOS ROM checksum
17h		Initialize cache before memory Autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable Interrupt Controller
20h	1-3-1-1	Test DRAM refresh
22h	1-3-1-3	Test 8742 Keyboard Controller
24h		Set ES segment register to 4 GB
28h		Autosize DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 kB Base RAM
2Ch	1-3-4-1	RAM Address test
2Eh	1-3-4-3	Base RAM Test
2Fh		Enable cache before system BIOS shadow
32h		Compute CPU clock speed in MHz
33h		Initialize Phoenix Dispatch Manager
36h		Warm start shut down
38h		Shadow system BIOS ROM
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
41h		Initialize RomPilot
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2-1-2-3	Check ROM copyright notice
47h		Initialize I20 support
48h		Check video configuration against CMOS
49h		Initialize PCI bus and devices
4Ah		Initialize all video adapters in system
4Bh		QuietBoot start (optional)
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
4Fh		Initialize MultiBoot
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard

Code	Beeps	POST Task Description
54h		Set key click if enabled
55h		Configure USB devices
58h	2-2-3-1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press F2 to enter SETUP"
5Bh		Disable CPU cache
5Ch		Conventional memory test
60h		Extended memory test
62h		Address Test on Extended Memory
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		CPU feature, MP, and APIC initialization
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display BIOS shadow status
70h		Display error messages
72h		Check for configuration errors
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Dh		Initialilze Intelligent System Monitoring
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs
81h		Late POST device initialisation
82h		Detect and install external RS232 ports
83h		Configure non-MCD IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices
86h		Re-initialize onboard I/O ports.
87h		Configure Motheboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers
91h		Program timing registers according to PIO modes
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1-2	Enable PCI devices and ROM Scan One long, two short beeps on checksum failure
99h		Check for SMART Drive
9Ah		Shadow option ROMs
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives
A0h		Set time of day
A2h		Check key lock
A4h		Initialize typematic rate

Code	Beeps	POST Task Description
A8h		Erase F2 prompt
AAh		Scan for F2 key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B1h		Inform RomPilot about the end of POST.
B2h		POST done - prepare to boot operating system
B3h		store enhanced CMOS values in non-volatile area
B4h		1 One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)
B7h		Initialize ACPI BIOS
B9h		Prepare Boot
BAh		Initialize DMI parameters
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Check virus and backup reminders
C0h		Try to boot with INT 19
C1h		Initialize POST PEM Error Manager
C2h		Initialize PEM error logging
C3h		Initialize error PEM display function
C4h		Initialize PEM system error handler
C5h		PnPnd dual CMOS (optional)
C6h		Initialize note dock (optional)
C7h		Initialize note dock late
C8h		Force check (optional)
C9h		Extended checksum (optional)
CAh		Redirect Int 15h to enable remote keyboard
CBh		Redirect Int 13h to Memory Technologies
CCh		Redirect Int 10h to enable remote serial video
CDh		Remap I/O and memory for PCMCIA
CEh		Initialize digitizer and display message
D2h		Unknown interrupt or exception

5.9.3 Memory Detection Postcodes

Code	Calistoga Memory Detection
FFA0h	Start memory detection
FF01h	Enable MCHBAR
FF02h	Check for DRAM initialisation interrupt and reset fail
FF03h	Verify all DIMMs are DDR2 and unbuffered
FF04h	Detect an improper warm reset and handle
FF05h	Detect if ECC SO-DIMMs are present in the system
FF06h	Verify all DIMMs are single or double sided and not asymmetric
FF07h	Verify all DIMMs are x8 or x16 width
FF08h	Find a common CAS latency between the DIMMS and the MCH
FF09h	Determine the memory frequency and CAS latency to program
FF10h	Determine the smallest common TRAS for all DIMMs
FF11h	Determine the smallest common TRP for all DIMMs
FF12h	Determine the smallest common TRCD for all DIMMs
FF13h	Determine the smallest refresh period for all DIMMs
FF14h	Verify burst length of 8 is supported by all DIMMs
FF15h	Determine the smallest tWR supported by all DIMMs
FF16h	Determine DIMM size parameters
FF17h	Program Graphics frequency and PLL settings
FF18h	Program system memory frequency
FF19h	Determine and set the mode of operation for the memory channels
FF20h	Program clock crossing registers
FF21h	Disable Fast Dispatch
FF22h	Program the DRAM Row Attributes and DRAM Row Boundary registers
FF23h	Program the DRAM Bank Architecture register
FF24h	Program the DRAM Timing & and DRAM Control registers
FF25h	Program ODT
FF26h	Perform steps required before memory init
FF27h	Program the receive enable reference timing control register Program the DLL Timing Control Registers , RCOMP settings
FF28h	Enable DRAM Channel I/O Buffers
FF29h	Enable all clocks on populated rows
FF30h	Perform JEDEC memory initialization for all memory rows
FF31h	Program PM Settings
FF32h	Perform additional steps required after memory init
FF33h	Program DRAM throttling and throttling event registers
FF34h	Setup DRAM control register for normal operation and enable
FF35h	Setup DRAM control register for normal operation and enable
FF36h	Enable RCOMP
FF37h	Clear DRAM initialization bit in the ICH

5.9.4 ACPI Postcodes

Code	ACPI Codes
03h	Enter Suspend State S3
04h	Enter Hibernate State S4
05h	Enter Softoff State S5
ABh	Enter Wakeup from Powerstate
CDh	End Wakeup from Powerstate