

## Datasheet

### Main Features

- Single Core ADC Architecture with 10-bit Resolution integrating a Selectable 1:1/2/4 DEMUX
- 1.5 Gsps Guaranteed Conversion Rate
- Differential input Clock (AC coupled)
- Analogue input Voltage: 500 mVpp Differential Full Scale (AC Coupled)
- Analogue and Clock Input Impedance: 100 $\Omega$  Differential
- LVDS Differential Output Data with Swing Adjustment and Data Ready
- Fine Adjustment of ADC Gain, Offset
- Fine Adjustment of Sampling Delay for Interleaving
- Static and Dynamic Test Mode for ADC and DEMUX
- Data Ready Common to the 4 Output Ports
- 1.7 W Power Dissipation
- Power Supply: 5.2V, 3.3V and 2.5V (Output Buffers)
- fpBGA 196 RoHS Package



### Performances

- 2.2 GHz Full Power Input Bandwidth (-3 dB)
- Gain Flatness:
  - 0.5 dB from 10 MHz to 1500 MHz (1<sup>st</sup> & 2<sup>nd</sup> Nyquist)
  - 1.0 dB from 1500 MHz to 1800 MHz (L-band)
- Single Tone Performance:
  - SFDR = 59 dBFS, ENOB = 8.2 bit\_FS, SNR = 54 dBFS at Fin = 750 MHz, -3 dBFS, Fs = 1.5 Gsps
  - SFDR = 59 dBFS, ENOB = 8.0 bit\_FS, SNR = 51 dBFS at Fin = 1800 MHz, -3 dBFS, Fs = 1.5 Gsps
  - SFDR = 58 dBFS, ENOB = 8.1 bit\_FS, SNR = 53 dBFS Fin = 750 MHz, -1 dBFS, Fs = 1.5 Gsps
  - SFDR = 56 dBFS, ENOB = 7.7 bit\_FS, SNR = 50 dBFS at Fin = 1800 MHz, -1 dBFS, Fs = 1.5 Gsps
  - SFDR = -60 dBFS, ENOB = 8.5 Bit; SNR = 55 dBFS at Fin = 750 MHz @-12 dBFS, Fs = 1.5 Gsps
  - SFDR = -60 dBFS, ENOB = 8.2 Bit; SNR = 53 dBFS at Fin = 1800 MHz @-12 dBFS, Fs = 1.5 Gsps
- Broadband Performance:
  - NPR = 45 dB at -13 dBFS Optimum Loading Factor in 1st Nyquist
  - NPR = 43 dB at -13 dBFS Optimum Loading Factor in L-band
- Latency 2.5 Clock Cycles

### Main Applications

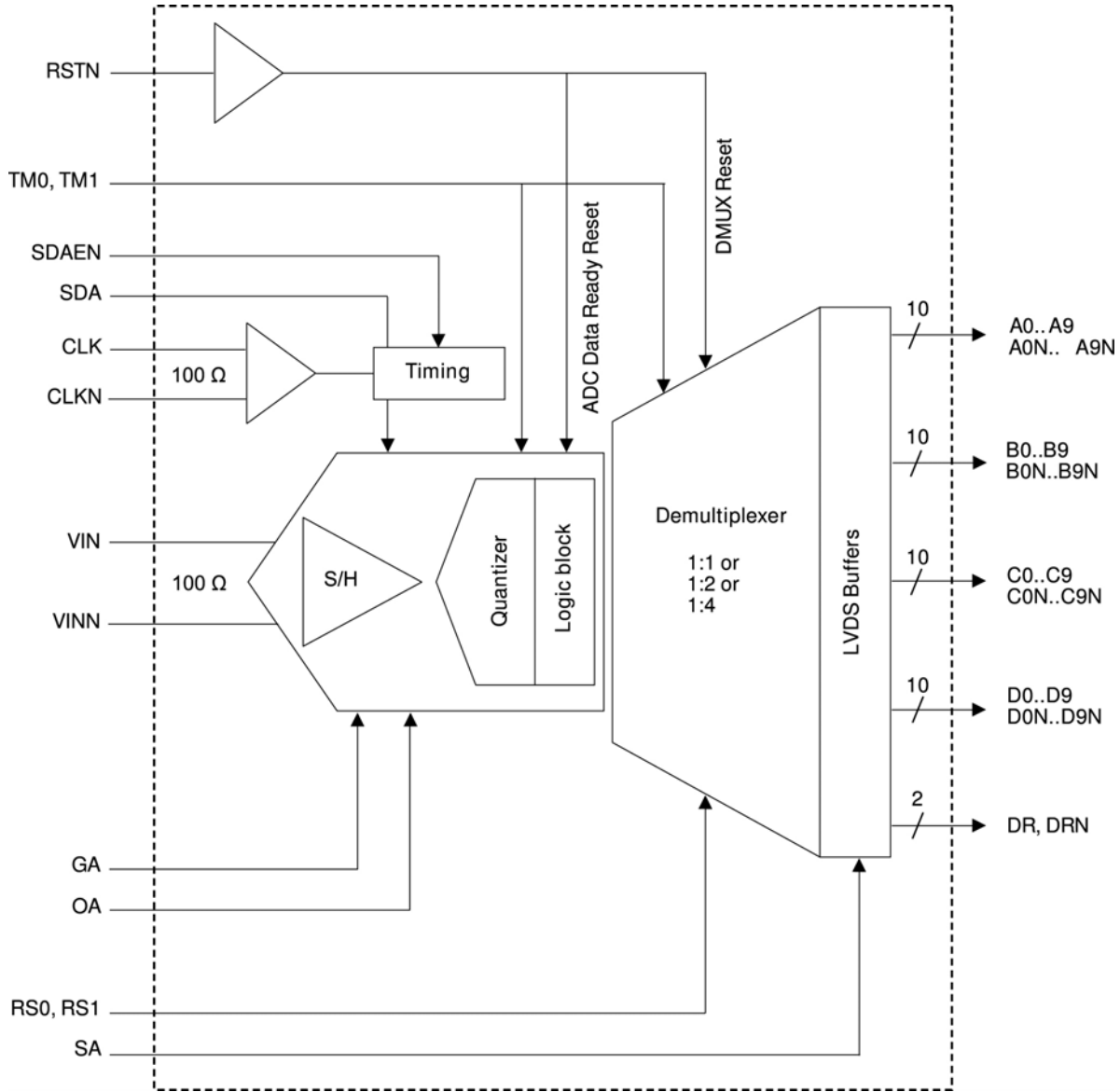
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- 10 Gbps Wireless Telecommunications
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# 1. General Description

## 1.1 Block Diagram

Figure 1-1. ADC with Integrated DEMUX Block Diagram



## 1.2 Description

The EV10AS180ZPY is a 10-bit 1.5 Gsps ADC. The device includes a front-end Track and Hold stage (T/H), followed by an analogue encoding stage (Analogue Quantizer) which outputs analogue residues resulting from analogue quantization. Successive banks of latches regenerate the analogue residues into logical levels before entering an error correction circuitry and a resynchronization stage followed by a DEMUX with 100 $\Omega$  differential output buffers.

### Main settings of the EV10AS180ZPY are as follows:

- It works in fully differential mode from analogue inputs up to digital outputs.
- It operates in the first Nyquist and L-Band (Fin ranging from DC to 1800 MHz).
- RS0 and RS1 pins allow to select the DEMUX Ratio (1:1 or 1:2 or 1:4).
- DEMUX outputs are synchronous on each port.
- A differential Data Ready output indicates when the outputs are valid. The Data Ready signal (DR, DRN) is common to the 4 ports.
- A power up reset ensures that the first digitized value corresponds to the first acquisition. An external Reset (RSTN) can also be used.
- The gain control pin, GA, and offset control, OA, are provided to adjust the ADC gain and offset transfer function.
- The SA pin is used to lower the swing of ADC output buffers.
- A Sampling Delay Adjust function (SDA) is provided to fine tune the ADC aperture delay, for applications requesting the interleaving of multiple ADCs for example.
- A diode monitors the junction temperature, with both the anode and the cathode being accessible.
- For debug and testability, the following functions are provided:
  - a static test mode, used to test either VOL or VOH at the ADC outputs (all bits at “0” level or “1” level respectively),
  - a dynamic Built-In Test, providing series of “1”s and “0”s in a checker board pattern fashion on all 4 ports.

## 2. Electrical Characteristics

### 2.1 Recommended Conditions of Use

**Table 2-1.** Recommended Conditions of Use

Parameter	Symbol	Comments	Typ.	Unit
Power supplies	$V_{CC5}$		5.2	V
	$V_{CC3}$		3.3	V
	$V_{CC0}$		2.5	V
Differential analogue input voltage (Full Scale)	$V_{IN} - V_{INN}$	100 $\Omega$ differential	500	mVpp
Clock input power level (Ground common mode)	$P_{CLK} - P_{CLKN}$	100 $\Omega$ differential input	4	dBm
Storage temperature	$T_{stg}$		-55 to 125	$^{\circ}$ C

### 2.2 Electrical Characteristics

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions.

**Table 2-2.** Electrical Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit
RESOLUTION		10			bit
ESD CLASSIFICATION		Class 1B			
<b>POWER REQUIREMENTS</b>					
Power Supply voltage					
- Analogue	$V_{CC5}$	5.0	5.2	5.5	V
- Analogue Core and Digital	$V_{CC3}$	3.15	3.3	3.45	V
- Output buffers	$V_{CC0}$	2.4	2.5	2.6	V
Power Supply current in 1:1 DEMUX Ratio					
- Analogue	$I_{V_{CC5}}$			85	mA
- Analogue Core and Digital	$I_{V_{CC3}}$			330	mA
- Output buffers	$I_{V_{CC0}}$			110	mA
Power Supply current in 1:2 DEMUX Ratio					
- Analogue	$I_{V_{CC5}}$			85	mA
- Analogue Core and Digital	$I_{V_{CC3}}$			335	mA
- Output buffers	$I_{V_{CC0}}$			160	mA
Power Supply current in 1:4 DEMUX Ratio					
- Analogue	$I_{V_{CC5}}$			85	mA
- Analogue Core and Digital	$I_{V_{CC3}}$			355	mA
- Output buffers	$I_{V_{CC0}}$			240	mA

Table 2-2. Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ.	Max	Unit
Power dissipation @ -12dBFS					
- 1:1 Ratio with standard LVDS output swing	PD		1.59		W
- 1:1 Ratio with 100mV LVDS output swing	PD		1.60		W
- 1:2 Ratio with standard LVDS output swing	PD		1.73		W
- 1:2 Ratio with 100mV LVDS output swing	PD		1.69		W
- 1:4 Ratio with standard LVDS output swing	PD		1.94		W
- 1:4 Ratio with 100mV LVDS output swing	PD		1.82		W
<b>LVDS Data and Data Ready Outputs</b>					
Logic compatibility		LVDS differential			
Output Common Mode <sup>(1)</sup>	V <sub>OCM</sub>	1.125	1.25	1.375	V
Differential output <sup>(1)(2)</sup>	V <sub>ODIFF</sub>	250	350	450	mV
Output level "High" <sup>(3)</sup>	V <sub>OH</sub>	1.25	-	-	V
Output level "Low" <sup>(3)</sup>	V <sub>OL</sub>	-	-	1.25	V
Output data format		Binary			
<b>ANALOGUE INPUT</b>					
Input type		AC coupled			
Analogue Input Common Mode (for DC coupled input)			3.1		V
Full scale input voltage range (differential mode)	V <sub>IN</sub> V <sub>INN</sub>	-125 -125		+125 +125	mV mV
Full scale analog input power level	P <sub>IN</sub>		-5		dBm
Analogue input capacitance (die only)	C <sub>IN</sub>		0.3		pF
Input leakage current (VIN = VINN = 0V)	I <sub>IN</sub>		50		μA
Analogue Input resistance (Differential)	R <sub>IN</sub>	96	100	104	Ω
<b>CLOCK INPUT (CLK, CLKN)</b>					
Input type		DC or AC coupled			
Clock Input Common Mode (for DC coupled clock)	V <sub>ICM</sub>		2		V
Clock Input power level (low phase noise sine wave input) 100Ω differential	P <sub>CLK</sub>	0	4	+10	dBm
Clock input swing (differential voltage) on each clock input	V <sub>CLK</sub> V <sub>CLKN</sub>	±447	±708	±1410	mV
Clock input capacitance (die only)	C <sub>CLK</sub>		0.3		pF
Clock Input resistance (Differential)	R <sub>CLK</sub>	94	98	102	Ω
<b>RSTN (active low)</b>					
Logic compatibility		2.5V CMOS compatible			
Input level "High"	V <sub>IH</sub>	2.0			V

**Table 2-2.** Electrical Characteristics (Continued)

Parameter	Symbol	Min	Typ.	Max	Unit
Input level "Low"	$V_{IL}$			0.4	V
<b>DIGITAL INPUTS (RS0, RS1, DECN, SDAEN, TM1, TM0)</b>					
Logic low Resistor to ground Voltage level Input current	$R_{IL}$ $V_{IL}$ $I_{IL}$	0 - -		10 0.5 450	$\Omega$ V $\mu A$
Logic high Resistor to ground Voltage level Input current	$R_{IH}$ $V_{IH}$ $I_{IH}$	10 k 2.0		infinite - 150	$\Omega$ V $\mu A$
<b>OFFSET, GAIN &amp; SAMPLING DELAY ADJUST SETTINGS (OA, GA, SDA)</b>					
Min voltage for minimum Gain, Offset or SDA	Analogue_min	$2 \times V_{cc3} / 3 - 0.5$			V
Max voltage for maximum Gain, Offset or SDA	Analogue_max			$2 \times V_{cc3} / 3 + 0.5$	V
Input current for min setting	$I_{min}$			200	$\mu A$
Input current for nominal setting	$I_{nom}$			50	$\mu A$
Input current for max setting	$I_{max}$			200	$\mu A$
<b>ANALOGUE SETTINGS (SA)</b>					
SA voltage for default swing value	Smax			$2 \times V_{cc3} / 3$	
SA voltage for minimum swing value	Smin	$2 \times V_{cc3} / 3 - 0.5$			
Input current (low, for default swing value)	$I_{min}$			50	$\mu A$
Input current (high) for min swing value	$I_{max}$			150	$\mu A$

- Notes:
1. Assuming 100 $\Omega$  termination ASIC load.
  2. VODIFF can be lobe lowered down to 100 mV with SA pin to reduce power consumption.
  3. VOH min and VOL max can never be 1.25V at the same time when VODIFF is min.

## 2.3 Converter Characteristics

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions.

**Table 2-3.** DC Converter Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Resolution		10			Bit
Missing codes	M <sub>CODES</sub>	None allowed			
<b>DC ACCURACY</b>					
Differential Non Linearity (for information only)	DNL+		0.5	1.0	LSB
Integral Non Linearity (for information only)	INL+		1.0	2.0	LSB
Integral Non Linearity	INL-		-1.0	-2.0	LSB
Gain central value <sup>(1)</sup>	ADC <sub>GAIN</sub>	0.9	1.0	1.1	
Gain error drift versus temperature (over 15 C°)				0.15	
ADC offset <sup>(2)</sup>	ADC <sub>OFFSET</sub>		±10		LSB

- Notes:
1. The ADC Gain center value can be tuned to 1.0 using the Gain adjust function.
  2. The ADC offset can be tuned to mid code 512 using the Offset adjust function.

## 2.4 Dynamic Performance

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions assuming an external clock jitter of 225 fs rms (which corresponds to the e2v testbench value). ADC internal clock jitter is 200 fs rms.

**Table 2-4.** Dynamic Performance

Parameter	Symbol	Min	Typ	Max	Unit
<b>AC Analogue Inputs</b>					
Full power Input Bandwidth	FPBW		2.2		GHz
Gain Flatness (from 10 to 750 MHz)			0.5		dB
Gain Flatness (from 750 to 1500 MHz)			1.2		dB
Gain Flatness (from 1500 to 1800 MHz)			1.0		dB
Deviation from linear phase (1 <sup>st</sup> Nyquist)			5		°
Deviation from linear phase (2 <sup>nd</sup> Nyquist)			1		°
Deviation from linear phase (L-band up to 2.25 GHz)			2		°
Input voltage standing Wave Ratio up to 1.8 GHz (unpowered device)	VSWR			1.2:1	
<b>AC Performance in 1<sup>st</sup> Nyquist</b>					
-12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max					
<b>Signal to Noise And Distortion Ratio</b> Fs = 1.5 Gsps Fin = 750 MHz	SINAD		53.0		dBFS
<b>Effective Number of Bits</b> Fs = 1.5 Gsps Fin = 750 MHz	ENOB		8.5		Bit FS
<b>Signal to Noise Ratio</b> Fs = 1.5 Gsps Fin = 750 MHz	SNR		55.0		dBFS
<b>Total Harmonic Distortion</b> (25 harmonics) Fs = 1.5 Gsps Fin = 750 MHz	THD		60		dBFS
<b>Spurious Free Dynamic Range</b> Fs = 1.5 Gsps Fin = 750 MHz	SFDR		62		dBFS
<b>Noise Power Ratio</b> Notch centered on 50 MHz, notch width 500 kHz on 20 MHz - 700 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR		45.0		dB
<b>Noise Power Ratio</b> Notch centered on 350 MHz, notch width 500 kHz on 20 MHz - 700 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR		45.0		dB
<b>Noise Power Ratio</b> Notch centered on 657 MHz, notch width 500 kHz on 20 MHz - 700 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR				dB

Table 2-4. Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
<b>IMD3 differential</b> ( $2F_{in1} - F_{in2}$ , $2F_{in2} - F_{in1}$ , unfilterable 3rd order Intermodulation products) At -7 dBFS $F_{in1} = 790$ MHz $F_{in2} = 800$ MHz	IMD		60		dBc
<b>AC Performance in 2<sup>nd</sup> Nyquist</b> -12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max					
<b>Noise Power Ratio</b> Notch centered on 800 MHz, notch width 500 kHz on 770 MHz - 1450 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR				dB
<b>Noise Power Ratio</b> Notch centered on 1100 MHz, notch width 500 kHz on 770 MHz - 1450 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR				dB
<b>Noise Power Ratio</b> Notch centered on 1407 MHz, notch width 500 kHz on 770 MHz - 1450 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR				dB
<b>AC Performance in LBAND</b> -12 dBFS differential input mode, 50% clock duty cycle, +4 dBm differential clock, external jitter = 225 fs rms max					
<b>Signal to Noise And Distortion Ratio</b> $F_s = 1.5$ Gsps $F_{in} = 1800$ MHz	SINAD		51.5		dBFS
<b>Effective Number of Bits</b> $F_s = 1.5$ Gsps $F_{in} = 1800$ MHz	ENOB		8.2		Bit FS
<b>Signal to Noise Ratio</b> $F_s = 1.5$ Gsps $F_{in} = 1800$ MHz	SNR		53.0		dBFS
<b>Total Harmonic Distortion</b> (25 harmonics) $F_s = 1.5$ Gsps $F_{in} = 1800$ MHz	THD		58		dBFS
<b>Spurious Free Dynamic Range</b> $F_s = 1.5$ Gsps $F_{in} = 1800$ MHz	SFDR		60		dBFS
<b>Noise Power Ratio</b> Notch centered on 1550 MHz, notch width 500 kHz on 1520 MHz - 2200 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR		43.0		dB
<b>Noise Power Ratio</b> Notch centered on 1850 MHz, notch width 500 kHz on 1520 MHz - 2200 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR				dB

**Table 2-4.** Dynamic Performance (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
<b>Noise Power Ratio</b> Notch centered on 2157 MHz, notch width 500 kHz on 1520 MHz - 2200 MHz band 1.5 Gsps at optimum loading factor of -13.1 dBFS	NPR				dB
<b>IMD3 differential</b> (2Fin1 – Fin2, 2Fin2 – Fin1, unfilterable 3rd order Intermodulation products) At -7 dBFS Fin1 = 1120 MHz Fin2 = 1130 MHz	IMD		59		dBc
<b>IMD3 differential</b> (2Fin1 – Fin2, 2Fin2 – Fin1, unfilterable 3rd order Intermodulation products) At -7 dBFS Fin1 = 1550 MHz Fin2 = 1560 MHz	IMD		58		dBc

## 2.5 Timing Characteristics and Switching Performances

Unless otherwise stated, requirements apply over the full operating temperature range (for performance) and at all power supply conditions.

**Table 2-5.** Timing Characteristics and Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit
<b>SWITCHING PERFORMANCE AND CHARACTERISTICS</b>					
Maximum clock frequency <sup>(1)</sup> 1:1 DEMUX Ratio 1:2 DEMUX Ratio 1:4 DEMUX Ratio		750 1500 1500			MHz
Minimum clock frequency <sup>(1)</sup>				1400	MHz
Maximum Output Rate per port (Data and Data Ready) 1:1 DEMUX Ratio 1:2 DEMUX Ratio 1:4 DEMUX Ratio		750 750 750			Msp/s
Maximum Output Frequency per port (Data and Data Ready) <sup>(2)</sup> 1:1 DEMUX Ratio 1:2 DEMUX Ratio 1:4 DEMUX Ratio		375 375 375			MHz
Analogue input frequency		DC		1800	MHz
BER@1.5 Gsps				10 <sup>-9</sup>	Error/ sample

**Table 2-5.** Timing Characteristics and Switching Performances (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
<b>TIMING</b>					
ADC settling time (VIN-VINN = 400 mVpp)	TS		770		ps
Overvoltage recovery time	ORT		0		ps
ADC step response (10% to 90%)			600		ps
Overshoot			0		%
Ringback			0		%
Clock duty cycle		40	50	60	%
Minimum clock pulse width (high)	TC1	0.25		0.375	ns
Minimum clock pulse width (low)	TC2	0.25		0.375	
Aperture delay <sup>(1)</sup>	TA		250		ps
Aperture delay adjustment	SDA	-42		+42	ps
Output rise/fall time for DATA (20% to 80%) <sup>(3)</sup>	TR/TF		400		ps
Output rise/fall time for DATA READY (20% to 80%) <sup>(2)</sup>	TR/TF		700		ps
Output Data to Data Ready propagation delay DMUX 1:1 @ 500 MSps sampling rate DMUX 1:2 @ 1.5 GSps sampling rate DMUX 1:4 @ 1.5 GSps sampling rate	TD1		1.44 1 1.5		ns ns ns
Data Ready to Output Data propagation delay DMUX 1:1 @ 500 MSps sampling rate DMUX 1:2 @ 1.5 GSps sampling rate DMUX 1:4 @ 1.5 GSps sampling rate	TD2		0.560 0.330 1.20		ns ns ns
Data output delay <sup>(4)</sup> DMUX 1:1 DMUX 1:2 and DMUX 1:4	TOD		3.5 6		ns
Data Ready output delay <sup>(4)</sup> DMUX 1:1 DMUX 1:2 and DMUX 1:4	TDR		4.5 6.8		ns
	ITOD - TDRI		1		ns

**Table 2-5.** Timing Characteristics and Switching Performances (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Output Data Pipeline delay					
1:1 DEMUX Ratio					
Port A			3.5		
1:2 DEMUX Ratio					
Port A			3.5		
Port B	TPD		2.5		Clock cycle
1:4 DEMUX Ratio					
Port A			5.5		
Port B			4.5		
Port C			3.5		
Port D			2.5		
Data Ready Pipeline delay					
1:1 DEMUX Ratio			4		Clock cycle
1:2 DEMUX Ratio	TPD		4.5		
1:4 DEMUX Ratio			7.5		
RSTN to DR, DRN	TRDR	10			ns
RSTN min pulse duration		4			ns

- Notes:
1. See Definition of Terms in [Section 3](#).
  2. Data Ready outputs are active on both rising and falling edges (DR/2 mode).
  3.  $L_{LOAD} = 5$  nH,  $C_{LOAD} = 5$  pF termination (for each single-ended outputLoad).
  4. TOD and TDR propagation times are defined at package input/outputs. They are given for reference only.
  5. Values for TD1 and TD2 are given for a 1.5 Gbps external clock frequency (50% duty cycle).  
For different sampling rates, apply the following formula:  
 $TD1 = T/2 + (TOD - TDR)$  and  
 $TD2 = T/2 + (TOD - TDR)$  where T = clock period.

This results in:

- placing the rising edge (True - False) of the differential Data Ready signal in the middle of the Output Data valid window.
- giving maximum setup and holding times for external data acquisition.

2.6 Timing Diagrams

Figure 2-1. Principle of Operation, DMUX 1:1

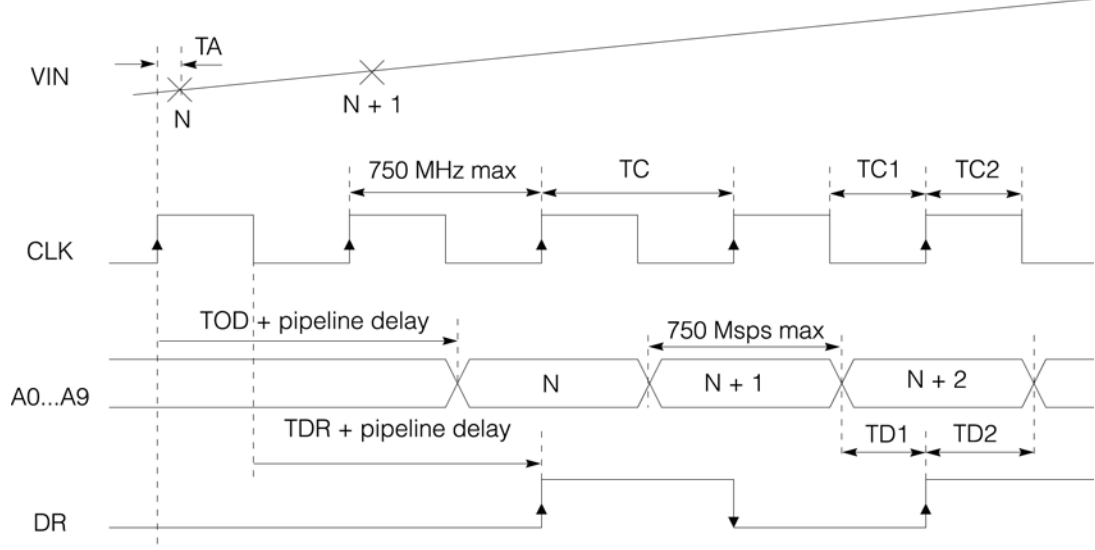


Figure 2-2. Principle of Operation, DMUX 1:2

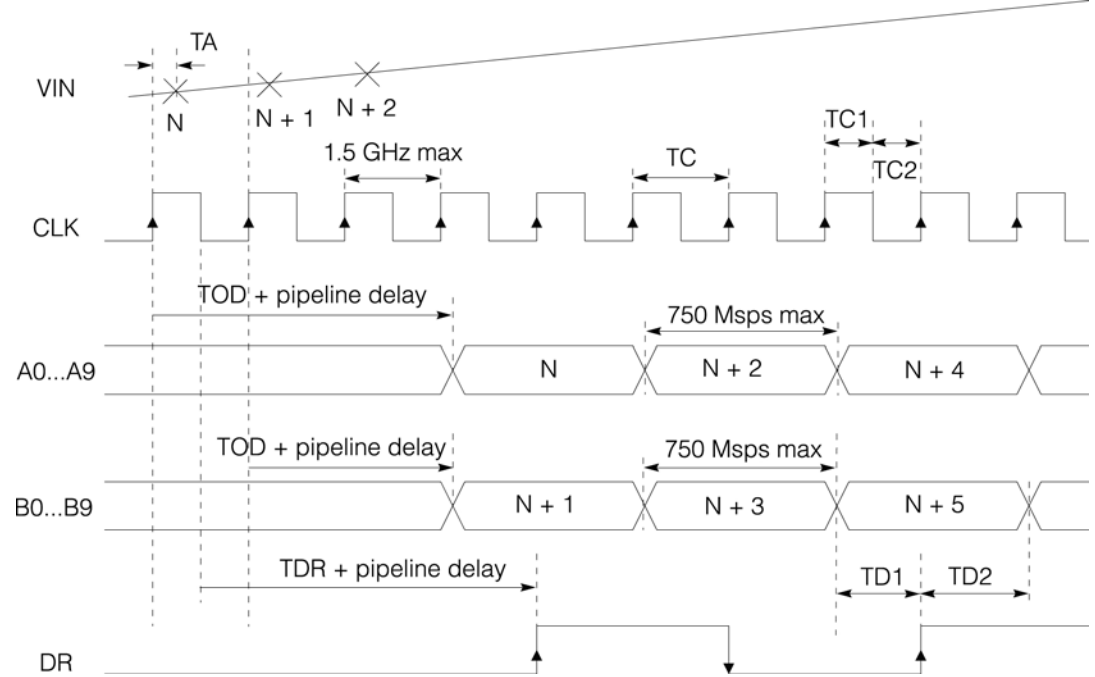
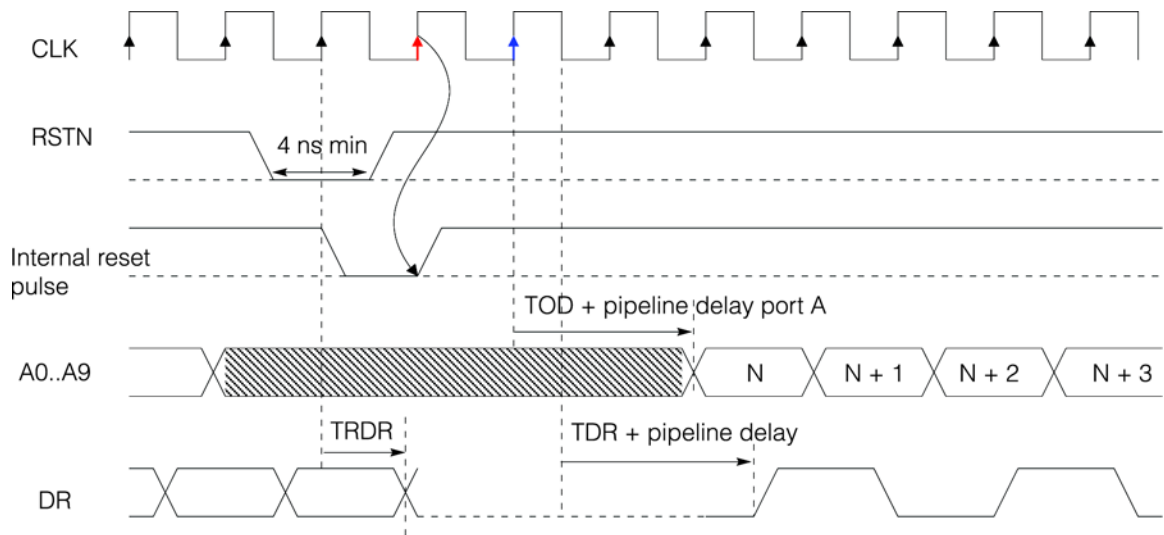




Figure 2-5. External Reset Timing Diagram (DMUX 1:1)



2.7 Coding

Table 2-6. ADC Coding Table

Differential analogue input	Voltage level	Digital output Binary MSB (bit 9).....LSB (bit 0)
> +250.25 mV	>Top end of full scale +½ LSB	1 1 1 1 1 1 1 1 1 1
+250.25 mV	Top end of full scale +½ LSB	1 1 1 1 1 1 1 1 1 1
+249.75 mV	Top end of full scale -½ LSB	1 1 1 1 1 1 1 1 1 0
+125.25 mV	<sup>3</sup> / <sub>4</sub> full scale +½ LSB	1 1 0 0 0 0 0 0 0 0
+124.75 mV	<sup>3</sup> / <sub>4</sub> full scale -½ LSB	1 0 1 1 1 1 1 1 1 1
+0.25 mV	Mid scale +½ LSB	1 0 0 0 0 0 0 0 0 0
-0.25 mV	Mid scale -½ LSB	0 1 1 1 1 1 1 1 1 1
-124.75 mV	<sup>1</sup> / <sub>4</sub> full scale +½ LSB	0 1 0 0 0 0 0 0 0 0
-124.25 mV	<sup>1</sup> / <sub>4</sub> full scale -½ LSB	0 0 1 1 1 1 1 1 1 1
-249.75 mV	Bottom end of full scale +½ LSB	0 0 0 0 0 0 0 0 0 1
-250.25 mV	Bottom end of full scale -½ LSB	0 0 0 0 0 0 0 0 0 0
< -250.25 mV	< Bottom end of full scale -½ LSB	0 0 0 0 0 0 0 0 0 0

### 3. Definition of Terms

**Table 3-1.** Definition of Terms

Abbreviation	Term	Definition
(Fs max)	Maximum Sampling Frequency	Sampling frequency for which ENOB < 6bits.
(Fs min)	Minimum Sampling frequency	Sampling frequency for which the ADC Gain has fallen by 0.5 dB with respect to the gain reference value. Performances are not guaranteed below this frequency.
(BER)	Bit Error Rate	Probability of exceeding a specified error threshold for a sample at maximum specified sampling rate. An error code is a code that differs by more than $\pm 4$ LSB from the correct code.
(FPBW)	Full power input bandwidth	Analogue input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale $-1$ dB ( $-1$ dBFS).
(SSBW)	Small Signal Input bandwidth	Analogue input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale $-10$ dB ( $-10$ dBFS).
(SINAD)	Signal to noise and distortion ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale ( $-1$ dBFS), to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	Signal to noise ratio	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale, to the RMS sum of all other spectral components excluding the twenty five first harmonics.
(THD)	Total harmonic distortion	Ratio expressed in dB of the RMS sum of the first twenty five harmonic components, to the RMS input signal amplitude, set at 1 dB below full scale. It may be reported in dB (i.e. related to converter $-1$ dB Full Scale), or in dBc (i.e. related to input signal level).
(SFDR)	Spurious free dynamic range	Ratio expressed in dB of the RMS signal amplitude, set at 1dB below Full Scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (i.e., related to converter $-1$ dB Full Scale), or in dBc (i.e. related to input signal level).
(ENOB)	Effective Number Of Bits	$\text{ENOB} = \frac{\text{SINAD} - 1.76 + 20 \log(A / \text{FS}/2)}{6.02}$ <p>Where A is the actual input amplitude and FS is the full scale range of the ADC under test.</p>
(DNL)	Differential non linearity	The Differential Non Linearity for an output code $i$ is the difference between the measured step size of code $i$ and the ideal LSB step size. DNL ( $i$ ) is expressed in LSBs. DNL is the maximum value of all DNL ( $i$ ). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	Integral non linearity	The Integral Non Linearity for an output code $i$ is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL ( $i$ ) is expressed in LSBs, and is the maximum value of all INL ( $i$ ).
(TA)	Aperture delay	Delay between the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point), and the time at which ( $V_{IN}$ , $V_{INN}$ ) is sampled.
(JITTER)	Aperture uncertainty	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	Settling time	Time delay to achieve 0.2% accuracy at the converter output when an 80% Full Scale step function is applied to the differential analogue input.
(ORT)	Overshoot recovery time	Time to recover 0.2% accuracy at the output, after a 150% full scale step applied on the input is reduced to midscale.
(TOD)	Digital data Output delay	Delay from the rising edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.

Table 3-1. Definition of Terms

Abbreviation	Term	Definition
(TDR)	Data ready output delay	Delay from the falling edge of the differential clock inputs (CLK, CLKN) (zero crossing point) to the next point of change in the differential output clock (zero crossing) with specified load.
(TD1)	Time delay from Data transition to Data Ready	General expression is $TD1 = TC1 + TDR - TOD$ with $TC = TC1 + TC2 = 1$ encoding clock period.
(TD2)	Time delay from Data Ready to Data	General expression is $TD2 = TC2 + TDR - TOD$ with $TC = TC1 + TC2 = 1$ encoding clock period.
(TC)	Encoding clock period	$TC1 =$ Minimum clock pulse width (high) $TC = TC1 + TC2$ . $TC2 =$ Minimum clock pulse width (low).
(TPD)	Pipeline Delay	Number of clock cycle between the sampling edge of an input signal and its associated output signal, regardless the TOD.
(TRDR)	Data Ready reset delay	Delay between the falling edge of RSTN and the reset to digital zero transition of the Data Ready output signal DR.
(TR)	Rise time	Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.
(TF)	Fall time	Time delay for the output DATA signals to fall from 20% to 80% of delta between low level and high level.
(PSRR)	Power supply rejection ratio	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	Non return to zero	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	InterModulation Distortion	The two tone intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products.
(NPR)	Noise Power Ratio	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When applying a notch-filtered broadband white-noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.
(VSWR)	Voltage Standing Wave Ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example a VSWR of 1.2 corresponds to a 20dB return loss (i.e. 99% power transmitted and 1% reflected).

4. Pin Description

Figure 4-1. Pin Mapping (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DGND	B4	B9	B9N	B8	B8N	NC DGND	DR	CBN	CB	C9N	C9	C4	DGND	A
B	NC DGND	NC DGND	B4N	B6	B5	B7	NC DGND	DRN	C7	C5	C6	C4N	NC DGND	NC DGND	B
C	B2N	NC DGND	NC DGND	B6N	B5N	B7N	DGND	DGND	C7N	C5N	C6N	NC DGND	NC DGND	C2N	C
D	B2	B3	B3N	DGND	DGND	VCC0	VCC0	VCC0	VCC0	DGND	DGND	C3N	C3	C2	D
E	B0N	B1	B1N	DGND	DGND	VCC0	VCC0	VCC0	VCC0	DGND	DGND	C1N	C1	C0N	E
F	B0	NC DGND	NC DGND	VCC0	VCC0	AGND	AGND	AGND	AGND	VCC0	VCC0	NC DGND	NC DGND	C0	F
G	A8	A8N	A9	A9N	DGND	AGND	AGND	AGND	AGND	DGND	D9N	D9	D8N	D8	G
H	A7	A7N	A4	A4N	DGND	AGND	AGND	AGND	AGND	DGND	D4N	D4	D7N	D7	H
J	A5N	A2	A2N	VCC3	VCC3	AGND	AGND	AGND	AGND	VCC3	VCC3	D2N	D2	D5N	J
K	A5	A0	A0N	DGND	DGND	AGND	VCC5	VCC5	AGND	DGND	DGND	D0N	D0	D5	K
L	A6N	A3	A3N	DGND	NC DGND	VCC5	VCC5	VCC5	VCC5	DGND	TMD	D3N	D3	D6N	L
M	A6	A1N	GA	OA	NC DGND	VCC5	VCC5	AGND	AGND	SDA	SDAEN	TM1	D1N	D6	M
N	A1	DIODEC	NC DGND	NC DGND	CLKN	AGND	AGND	AGND	AGND	AGND	AGND	SA	DECN	D1	N
P	DGND	DIODEA	RSTN	NC DGND	CLK	AGND	AGND	AGND	VIN	VINN	AGND	RSD	R81	DGND	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 4-1. Pin Description

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
<b>POWER SUPPLIES</b>				
V <sub>CC5</sub>	K7, K8, L6, L7, L8, L9, M6, M7	5.2V analogue supply (Front-end Track & Hold circuitry). Referenced to AGND.	N/A	
V <sub>CC3</sub>	J4, J5, J10, J11	3.3V power supply (ADC Core, Regeneration and Logic, DEMUX circuitry and Timing circuitry). Referenced to AGND.	N/A	
V <sub>CC0</sub>	D6, D7, D8, D9, E6, E7, E8, E9, F4, F5, F10, F11	2.5V digital power supply (output buffers). Referenced to DGND.	N/A	
AGND	F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9K6, K9, M8, M9, N6, N7, N8, N9, N10, N11, P6, P7, P8, P11	Analogue Ground. AGND plane should be separated from DGND on the board (the two planes can be connected by 0Ω resistors).	N/A	
DGND	A1, A14, C7, C8, D4, D5, D10, D11, E4, E5, E10, E11, G5, G10, H5, H10, K4, K5, K10, K11, L4, L10, P1, P14	Ground for output buffers. DGND plane should be separated from AGND on the board (the two planes can be connected by 0Ω resistors).	N/A	
<b>ANALOGUE INPUTS</b>				
VIN VINN	P9 P10	Analogue input (differential) with internal common mode at 3.1V.  It should be driven in AC coupling. Analogue input is sampled and converted (10-bit) on each positive transition of the CLK input.  Equivalent internal differential 100Ω input resistor.	I	

Table 4-1. Pin Description (Continued)

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
<b>CLOCK INPUTS</b>				
CLK CLKN	P5 N5	<p>Master sampling clock input (differential) with internal common mode at 2.65V.</p> <p>It should be driven in AC coupling.</p> <p>Equivalent internal differential 100Ω input resistor.</p>	I	
<b>RESET INPUT</b>				
RSTN	P3	<p>Reset input (single-ended).</p> <p>It is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented).</p> <p>This reset is Asynchronous, it is 2.5 V CMOS compatible. It is active low.</p> <p>Refer to <a href="#">Section 2.6</a> and <a href="#">Section 5.4</a></p>	I	<p>Input voltage command 0 – 2.5V CMOS compatible. If nothing is applied, IN = 2.5V.</p>

Table 4-1. Pin Description (Continued)

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
<b>DIGITAL OUTPUTS</b>				
A0, A0N A1, A1N A2, A2N A3, A3N A4, A4N A5, A5N A6, A6N A7, A7N A8, A8N A9, A9N	K2, K3 N1, M2 J2, J3 L2, L3 H3, H4 K1, J1 M1, L1 H1, H2 G1, G2 G3, G4	In-phase (Ai) and inverted phase (AiN) digital outputs on DEMUX Port A (with i = 0...9).  Differential LVDS signal.  A0 is the LSB, A9 is the MSB.  The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings).  Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 4-1. Pin Description (Continued)

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
B0, B0N B1, B1N B2, B2N B3, B3N B4, B4N B5, B5N B6, B6N B7, B7N B8, B8N B9, B9N	F1, E1 E2, E3 D1, C1 D2, D3 A2, B3 B5, C5 B4, C4 B6, C6 A5, A6 A3, A4	In-phase (Bi) and inverted phase (BiN) digital outputs on DEMUX Port B (with i = 0...9).  Differential LVDS signal.  B0 is the LSB, B9 is the MSB.  The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings).  Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	
C0, C0N C1, C1N C2, C2N C3, C3N C4, C4N C5, C5N C6, C6N C7, C7N C8, C8N C9, C9N	F14, E14 E13, E12 D14, C14 D13, D12 A13, B12 B10, C10 B11, C11 B9, C9 A10, A9 A12, A11	In-phase (Ci) and inverted phase (CiN) digital outputs on DEMUX Port C (with i = 0...9).  Differential LVDS signal.  C0 is the LSB, C9 is the MSB.  The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings).  Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	
D0, D0N D1, D1N D2, D2N D3, D3N D4, D4N D5, D5N D6, D6N D7, D7N D8, D8N D9, D9N	K13, K12 N14, M13 J13, J12 L13, L12 H12, H11 K14, J14 M14, L14 H14, H13 G14, G13 G12, G11	In-phase (Di) and inverted phase (DiN) digital outputs on DEMUX Port D (with i = 0...9).  Differential LVDS signal.  D0 is the LSB, D9 is the MSB.  The differential digital output data is transmitted at clock rate divided by the DMUX ratio (refer to RS0 and RS1 settings).  Each of these outputs should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.	O	

Table 4-1. Pin Description (Continued)

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
DR DRN	A8 B8	<p>In-phase (DR) and inverted phase (DRN) global data ready digital output clock.</p> <p>Differential LVDS signal.</p> <p>The differential digital output clock is used to latch the output data on rising and falling edge.</p> <p>The differential digital output clock rate is (CLK/2) divided by the DMUX ratio (provided by RS0 and RS1 pins).</p> <p>This differential digital output clock should be terminated by a 100Ω differential resistor placed as close as possible to the differential receiver.</p>	O	

Table 4-1. Pin Description (Continued)

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
<b>ADDITIONAL FUNCTIONS</b>				
DECN	N13	Decimation Function Enable (single-ended). Active low. Refer to <a href="#">Section 5.9</a> for more information.	I	
TM0, TM1	L11, M12	Test Mode. Refer to <a href="#">Section 5.3</a> for more information.	I	
RS0, RS1	P12, P13	DEMUX Ratio Selection. Refer to <a href="#">Section 5.2</a> for more information.	I	
SDAEN	M11	SDAEN = Sampling delay adjust enable. SDA = Sampling delay adjust. Please refer to <a href="#">Section 5.10</a> for more information.	I	

Driving by resistor: 10Ω or 10 kΩ.  
Driving by voltage: 0.5V or 2V.

Table 4-1. Pin Description (Continued)

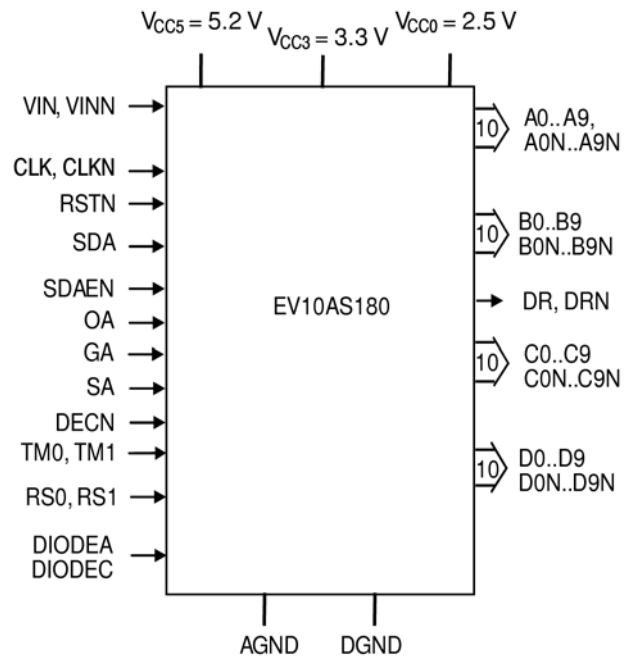
Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
SDA	M10	SDAEN = Sampling delay adjust enable. SDA = Sampling delay adjust. Please refer to <a href="#">Section 5.10</a> for more information.	I	<p>Variation on AP node: from <math>2 / (V_{CC3} / 3) - 0.5V</math> to <math>2 / (V_{CC3} / 3) - 0.5V</math>.</p>

Table 4-1. Pin Description (Continued)

Signal Name	Pin Number	Description	Direction	Equivalent Simplified Schematics
GA	M3	Gain Adjust. Refer to <a href="#">Section 5.6</a> for more information.	I	<p>Variation on AP node: from <math>2 / (V_{CC3} / 3) - 0.5V</math> to <math>2 / (V_{CC3} / 3) - 0.5V</math>.</p>
OA	M4	Offset Adjust. Refer to <a href="#">Section 5.7</a> for more information.	I	
SA	N12	Swing adjust. Refer to <a href="#">Section 5.8</a> for more information.	I	
DIODEA	P2	Die Junction temperature monitoring (DIODEA = anode, DIODEC = cathode). Please refer to <a href="#">Section 5.11</a> for more information.	I	
DIODEC	N2		O	
NC	A7 B1, B2, B7, B13, B14 C2, C3, C12, C13 F2, F3, F12, F13 N3, N4, P4, L5, M5	Not connected pins, connect to ground (DGND).	N/A	

## 5. Functional Description

Name	Function
V <sub>CC5</sub>	5.2V Power supply
V <sub>CC3</sub>	3.3V Power supply
V <sub>CC0</sub>	2.5V Power supply
AGND	Analogue Ground
DGND	Digital Ground
VIN,VINN	Differential Analogue Input
CLK,CLKN	Differential Clock Input
[A0:A9] [A0N:A9N]	Differential Output Data on port A
[B0:B9] [B0N:B9N]	Differential Output Data on port B
[C0:C9] [C0N:C9N]	Differential Output Data on port C
[D0:D9] [D0N:D9N]	Differential Output Data on port D
DR, DRN	Global Differential Data Ready
SA	Analogue tuning to adjust output swing
RS0, RS1	DEMUX Ratio select
RSTN	External reset
TM0, TM1	Test Mode pins
SDA	Sampling Delay Adjust input
SDAEN	Sampling Delay Adjust Enable
GA	Gain Adjust input
OA	Offset adjust input
DECN	Decimation function enable
DIODEA, DIODEC	Diode for die junction temperature monitoring



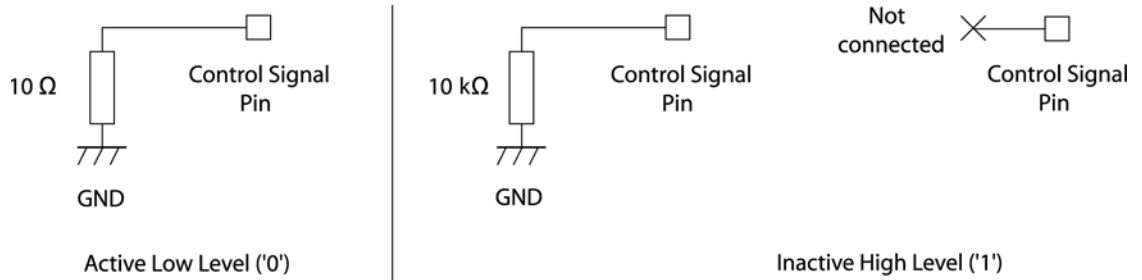
## 5.1 Control Signal Settings

The RS0, RS1, TM0, TM1, SDAEN and DECN control signals use the same static input buffer.

Logic “1” (10 kΩ to Ground, or tied to V<sub>CC3</sub> = 3.3V, or left floating) was chosen for the default modes:

- 1:2 DMUX (RS1 = RS0 = “1”), please refer to [Section 5.2](#) for more information,
- Test Mode off (TM0 = TM1 = “1”), please refer to [Section 5.3](#) for more information,
- Decimation Off (please refer to [Section 5.9](#) for more information),
- SDA off (please refer to [Section 5.10](#) for more information).

**Figure 5-1.** Mode Settings - Summary



**Table 5-1.** ADC Mode Settings - Summary

Function	Logic Level	Electrical Level	Description
SDAEN	0	10Ω to ground	Sampling delay adjust enabled
	1	10 kΩ to ground or V <sub>CC3</sub>	Sampling delay adjust disabled
		N/C	
DECN	0	10Ω to ground	Decimation by 8
	1	10 kΩ to ground or V <sub>CC3</sub>	Normal conversion (no decimation)
		N/C	
RS<1:0>	01	RS1: 10Ω to ground RS0: 10 kΩ to ground or NC or V <sub>CC3</sub>	1:1 DEMUX Ratio (Port A)
	11	RS1: 10 kΩ to ground or NC or V <sub>CC3</sub> RS0: 10 kΩ to ground or NC or V <sub>CC3</sub>	1:2 DEMUX Ratio (Ports A and B)
	10	RS1: 10 kΩ to ground or NC or V <sub>CC3</sub> RS0: 10Ω to ground	1:4 DEMUX Ratio (Ports A, B C and D)
	00	RS1: 10Ω to ground RS0: 10Ω to ground	Not used

**Table 5-1.** ADC Mode Settings - Summary (Continued)

Function	Logic Level	Electrical Level	Description
TM<1:0>	01	TM1: 10Ω to ground TM 0: 10 kΩ to ground or NC or V <sub>CC3</sub>	Static Test (all "0"s at the output for VOL test)
	11	TM 1: 10 kΩ to ground or NC or V <sub>CC3</sub> TM 0: 10 kΩ to ground or NC or V <sub>CC3</sub>	Normal conversion mode (default mode)
	10	TM 1: 10 kΩ to ground or NC or V <sub>CC3</sub> TM 0: 10Ω to ground	Static Test (all "1"s at the output for VOH test)
	00	TM1: 10Ω to ground TM0: 10Ω to ground	Dynamic test (checker board pattern = all bits toggling from "0" to "1" or "1" to "0" every cycle with 10101010 or 01010101 patterns)

## 5.2 DEMUX Ratio Select (RS0, RS1) Function

Configure pins RS0 and RS1 as described in the table below to select one of the three DEMUX ratio values.

**Table 5-2.** Ratio Select Coding

RS<1:0>	01	1:1 DEMUX Ratio (Port A)
	11	1:2 DEMUX Ratio (Ports A and B)
	10	1:4 DEMUX Ratio (Ports A, B, C and D)
	00	Not used

ADC in 1:1 Ratio

Input Words:

1, 2, 3, 4, 5, 6, 7, 8...

1:1 →

Output Words:

Port A	1 2 3 ...
Port B	Not used
Port C	Not used
Port D	Not used

ADC in 1:2 Ratio

Input Words:

1, 2, 3, 4, 5, 6, 7, 8...

1:2 →

Output Words:

Port A	1 3 5 ...
Port B	2 4
Port C	Not used
Port D	Not used

ADC in 1:4 Ratio

Input Words:

1, 2, 3, 4, 5, 6, 7, 8...

1:4 →

Output Words:

Port A	1 5 9...
Port B	2 6
Port C	3 7
Port D	4 8

- The values of each port display simultaneously.
- Any used port should be terminated by a 100Ω differential resistor. Refer to [Section 5.15](#) for more information.
- Any unused port can be left open (no external termination required).

### 5.3 Test Mode (TM0, TM1) Function

Two test modes are made available in order to test the 10-bit digital outputs of the ADC:

- a static test mode, where one can choose to output only “1”s or only “0”s,
- a dynamic test mode, where all bits toggle from “1” to “0” or from “0” to “1” every cycle, used to test the output transitions.

The Test Mode coding is described in the tables below.

**Table 5-3.** Ratio Select Coding

TM<1:0>	01	Static Test (all “0”s at the 10-bit output for VOL test)
	11	Normal conversion mode (default mode)
	10	Static Test (all “1”s at the 10-bit output for VOH test)
	00	Dynamic test (checker board pattern = all 10 bits toggling from “0” to “1” or “1” to “0” every cycle with 1010101010 or 0101010101 patterns)

Note: The sequence should start on port A, whatever the DEMUX mode is.

**Table 5-4.** Test Mode (TBC)

Cycle	DR	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0
N		0	1	0	1	0	1	0	1	0	1
N+1		1	0	1	0	1	0	1	0	1	0
N+2		0	1	0	1	0	1	0	1	0	1
N+3		1	0	1	0	1	0	1	0	1	0
N+4		0	1	0	1	0	1	0	1	0	1

### 5.4 External Reset (RSTN)

An external reset (RSTN) is available in case it is necessary to reset the ADC during operation (it is not mandatory to perform an external reset on the ADC for proper operation of the ADC as a power up reset is already implemented). This reset is 2.5V CMOS compatible. It is active low.

### 5.5 Power Up Reset

A power up reset has been integrated in the ADC. It is generated internally by the digital section of the ADC (on  $V_{CC3}$  power supply) and is de-activated when  $V_{CC5}$  reaches 80% of its steady state value. It is important that  $V_{CC3}$  is switched on first in order to properly start the ADC.  $V_{CC5}$  and  $V_{CC5}$  can be switched on after  $V_{CC3}$  in any order ( $V_{CC5}$  then  $V_{CC0}$  or  $V_{CC0}$  then  $V_{CC5}$ ).

Please refer to [Section 2.6](#), [Figure 2-4](#) for more information.

## 5.6 Gain Adjust (GA) Function

This function is used to adjust the ADC Gain so that it can always be tuned to 1.0.

The ADC Gain can be tuned by  $\pm 10\%$  by setting the voltage applied on GA by  $\pm 0.5V$  around  $2 \times V_{CC3} / 3$ .

## 5.7 Offset Adjust (OA) Function

This function is used to adjust the ADC Offset so that it can always be tuned to mid-code 512.

The ADC Offset can be tuned by  $\pm 40$  LSB ( $\pm 20$  mV) by tuning the voltage applied on OA by  $\pm 0.5V$  around  $2 \times V_{CC3} / 3$ .

## 5.8 Swing Adjust (SA) Function

This function is used to reduce the nominal swing of the ADC in order to reduce power consumption in digital output buffers.

The nominal LVDS swing (250 to 450 mV) can be lowered (continuous tuning) to at least 100 mV by reducing the voltage applied on SA by  $-0.5V$  from the middle value  $2 \times V_{CC3} / 3$  (When SA is set at  $2 \times V_{CC3} / 3$ , the swing is a standard LVDS swing around 300 mV, when SA is set to  $2 \times V_{CC3} / 3 - 0.5$ , then swing is reduced to about 100 mV).

## 5.9 Decimation (DECN) Function

The decimation function allows:

- a quick check of the ADC during the debugging phase of the product running at its max speed.
- to reduce the speed of the output signals while using the max clock frequency value, i.e. 1.5 Gsps.

When active, this function makes the ADC output only 1 out of 8 data, thus resulting in a data rate which is 8 times slower than the clock rate. In addition, DEMUX Ratio can be chosen in order to divide the data rate by 16 (1:2 mode) or by 32 (1:4 mode).

Note: The ADC Decimation Test mode is different from the Test Mode function, which can be used to check the ADC outputs

DECN is active at low level.

To deactivate the decimation mode, connect DECN to a high level by connecting it to  $V_{CC3}$  or by leaving DECN pin floating.

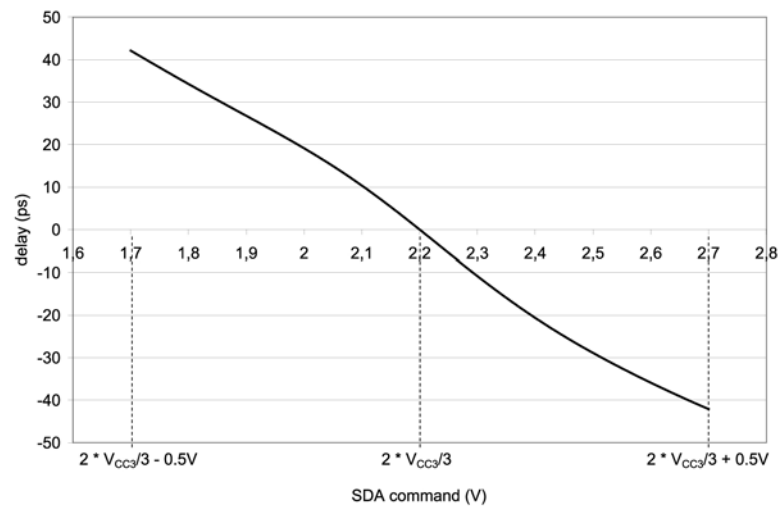
## 5.10 Sampling Delay Adjust (SDA) Function

Sampling delay adjust (SDA pin) is used to fine tune the sampling ADC aperture delay TA around its nominal value. This functionality is enabled using the SDAEN signal, which is active at low level (when tied to ground) and inactive at high level (10 k $\Omega$  to Ground, or tied to  $V_{CC3} = 3.3V$ , or left floating).

This feature is relevant for interleaving ADCs to increase sampling rate.

The variation of the delay around its nominal value as a function of the SDA voltage is shown in the following graph (simulation result):

**Figure 5-2.** Typical Tuning Range is  $\pm 40$  ps for Applied Control Voltage Varying Between  $\pm 0.5V$  around  $2 \times V_{CC3} / 3$  on SDA Pin



The variation of the delay in function of the temperature is negligible.

### 5.11 Temperature DIODE Function

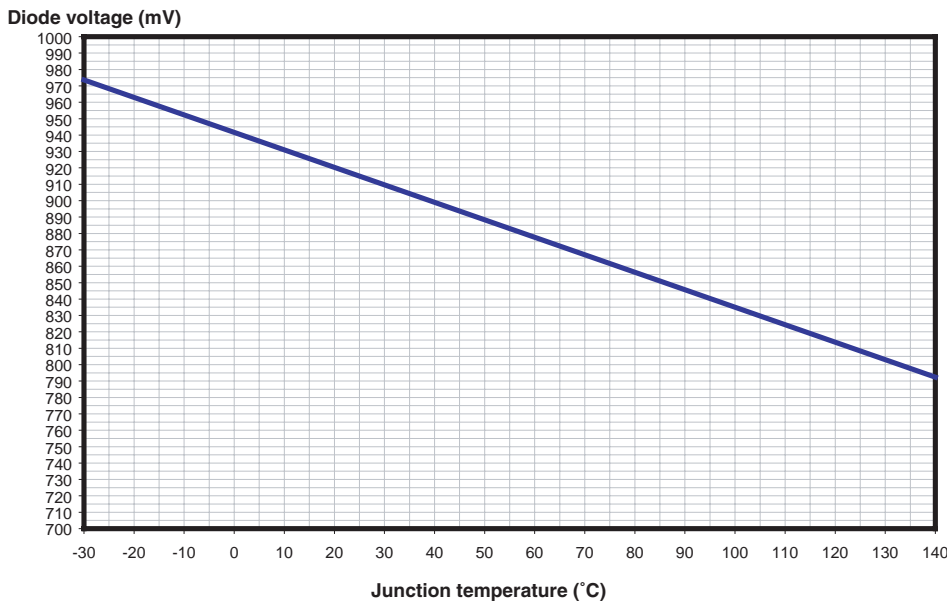
A diode for die junction temperature monitoring is available in this ADC. It is constituted by an ESD diode. Both Anode and cathode of the diode are accessible externally.

In order to monitor the die junction temperature of the ADC, a current of 1 mA has to be applied on the DIODEA pin (anode of the diode). The voltage across the DIODEA pin and the DIODEC pin provides the junction temperature of the die thanks to the intrinsic diode characteristics provided in [Figure 5-3](#).

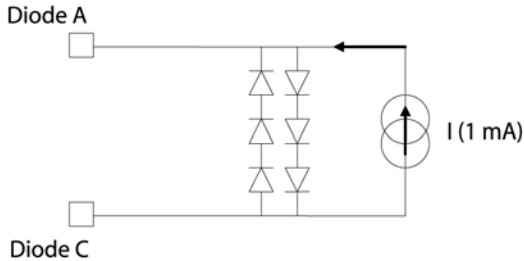
The use of three protection diodes is recommended to avoid any damage to the internal diode due to over-voltages. The recommended implementation is provided in [Figure 5-4](#).

**Figure 5-3.** Temperature DIODE Characteristics

Junction Temperature versus Diode voltage for I = 1mA



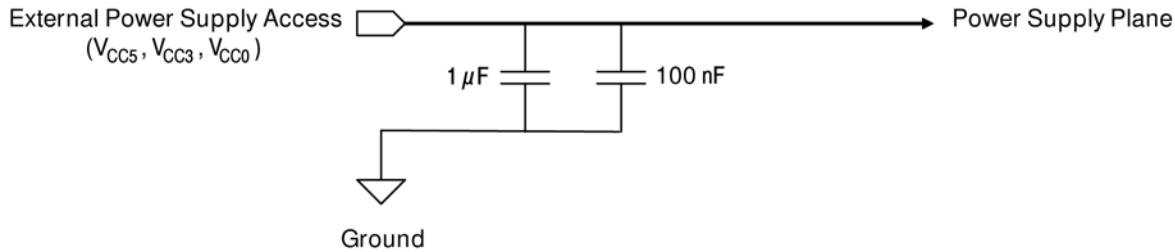
**Figure 5-4.** Temperature DIODE Implementation



5.12 Bypassing, Decoupling and Grounding

All power supplies have to be decoupled to ground as close as possible to the signal accesses to the board by 1 μF in parallel to 100 nF.

Figure 5-5. EV10AS180ZPY Power Supplies Decoupling and Grounding Scheme

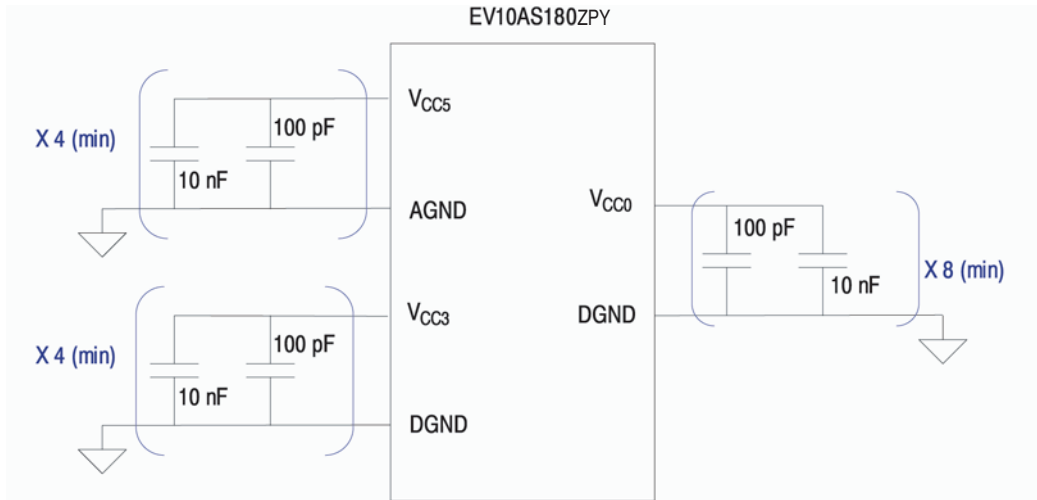


Each group of neighboring power supply pins attributed to the same value should be bypassed with at least one pair of 100 pF in parallel to 10 nF capacitors. These capacitors should be placed as close as possible to the power supply package pins.

The minimum required number of pairs of capacitors by power supply type is:

- 4 for  $V_{CC5}$
- 4 for  $V_{CC3}$
- 8 for  $V_{CC0}$

Figure 5-6. EV10AS180ZPY Power Supplies Bypassing Scheme



Each power supply has to be bypassed as close as possible to its source or access by 100 nF in parallel to 1 μF capacitors.

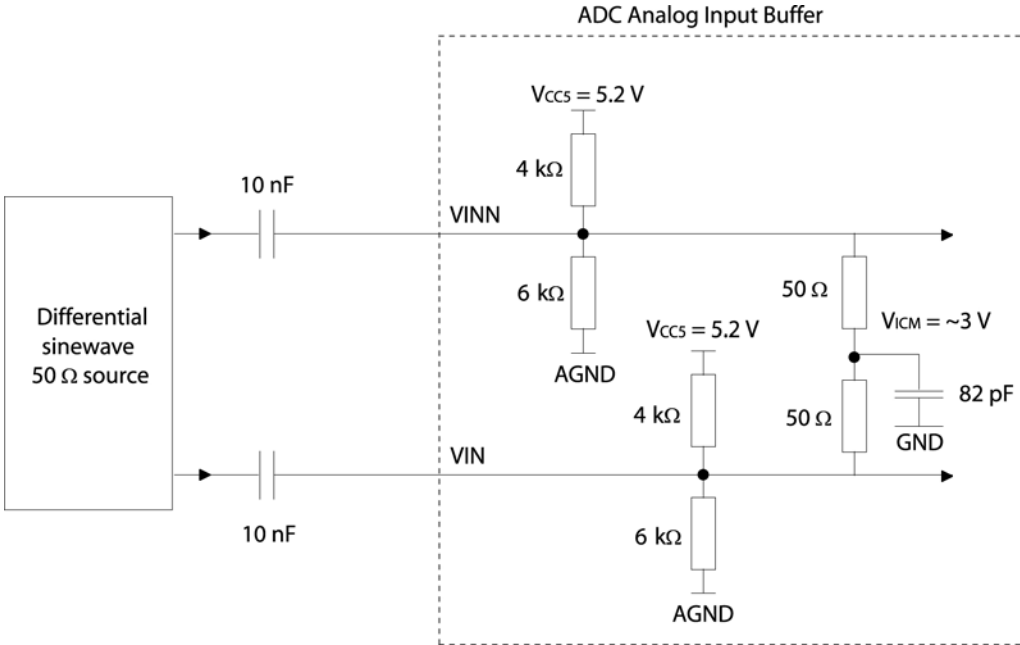
5.13 Analogue Inputs (VIN/VINN)

The analogue input should be used in differential mode. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

5.13.1 Differential Analogue Input

The analogue input should be AC coupled as described in Figure 5-7.

Figure 5-7. Differential Analogue Input Implementation (AC Coupled)

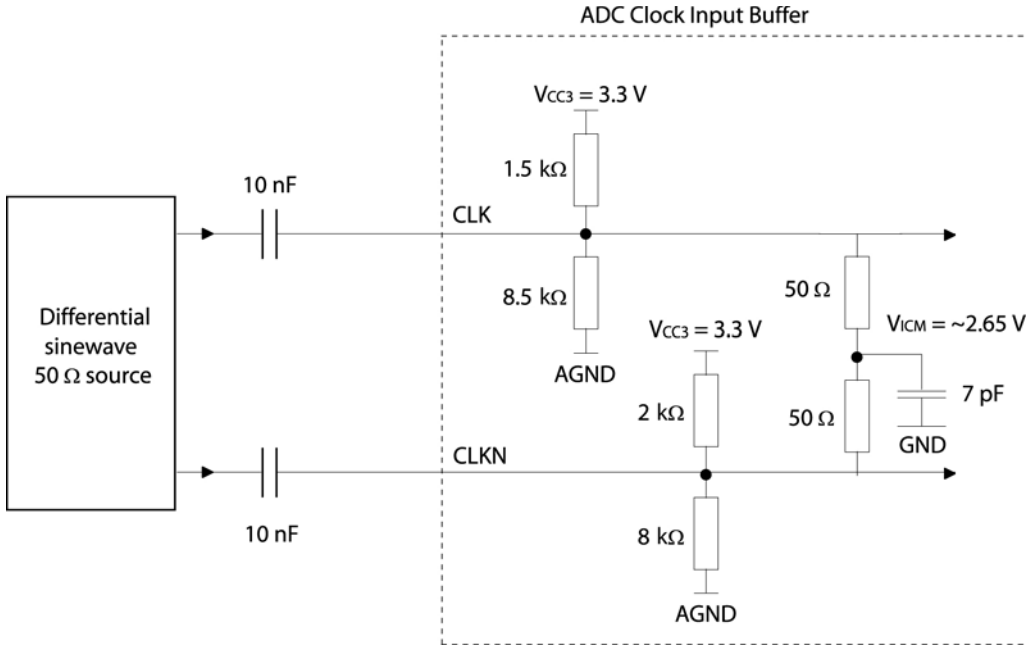


5.14 Clock Inputs (CLK/CLKN)

Differential mode is the recommended input scheme. Single-ended clock input is not recommended due to performance limitations. If a single-ended source is used, then a balun (transformer) should be implemented to convert the signal to a differential signal at the input of the ADC.

Since the clock input common mode is 2.65V, we recommend to AC couple the input clock as described in Figure 5-8.

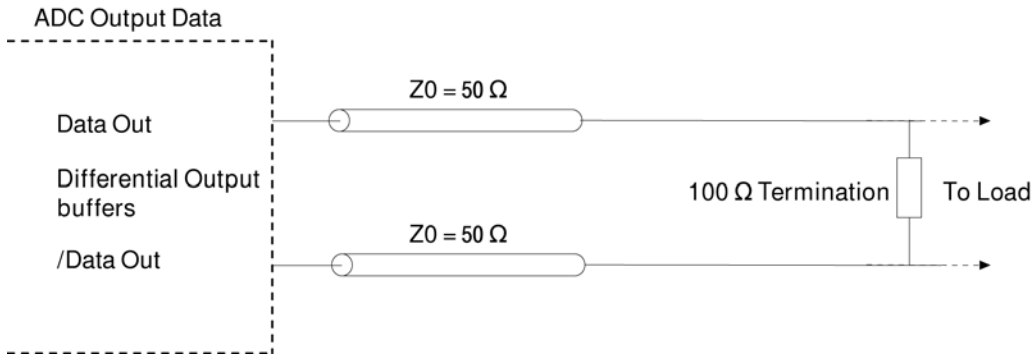
**Figure 5-8.** Differential Clock Input Implementation (AC Coupled)



**5.15 Digital Outputs**

The digital outputs are LVDS compatible. They have to be 100Ω differentially terminated.

**Figure 5-9.** Differential Digital Outputs Terminations (100Ω LVDS)



If the ADC is used in 1:1 or 1:2 DMUX modes, the unused ports can be left open (no external termination required).

### 6. Board Layout Recommendations

Assumptions:

- RO4003 for the top and bottom layers, FR4 HTG for the internal layers
- Dielectric thickness: 200 μm
- Dielectric constant: 3.38
- Lands diameter: 750 μm
- GND Via/Land Diameter: 200 μm

#### 6.1 Clock Input & Analogue Input

It is necessary to have 50Ω lines on the board.

The high speed differential input signals (analogue input, clock input), should be routed in parallel with a 400 μm width and a pitch of 1.27 mm (obtained by calculation on LINPAR software).

Max difference between CLK and CLKN or VIN and VINN = ±0.1mm.

In addition, the lines for VIN, VINN and CLK, CLKN should be matched to one another within ±1mm.

A clearance in the ground plane below the CLK, CLKN and VIN, VINN package lands is necessary in order to reduce impedance mismatch between board and package. It is illustrated in Figure 6-2.

Figure 6-1. Recommended Routing on RO4003 for the Clock and Analogue Input

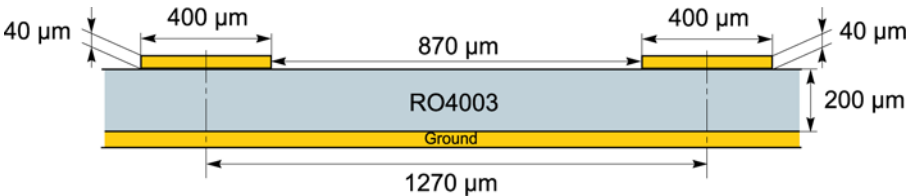
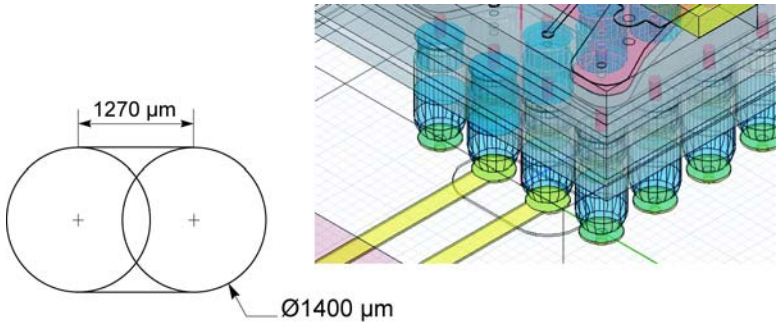


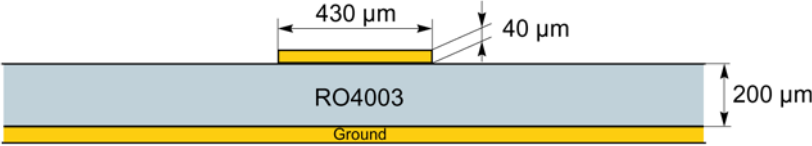
Figure 6-2. Recommended Clearance under CLK, CLKN, and VIN, VINN on the Ground Plane



6.2 RSTN

The RSTN signal is a single-ended signal with 50Ω impedance.

Figure 6-3. Recommended Routing on RO4003 for RSTN Signal



6.3 Digital Output Data

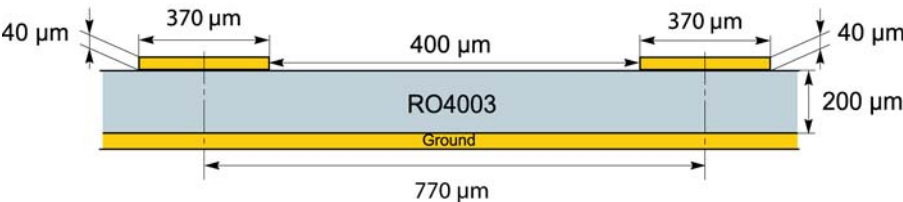
The high speed differential output signals (digital output, clock output), should be routed in parallel with 50Ω impedance, 370 μm width and a pitch of 0.77 mm (obtained by calculation on LINPAR software).

Max difference between any two signals = ±1.5 mm.

Max difference between longest and shortest data per port = ±1 mm

Max difference between two signals of the same differential pair (Xi, XiN) = ±0.5 mm (where X = A, B, C or D, i = 0...9).

Figure 6-4. Recommended Routing on RO4003 for Digital Output Data Signals



## 6.4 Package Internal Skew

**Table 6-1.** Skew Data-OUT

Data Name	Data Name	Top Trace Length mm	Bottom Trace Length mm	Wire Length mm	Total Length mm	Referenced Length mm	Required Correction ps
A0	D0	1,86	0,45	2,26	4,57	1,34	9
A0N	D0N	0,87	0,45	2,26	3,58	0,35	2
A1	D1	4,73	0,45	2,28	7,46	4,23	28
A1N	D1N	4,00	0,45	2,29	6,74	3,51	24
A2	D2	1,75	0,45	2,28	4,49	1,26	8
A2N	D2N	0,60	0,45	2,28	3,34	0,11	1
A3	D3	2,32	0,45	2,26	5,03	1,80	12
A3N	D3N	1,54	0,45	2,27	4,25	1,02	7
A4	D4	0,57	0,45	2,28	3,30	0,07	0
A4N	D4N	0,91	0,45	2,28	3,64	0,41	3
A5	D5	3,44	0,45	2,29	6,17	2,94	20
A5N	D5N	2,86	0,45	2,29	5,60	2,37	16
A6	D6	4,96	0,45	2,28	7,69	4,46	30
A6N	D6N	4,26	0,45	2,28	6,99	3,76	25
A7	D7	2,52	0,45	2,29	5,25	2,02	14
A7N	D7N	1,61	0,45	2,29	4,34	1,11	7
A8	D8	2,53	0,45	2,29	5,27	2,04	14
A8N	D8N	1,52	0,45	2,29	4,26	1,03	7
A9	D9	0,50	0,45	2,29	3,23	0,00	0
A9N	D9N	0,67	0,46	2,29	3,42	0,19	1

B0	C0	2,82	0,45	2,26	5,53	2,30	15
B0N	C0N	2,84	0,45	2,26	5,55	2,32	16
B1	C1	1,83	0,45	2,28	4,56	1,33	9
B1N	C1N	0,76	0,45	2,27	3,49	0,26	2
B2	C2	3,20	0,45	2,29	5,94	2,71	18
B2N	C2N	3,38	0,45	2,30	6,12	2,89	19
B3	C3	2,01	0,45	2,20	4,67	1,44	10
B3N	C3N	1,18	0,45	2,20	3,83	0,60	4
B4	C4	4,88	0,45	2,24	7,57	4,34	29
B4N	C4N	3,72	0,45	2,23	6,40	3,17	21
B5	C5	1,86	0,45	2,27	4,57	1,34	9

Table 6-1. Skew Data-OUT

B5N	C5N	0,87	0,55	2,27	3,69	0,46	3
B6	C6	2,13	0,45	2,23	4,81	1,58	11
B6N	C6N	1,19	0,45	2,23	3,87	0,64	4
B7	C7	1,70	0,45	2,27	4,42	1,19	8
B7N	C7N	0,67	0,49	2,27	3,43	0,20	1
B8	C8	3,36	0,45	2,28	6,09	2,86	19
B8N	C8N	2,68	0,45	2,28	5,42	2,19	15
B9	C9	4,36	0,45	2,27	7,08	3,85	26
B9N	C9N	3,63	0,45	2,27	6,35	3,12	21
-	DR	2,53	0,45	2,29	5,26	2,03	14
-	DRN	1,57	0,45	2,29	4,30	1,07	7

Data name	top trace length mm	bottom trace length mm	wire length mm	total length mm
-----------	---------------------	------------------------	----------------	-----------------

VIN	2,324	0,45	2,312	5,09
VINN	2,324	0,45	2,318	5,09

RSTN	3,185	0,45	2,253	5,89
-	2,339	0,45	2,251	5,04

CLK	2,666	0,45	2,262	5,38
CLKN	1,828	0,45	2,262	4,54

-	3,348	0,45	2,224	6,02
-	3,608	0,45	2,227	6,29

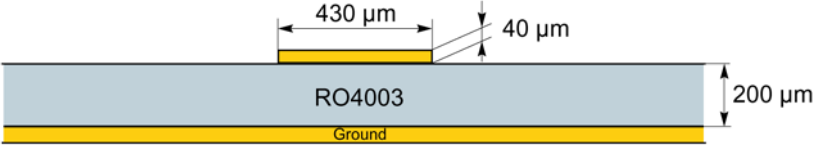
-	2,905	0,45	2,258	5,61
-	2,054	0,45	2,260	4,76

- Notes:
1. Take 6.7 ps/mm ( $E_r = 4.1$ )
  2. Referenced length = total length - shortest length (3.23)
  3. Required correction = referenced length \* 6.7 ps/mm
  4. A6 has the longest trace and A9 has the shortest trace (reference).
  5. Port D and C are deduced from ports A and B respectively (symmetry).

6.5 SA, RSx, TMx, SDA, SDAEN, GA, OA, DECN and Diode

These are “static” signals to be routed in single-ended 50Ω impedance.

Figure 6-5. Recommended Routing on RO4003 for Static Signal

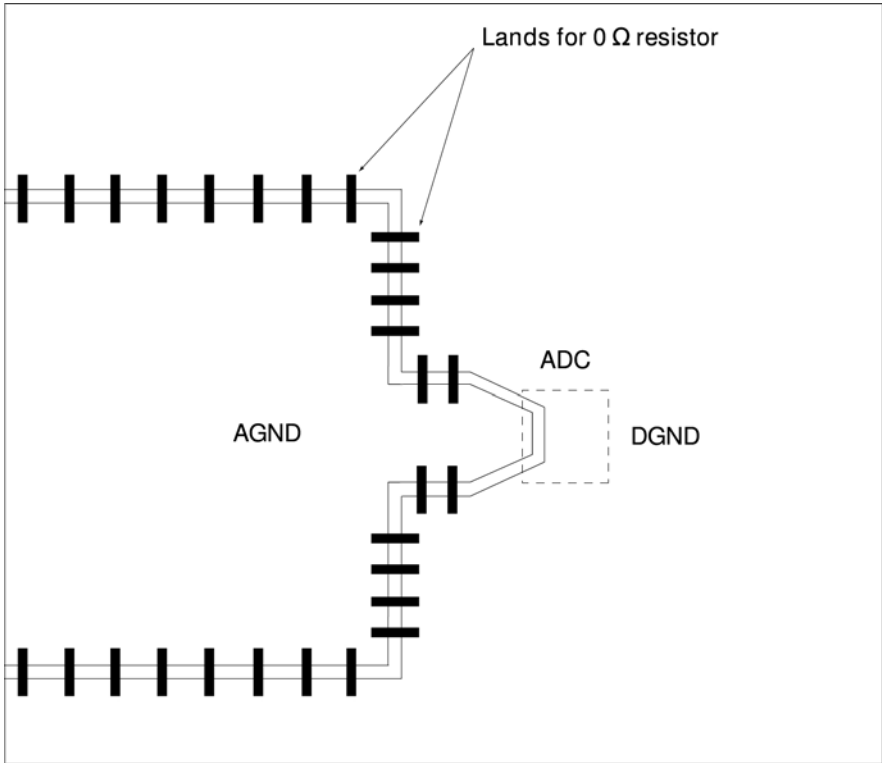


6.6 Ground Layers

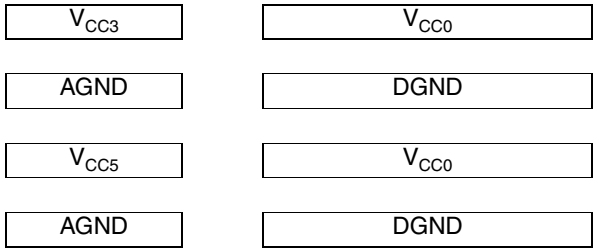
It is recommended to have 2 planes for the AGND and the DGND on the PCB. These planes can be reunited via 0Ω resistors (16 locations for 0Ω resistors are planned in the EV10AS180ZPY-EB evaluation board). Only the input clock and analogue input are referenced to AGND, the other parts of the ADC are referenced to DGND.

Important note: AGND and V<sub>CC0</sub> should not be superimposed in order to avoid coupling effects. V<sub>CC3</sub> and V<sub>CC5</sub> are referenced to AGND while V<sub>CC0</sub> is referenced to DGND.

Figure 6-6. AGND and DGND Plane (Bottom Layer)



**Figure 6-7.** AGND, DGND and Power Plane Stacking



## 7. Thermal Characteristics

### 7.1 Thermal characteristics fpBGA196

#### 7.1.1 Thermal resistance

Assumptions:

- No air
- Pure conduction
- No radiation
- Heating zone = 5% of die surface

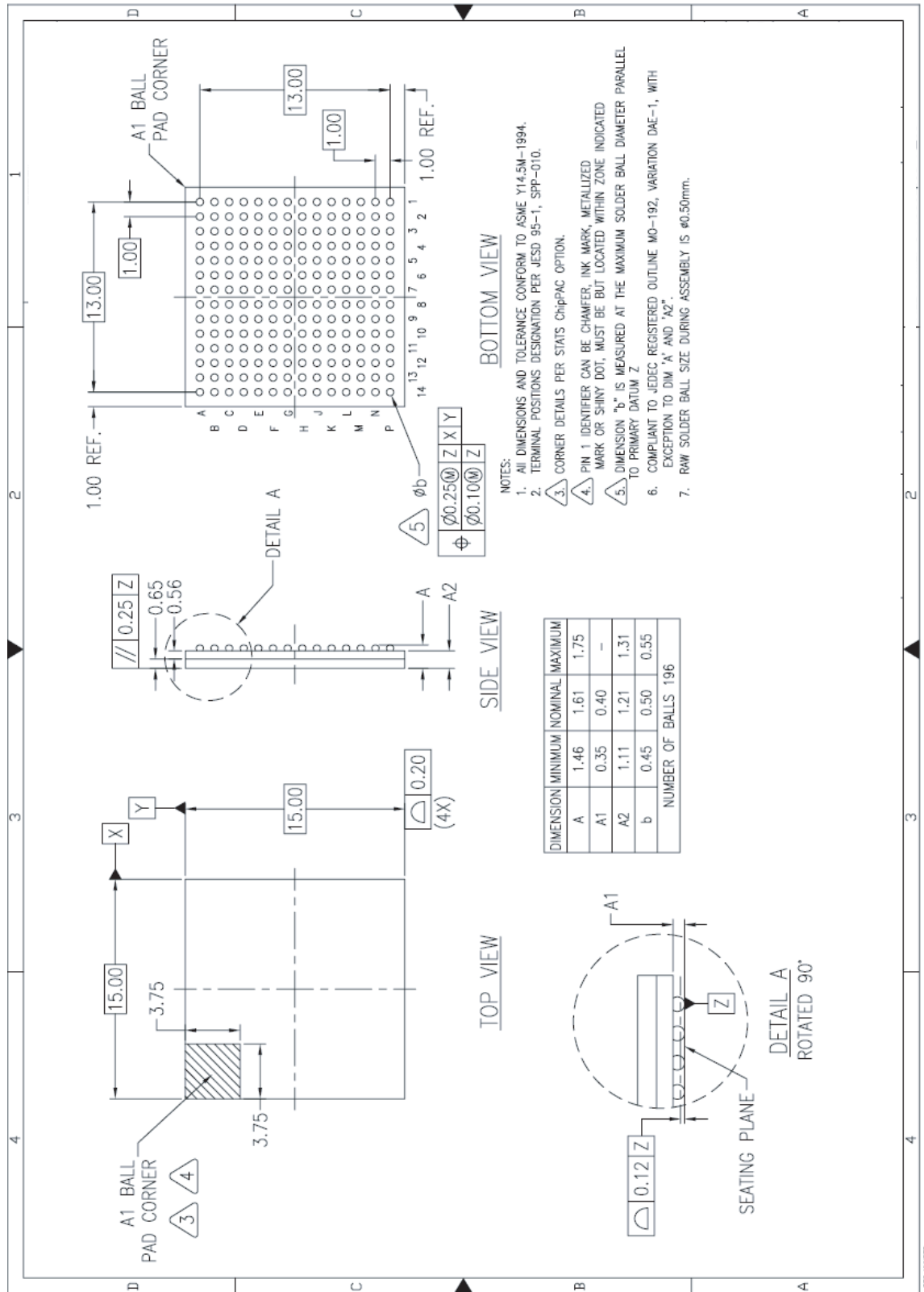
- Rth Junction to bottom of Balls = 13.6°C/W
- Rth Junction to board (JEDEC JESD-51-8) = 18.4°C/W
- Rth Junction to top of case = 17.0°C/W

Assumptions:

- Heating zone = 5% of die surface
- Still air, Jedec condition

- Rth Junction to ambient (JEDEC) = 32.3°C/W

8. Package Information fpBGA196



9. Ordering Information

Table 9-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX10AS180ZPY	fpBGA196 RoHS	Ambient	Prototype	
EV10AS180CZPY	fpBGA196 RoHS	0°C < T <sub>amb</sub> < +70°C	Commercial Grade	
EV10AS180VZPY	fpBGA196 RoHS	-40°C < T <sub>amb</sub> < +85°C	Industrial Grade	
EV10AS180ZPY-EB	fpBGA196 RoHS	Ambient	Prototype	Evaluation board



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